Linear Phase 8th Order Lowpass Filter

DESCRIPTION

The LTC1064-7M/883 is a clock-tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband while it exhibits steeper roll-off than an equivalent 8th order Bessel filter. For instance, at twice the cutoff frequency the filter attains 34dB attenuation (vs 12dB for Bessel), while at three times the cutoff frequency the filter attains 68dB attenuation (vs 30dB for Bessel). The cutoff frequency of the LTC1064-7M/883 is tuned via an external TTL or CMOS clock.

The LTC1064-7M/883 features wide dynamic range. With single 5V supply, the S/N + THD is 76dB. Optimum 92dB S/N is obtained with ±7.5V supplies.

The clock-to-cutoff frequency ratio of the LTC1064-7M/883 can be set to 50:1 (pin 10 to V^+) or 100:1 (pin 10 to V^-).

When the filter operates at clock-to-cutoff frequency ratio of 50:1, the input is double-sampled to lower the risk of aliasing.

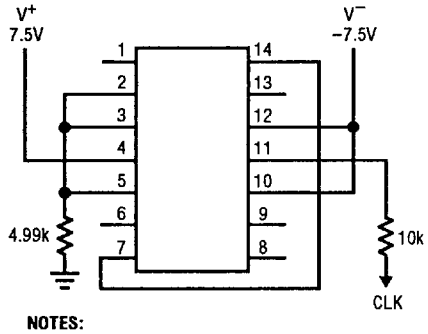
The LTC1064-7M/883 is pin-compatible with the LTC1064-X series, LTC1164-7 and LTC1264-7.

The device is processed to the requirements of MIL-STD-883 Class B to yield circuits usable in precision military applications.

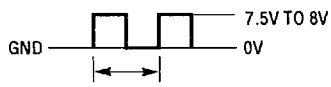
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16V
Power Dissipation 400mW
Burn-In Voltage 16V
Voltage at Any Input ..... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Storage Temperature Range ..... −65°C to 150°C
Operating Temperature Range ..... −55°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

BURN-IN CIRCUIT



NOTES:
1. T_A = 125°C
2. BURN-IN VOLTAGES: V^+ = 7.5V TO 8V
   V^- = −7.5V TO −8V
3. CLK = SQUARE WAVE,



FREQUENCY = 1kHz ±10%

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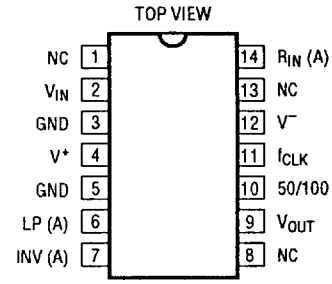
PACKAGE/ORDER INFORMATION



J PACKAGE
14-LEAD CERAMIC DIP

T_{JMAX} = 150°C, θ_{JA} = 65°C/W

ORDER PART NUMBER
LTC1064-7M/883
PART MARKINGS†
LTC1064-7M/883C

† The suffix letter "C" of the part mark indicates compliance per MIL-STD-883, para 1.2.1.1.

TABLE 1: ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, f_{CUTOFF} = 10kHz or 20kHz, f_{CLK} = 1MHz, TTL or CMOS level (maximum clock rise or fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified.

PARAMETER	CONDITIONS	NOTES	MIN	MAX	SUB-GROUP	UNITS
Passband Gain	0.1Hz ≤ f ≤ 0.25 f_{CUTOFF}					
	f_{TEST} = 5kHz, (f_{CLK}/f_C) = 50:1		−0.60	0.65	1,2,3	dB
Gain at 0.50f_{CUTOFF}	f_{TEST} = 10kHz, (f_{CLK}/f_C) = 50:1	3	−0.90	0.15	1,2,3	dB
	f_{TEST} = 5kHz, (f_{CLK}/f_C) = 100:1	3	−1.30	1.25	1,2,3	dB
Gain at 0.75f_{CUTOFF}	f_{TEST} = 15kHz, (f_{CLK}/f_C) = 50:1	1	−2.0	−0.35	1,2,3	dB
Gain at f_{CUTOFF}	f_{TEST} = 20kHz, (f_{CLK}/f_C) = 50:1		−4.50	−2.50	1,2,3	dB
	f_{TEST} = 10kHz, (f_{CLK}/f_C) = 100:1		−5.75	−3.75	1,2,3	dB
Gain at 2f_{CUTOFF}	f_{TEST} = 40kHz, (f_{CLK}/f_C) = 50:1		−36.5	−31.75	1,2,3	dB
	f_{TEST} = 20kHz, (f_{CLK}/f_C) = 100:1		−37.0	−31.75	1,2,3	dB
Gain with f_{CLK} = 20kHz	f_{TEST} = 200Hz, (f_{CLK}/f_C) = 100:1		−6.5	−3.5	1	dB
Gain with f_{CLK} = 400kHz, V_S = ±2.375V	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 50:1		−0.9	0.25	1	dB
	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 50:1		−4.5	−2.00	1	dB
Phase Factor (F) Phase = 180° − $F(f/f_C)$	0.1Hz ≤ f ≤ f_{CUTOFF}					
	(f_{CLK}/f_C) = 50:1	1	422	437	1,2,3	Deg
	(f_{CLK}/f_C) = 100:1	1	414	429	1,2,3	Deg
Phase Nonlinearity	(f_{CLK}/f_C) = 50:1	1		±4.0	1,2,3	%
	(f_{CLK}/f_C) = 100:1	1		±4.0	1,2,3	%
Group Delay (t_d) $t_d = (F/360)(1/f_C)$	(f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF}	2	58.6	60.7	1,2,3	µs
	(f_{CLK}/f_C) = 100:1, f ≤ f_{CUTOFF}	2	115.0	119.0	1,2,3	µs
Group Delay Deviation	(f_{CLK}/f_C) = 50:1, f ≤ f_{CUTOFF}	2		±4.0	1,2,3	%
	(f_{CLK}/f_C) = 100:1, f ≤ f_{CUTOFF}	2		±4.0	1,2,3	%
Input Impedance			25	70	1	kΩ
Output DC Voltage Swing	V_S = ±2.375V	4	±1.0		4	V
	V_S = ±5V	4	±2.1		4,5,6	V
	V_S = ±7.5V	4	±3.0		4,5,6	V
Output DC Offset	50:1, V_S = ±5V			±220	4	mV
Power Supply Current (f_{CLK} = 1MHz)	V_S = ±2.375V			22	1	mA
				22	2,3	mA
	V_S = ±5V			25	1	mA
				30	2,3	mA
	V_S = ±7.5V			30	1	mA
				35	2,3	mA
Power Supply Range			±2.375	±7.5	1	V

TABLE 1: ELECTRICAL CHARACTERISTICS

Note 1: Input frequencies, f, are linearly phase shifted through the filter as long as $f \leq f_C$; f_C = cutoff frequency.

Figure 1 curve shows the typical phase response of an LTC1064-7M/883 operating at f_{CLK} = 1MHz, ratio = 50:1, f_C = 20kHz and it closely matches an ideal straight line. The phase shift is described by: phase shift = 180° – $F(f/f_C)$; $f \leq f_C$.

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor allows the calculation of the phase at a given frequency. Example: the phase shift at 14kHz of the LTC1064-7 shown in Figure 1 is: phase shift = 180° – 430° (14kHz/20kHz) ± nonlinearity = –121° ± 1% or –121° ± 1.20°.

Note 2: Group delay and group delay deviation are calculated from the measured phase factor and phase deviation specifications.

Note 3: The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

Note 4: The AC swing is typically $11V_{P-P}$, $7V_{P-P}$, $2.8V_{P-P}$, with ±7.5V, ±5V, ±2.5V supply respectively. For more information refer to the THD + Noise vs Input graphs in the LTC1064-7 standard data sheet.

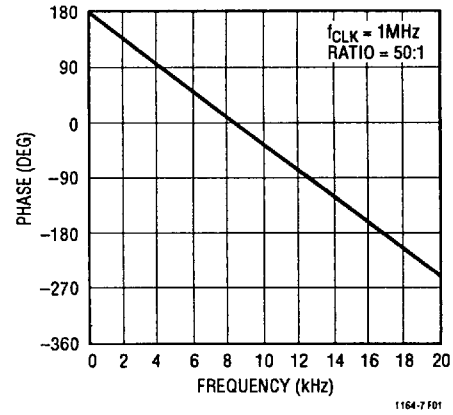


Figure 1. Phase Response in the Passband (Note 1)

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6
Group A Test Requirements (Method 5005)	1,2,3,4,5,6
Group C and D End Point Electrical Parameters (Method 5005)	1,2,3,4,5,6

* PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.