

TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9472F

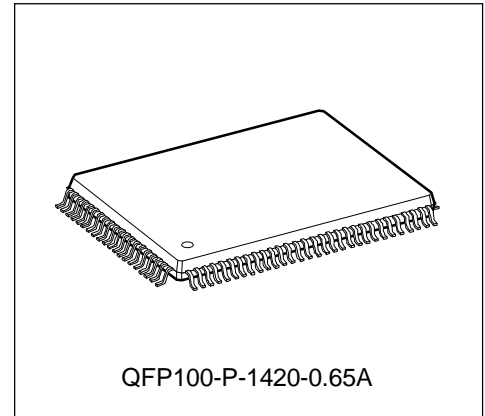
1 chip AUDIO DIGITAL SIGNAL PROCESSOR

TC9472F is the 1 chip audio DSP which built in 24-bits, a 22.5 MIPS DSP core, 3 ch AD converter, 5 ch DA converter, and electronic volume for trims, and corresponds to a Multi-speaker system.

It is possible to realize many application, such as sound field control - hall simulation, for example -, digital filter for equalizers, dynamic range control, KARAOKE and something.

FEATURES

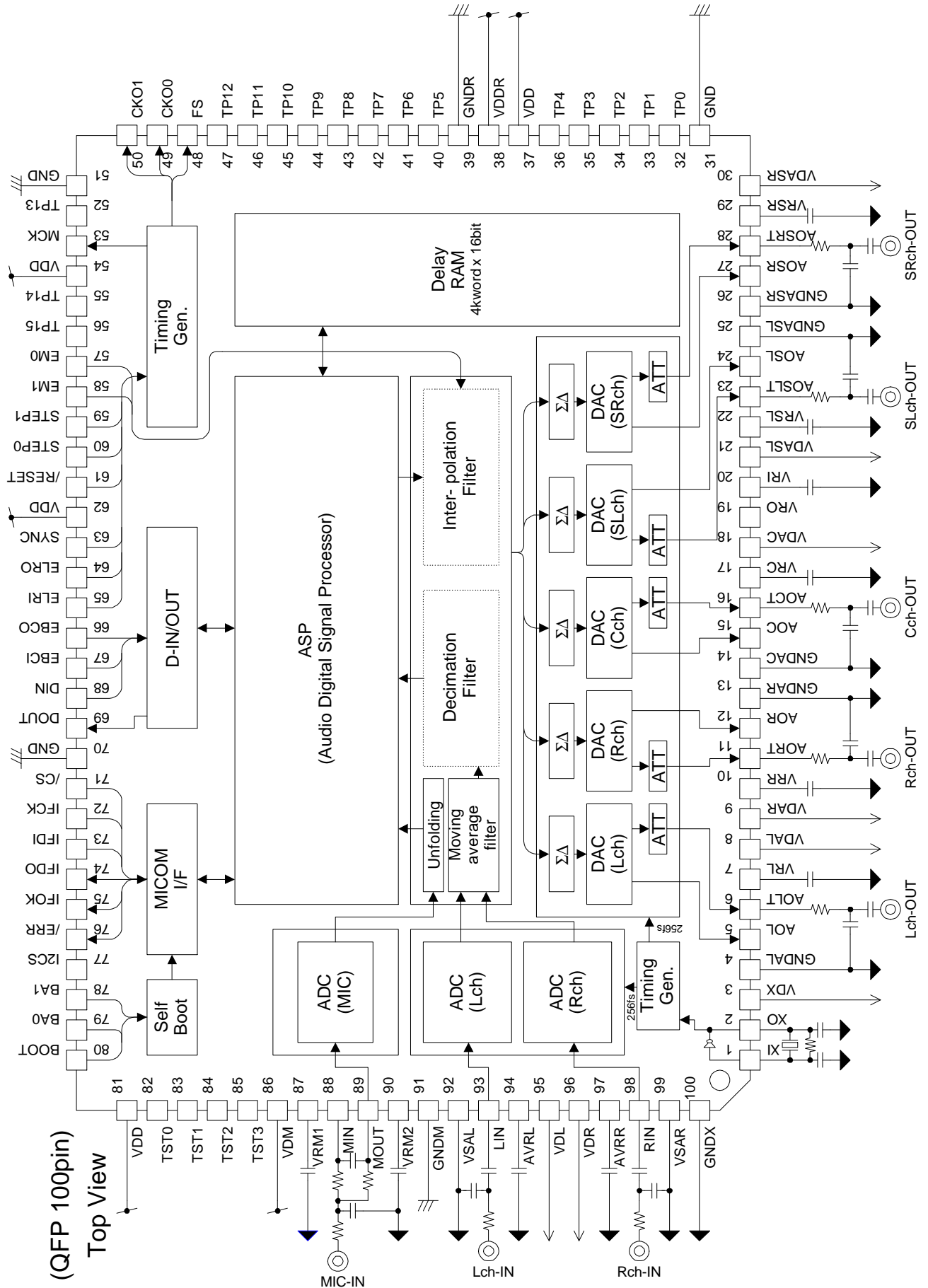
- Incorporates 3 ch AD converter, 2 ch is 1bit Σ - Δ type AD converter for HiFi - Audio and 1 ch is 16 bit Multi-bit type AD converter for Microphone.
 - 2 ch HiFi-ADC (1bit Σ - Δ type) S / N : 98 dB (typ.)
 - 1 ch Mic. ADC (16 bit Multi - bit type) S / N : 80 dB (typ.)
- Incorporates 1bit Σ - Δ type DA converter, and the attenuator for trims is built in each DAC output. In case of the use which does not use a trim, It is possible to output the analog signal of DAC directly.
 - 5 ch DAC (1bit Σ - Δ type) S / N : 100 dB (typ.)
- A built-in self-boot function automatically sets the coefficients and register values at initialization.
 - Boot ROM : 1024 word x 18 bit
- The DSP block specification are as follows :
 - Data bus : 24 bit
 - Multiplier / adder : 24 bit x 16 bit + 43 bit => 43 bit
 - Accumulator : 43 bit (sign extension : 4 bit)
 - Program ROM : 2048 word x 32 bit
 - Coefficient RAM : 448 word x 16 bit
 - Coefficient ROM : 256 word x 16 bit
 - Offset RAM : 64 word x 16 bit
 - Data RAM : 256 word x 24 bit
 - Operation speed : 44 ns (510-step (approx.) operation per cycle at fs = 44.1 kHz)
 - Interface buffer RAM : 32 word x 16 bit
- Incorporates data delay RAM of 64 kbit.
 - Delay RAM : 4096 word x 16 bit (64 kbit)
- The microcontroller interface can be selected between TOSHIBA original 3 line type and I2C bus format.
- CMOS silicon structure supports high speed.
- The package is a 100-pin flat package.



Weight : 1.57g (typ.)

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BLOCK DIAGRAM / PIN CONNECTION



PIN FUNCTION

PIN No.	SYMBOL	I / O	FUNCTION	REMARKS
1	XI	I	Crystal oscillator connect or external clock input pin	
2	XO	O	Crystal oscillator connect pin	
3	VDX	-	Power pin for oscillator circuit	
4	GNDAL	-	Ground pin for DAC Left channel	
5	AOL	O	DAC Left channel signal output pin	
6	AOLT	O	DAC Left channel attenuator output pin	
7	VRL	-	Reference voltage pin for DAC Left channel	
8	VDAL	-	Power pin for DAC Left channel	
9	VDAR	-	Power pin for DAC Right channel	
10	VRR	-	Reference voltage pin for DAC Right channel	
11	AORT	O	DAC Right channel attenuator output pin	
12	AOR	O	DAC Right channel signal output pin	
13	GNDAR	-	Ground pin for DAC Right channel	
14	GNDAC	-	Ground pin for DAC Center channel	
15	AOC	O	DAC Center channel signal output pin	
16	AOCT	O	DAC Center channel attenuator output pin	
17	VRC	-	Reference power pin for DAC Center channel	
18	VDAC	-	Power pin for DAC Center channel	
19	VRO	O	Reference voltage pin for attenuator (Buffer output)	
20	VRI	I	Reference voltage pin for attenuator (Buffer input)	
21	VDASL	-	Power pin for DAC SL channel	
22	VRSL	-	Reference voltage pin for DAC SL channel	
23	AOSLT	O	DAC SL channel attenuator output pin	
24	AOSL	O	DAC SL channel signal output pin	
25	GNDASL	-	Ground pin for DAC SL channel	
26	GNDASR	-	Ground pin for DAC SR channel	
27	AOSR	O	DAC SR channel signal output pin	
28	AOSRT	O	DAC SR channel attenuator output pin	
29	VRSR	-	Reference voltage pin for DAC SR channel	
30	VDASR	-	Power pin for DAC SR channel	
31	GND	-	Ground pin	
32	TP0	O	Test pin 0	
33	TP1	O	Test pin 1	

PIN No.	SYMBOL	I / O	FUNCTION	REMARKS
34	TP2	O	Test pin 2	
35	TP3	O	Test pin 3	
36	TP4	O	Test pin 4	
37	VDD	-	Power pin	
38	VDDR	-	Power pin for delay RAM	
39	GNDR	-	Ground pin for delay RAM	
40	TP5	O	Test pin 5	
41	TP6	O	Test pin 6	
42	TP7	O	Test pin 7	
43	TP8	O	Test pin 8	
44	TP9	O	Test pin 9	
45	TP10	O	Test pin 10	
46	TP11	O	Test pin 11	
47	TP12	O	Test pin 12	
48	FS	O	Clock out pin (Sampling frequency)	
49	CKO0	O	Clock output pin 0	
50	CKO1	O	Clock output pin 1	
51	GND	-	Ground pin	
52	TP13	O	Test pin 3	
53	MCK	O	MCK clock output pin	
54	VDD	-	Power pin	
55	TP14	O	Test pin 14	
56	TP15	O	Test pin 15	
57	EM0	I	De-emphasis setting pin 0	Schmitt input
58	EM1	I	De-emphasis setting pin 1	Schmitt input
59	STEP1	I	ASP execution step switching pin 1	Schmitt input
60	STEP0	I	ASP execution step switching pin 0	Schmitt input
61	/RESET	I	Reset pin	Schmitt input
62	VDD	-	Power pin	
63	SYNC	I	Program synchronous signal input pin	Schmitt input
64	ELRO	I	LR clock input pin for serial data output (DOUT)	Schmitt input
65	ELRI	I	LR clock output pin for serial data input (DIN)	Schmitt input
66	EBCO	I	Bit clock input pin for serial data output (DOUT)	Schmitt input
67	EBCI	I	Bit clock input pin for serial data output (DIN)	Schmitt input

PIN No.	SYMBOL	I / O	FUNCTION	REMARKS
68	DIN	I	Serial data input pin	Schmitt input
69	DOUT	O	Serial data output pin	
70	GND	-	Ground pin	
71	/CS	I	Microcontroller interface chip select signal input pin	Schmitt input
72	IFCK	I	Microcontroller interface data shift clock signal input pin	Schmitt input
73	IFDI	I	Microcontroller interface data input pin	Schmitt input
74	IFDO	O	Microcontroller interface data output pin	
75	IFOK	O	Microcontroller interface operation flag pin	Open drain output
76	/ERR	O	Error flag output pin	Open drain output
77	I2CS	I	Microcontroller interface I2C bus / 3 line bus switching pin	
78	BA1	I	Boot address setting pin 1	Schmitt input
79	BA0	I	Boot address setting pin 0	Schmitt input
80	BOOT	I	Self boot control pin	Schmitt input
81	VDD	-	Power pin	
82	TST0	I	Test pin T0	Schmitt input
83	TST1	I	Test pin T1	Schmitt input
84	TST2	I	Test pin T2	Schmitt input
85	TST3	I	Test pin T3	Schmitt input
86	VDM	-	Power pin for microphone ADC	
87	VRM1	-	Reference voltage pin 1 for microphone ADC	
88	MIN	I	Microphone ADC amplifier input pin	
89	MOUT	O	Microphone ADC amplifier output pin	
90	VRM2	-	Reference voltage pin 2 microphone ADC	
91	GNDM	-	Ground pin for microphone ADC	
92	VSAL	-	Ground pin for ADC L channel	
93	LIN	I	ADC L channel signal input pin	
94	AVRL	-	Reference voltage pin for ADC L channel	
95	VDL	-	Power pin for ADC L channel	
96	VDR	-	Power pin for ADC R channel	
97	AVRR	-	Reference voltage pin for ADC R channel	
98	RIN	I	ADC R ch signal input pin	
99	VSAR	-	Ground pin for ADC R channel	
100	GNDX	-	Ground pin for oscillator circuit	

MAXMUM RATINGS (Ta=25 degrees centigrade)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{DD}	-0.3 ~ 6.0	V
Input Voltage	V _{in}	-0.3 ~ V _{DD} + 0.3	V
Power Dissipation	P _D	1500	mW
Operating Temperature	T _{opr}	-40 ~ 75 (Notes)	degrees centigrade
Storage Temperature	T _{stg}	-55 ~ 150	degrees centigrade

(Notes) When operating frequency is 340-step mode, operating temperature is Ta=-40~85 degrees centigrade.

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, Ta=-25 degrees centigrade,

VDD=VDX=VDDR=VDM=VDL=VDR=VDX=VDAL=VDAR=VDAC=VDAS=VDASR=5.0V)

DC Characteristics

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	V _{DD}	-	Ta=-40~75 degrees centigrade	4.75	5.0	5.25	V
Operating Frequency Range	f _{opr}	-	340-step mode	8	15	25	MHz
			511-step mode	12	33.8	34	
Operating Power Supply Current	I _{DD}	-	f _{opr} =33.8688MHz, 511-step mode	-	135	150	mA

Clock Pins (XI, XO)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage(1)	"H" LEVEL	V _{IH1}	XI pin	3.5	-	-	V
	"L" LEVEL	V _{IL1}		-	-	1.5	
Output Voltage(1)	"H" LEVEL	V _{OH1}	I _{OH} =-3.0mA	4.5	-	-	
	"L"LEVEL	V _{OL1}	I _{OL} = 5.0mA	-	-	0.5	

Input Pins

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage(2)	"H" LEVEL	V _{IH2}	(Note 1)	4.0	-	-	V
	"L" LEVEL	V _{IL2}		-	-	1.0	
Input Leakage Current	"H" LEVEL	I _{IH2}	V _{IN} =V _{DD}	-	-	10	μA
	"L" LEVEL	I _{IL2}	V _{IN} =0V	-10	-	-	

(Note 1) XI, STEP0~1, /RESET, SYNC, ELRO, ELRI, EBCO, EBCI, DIN, EM0~1,

I2CS, /CS, IFCK, IFDI, BOOT, BA0~BA1, TST0~3 (Normally input pins and Schmitt input pins)

Output Pins

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage(2)	"H" LEVEL	V _{OH2}	I _{OH} =-2.0mA	4.5	-	-	V
	"L" LEVEL	V _{OL2}	I _{OL} = 2.0mA	-	-	0.5	
Output Voltage(3)	"L" LEVEL	V _{OL3}	I _{OL} = 4.0mA	-	-	0.5	
Output Open Leakage Current	I _{OZ4}	-	V _{OH} =V _{DD}	-10	-	+10	

(Note 2) FS, CKO0~1, MCK, DOUT, IFDO (Normally output)

(Note 3) IFDI (When I2C mode output), IFOK, /ERR(Open drain output)

AC Characteristics

AD converter (1) : LIN and RIN pins

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Input Signal Level	V_i	-	Input level for ADC output at full-scale digital output (Note 1)	1.18	1.25	-	Vrms
Input Impedance	Z_{in}	-	LIN, RIN pins	-	27	-	k Ω
S / (N+D) ratio	S / N_{a1}	-	A-Weight, X'tal : 33.8688MHz (Note 1)	90	98	-	dB
	S / N_{a2}	-	CCIR-ARM, X'tal : 33.8688MHz (Note 1)	87	92	-	
THD+N	THD_a	-	20kHz LPF, X'tal : 33.8688MHz (Note 1)	-	-80	-70	dB
Cross-talk	CT_a	-	A-Weight, X'tal : 33.8688MHz (Note 1)	-	-90	-83	dB
Dynamic Range	DR_a	-	A-Weight, X'tal : 33.8688MHz (Note 1)	85	92	-	dB

(Note 1) Input channels : LIN, RIN

AD converter (2) : MIN pin

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Input Signal Level	V_{iM}	-	Input level for ADC output at full-scale digital output (Note 1)	-	1.0	1.15	Vrms
Input Impedance	Z_{inM}	-	MIN pin	-	1	-	k Ω
S / (N+D) ratio	S / N_{aM}	-	A-Weight, X'tal : 33.8688MHz (Note 1)	70	80	-	dB
THD+N	THD_{aM}	-	20kHz LPF, X'tal : 33.8688MHz (Note 1)	-	-62	-55	dB
Cross-talk	CT_{aM1}	-	LIN, RIN to MIN (Note 2)	-	-76	-60	dB
	CT_{aM2}	-	MIN to LIN, RIN (Note 2)	-	-90	-83	

(Note 1) Input channel: MIN

(Note 2) Input channels: LIN, RI, MIN

DA converter

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Signal Level	A _{o1}	-	Output voltage at full-scale digital input (Note 1)	1.13	1.18	1.25	V _{rms}
	A _{o2}	-	Output voltage at full-scale digital input (Note 2)	1.43	1.48	1.55	
S / N ratio	S / N _d	-	A-Weight, X'tal : 33.8688MHz (Note 3)	90	100	-	dB
THD+N	THD _{d1}	-	20kHz LPF, X'tal : 33.8688MHz (Note 1)	-	-85	-78	dB
	THD _{d2}		20kHz LPF, X'tal : 33.8688MHz (Note 2)	-	-82	-75	
Cross-talk	CT _{d1}	-	20kHz LPF, X'tal : 33.8688MHz AOLT - AORT ch	-	-73	-66	dB
	CT _{d2}		20kHz LPF, X'tal : 33.8688MHz AORT- AOCT-AOSLT-AOSRT ch	-	-90	-83	
	CT _{d3}		20kHz LPF, X'tal : 33.8688MHz AOL-AOR-AOC-AOSL-AOSR ch	-	-97	-90	
Dynamic Range	DR _d	-	A-Weight, X'tal : 33.8688MHz (Note 3)	88	95	-	dB

(Note 1) Output channel : AOL, AOR, AOC, AOSL, AOSR

(Note 2) Output channel : AOLT, AORT, AOCT, AOSLT, AOSRT

(Note 3) Output channel : AOL, AOR, AOC, AOSL, AOSR, AOLT, AORT, AOCT, AOSLT, AOSRT

Timing

Clock Input Pin (XI)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Cycle	t_{XI}	-	-	29	-	-	ns
Clock "H" Cycle Width	t_{XIH}	-	-	-	14.5	-	
Clock "L" Cycle Width	t_{XIL}	-	-	-	14.5	-	

Reset Pin (/RESET)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Standby Time	t_{RRS}	-	-	10	-	-	ms
Reset Pulth Width	t_{WRS}	-	-	1.0	-	-	μ s

Timing Output

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CKO Output Delay Time	t_{DFC}	-	-	-150	-	150	ns

Audio Serial Interface (EBCI, DIN, EBCO, DOUT)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ELRI Hold Time	t_{LIH}	-	-	-75	-	75	ns
DIN Setup Time	t_{SDI}	-	-	50	-	-	
DIN Hold Time	t_{HDI}	-	-	50	-	-	
EBCI Clock Cycle	t_{EBCI}	-	-	300	-	-	
EBCI Clock "H" Cycle Width	t_{EBIH}	-	-	150	-	-	
EBCI Clock "L" Cycle Width	t_{EBIL}	-	-	150	-	-	
ERLO Hold Time	t_{LOH}	-	-	-75	-	75	
DOUT Output Delay Time(1)	t_{DO1}	-	-	-	-	60	
DOUT Output Delay Time(2)	t_{DO2}	-	-	-	-	60	
EBCO Clock Cycle	t_{EBCO}	-	-	300	-	-	
EBCO Clock "H" Cycle Width	t_{EBOH}	-	-	150	-	-	
EBCO Clock "L" Cycle Width	t_{EBOL}	-	-	150	-	-	

Microcontroller Interface

(1) Standard Transmission Mode (/CS, IFCK, IFDI, IFDO)

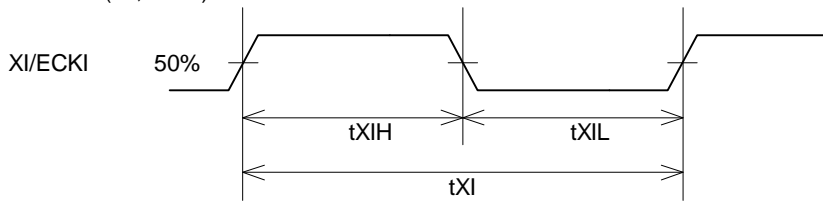
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Standby Time	t _{STB}	-	-	1.0	-	-	μs
/CS falling edge - IFCK falling edge Setup Time	t _{CCD}	-	-	0.2	-	-	
IFCK "L" Cycle Width	t _{WLC}	-	-	0.25	-	-	
IFCK "H" Cycle Width	t _{WHC}	-	-	0.25	-	-	
IFCK rising edge - /CS rising edge Setup Time	t _{CKC}	-	-	0.2	-	-	
/CS "H" Cycle Width	t _{WCS}	-	-	0.5	-	-	
IFDI - IFCK rising edge Setup Time	t _{SCD}	-	-	0.2	-	-	
IFCK rising edge - IFDI Hold Time	t _{HCD}	-	-	0.2	-	-	
IFCK falling edge - IFDO Propagation Delay Time	t _{DDO}	-	C _L =30pF	-	-	0.2	

(2) I2C Mode (/CS, IFCK, IFDI)

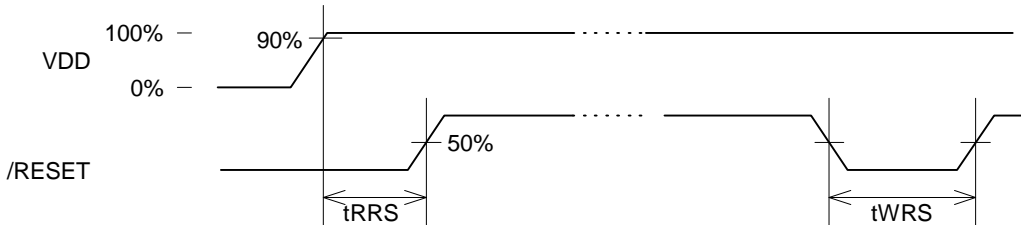
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IFCK Clock Frequency	t _{IFCK}	-	C _L =400pF	0	-	400	kHz
IFCK "H" Cycle Width	t _H	-	C _L =400pF	0.6	-	-	
IFCK "L" Cycle Width	t _L	-	C _L =400pF	1.3	-	-	
Data Setup Time	t _{DS}	-	C _L =400pF	0.1	-	-	
Data Hold Time	t _{DH}	-	C _L =400pF	0	-	-	
Transmission Start Condition Hold Time	t _{SCH}	-	C _L =400pF	0.6	-	-	
Repeat Transmission Start Condition Setup Time	t _{SCS}	-	C _L =400pF	0.6	-	-	
Transmission End Condition Setup Time	t _{ECS}	-	C _L =400pF	0.6	-	-	
Data Transmission Interval	t _{BUF}	-	C _L =400pF	1.3	-	-	
I2C Rising Time	t _R	-	C _L =400pF	-	-	0.3	
I2C Falling Time	t _F	-	C _L =400pF	-	-	0.3	

AC Characteristic Measurement Point

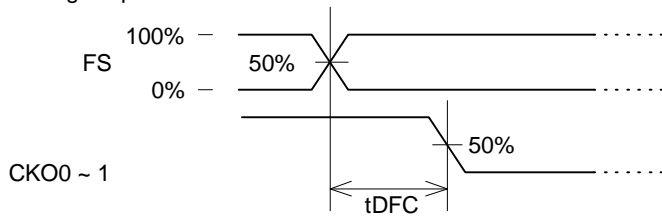
(1) Clock Pins (XI, ECKI)



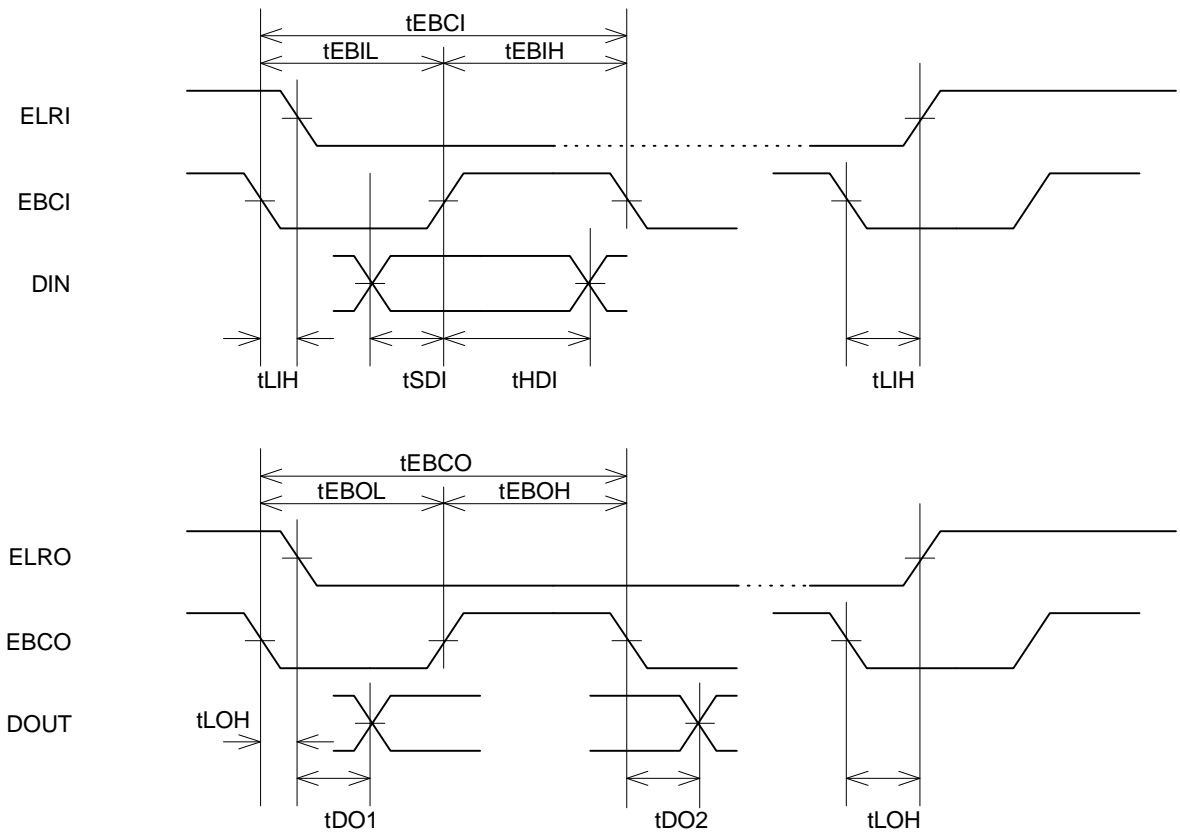
(2) Reset



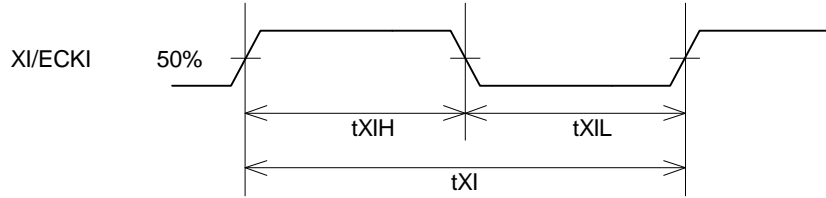
(3) Timing Output



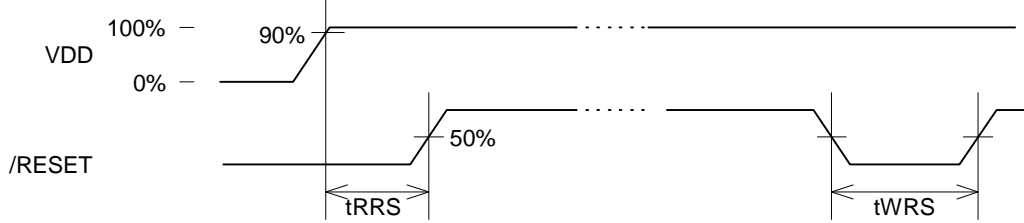
(4) Audio Serial Interface (ELRI, EBCI, DIN, ELRO, EBCO, DOUT)



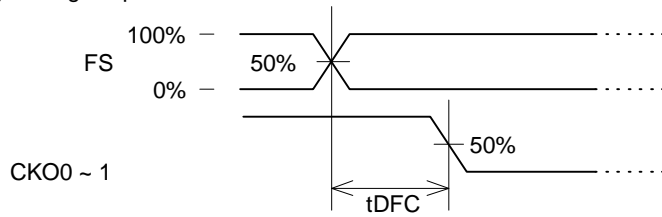
(1) Clock Pins (XI, ECKI)



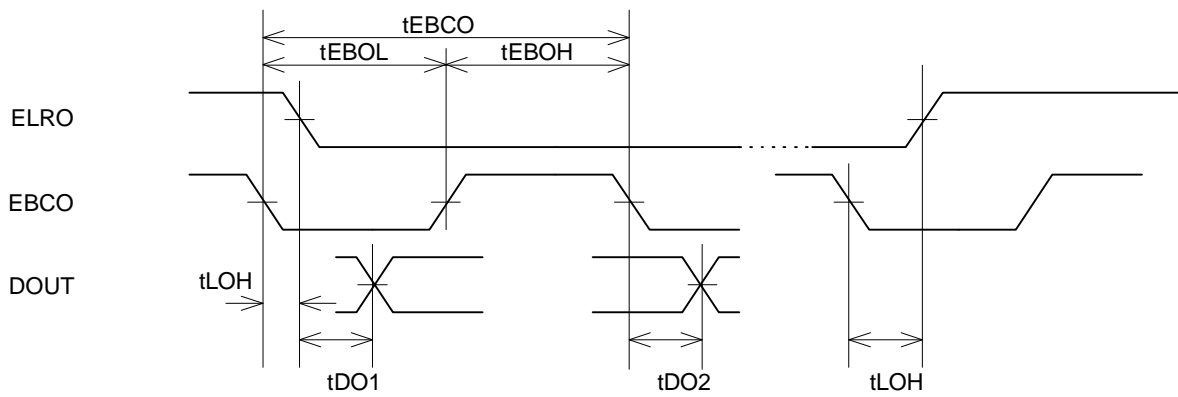
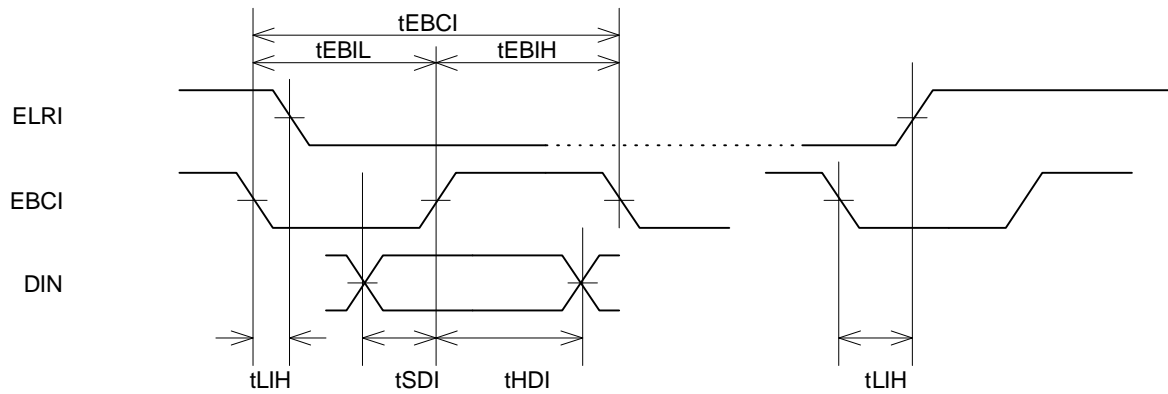
(2) Reset



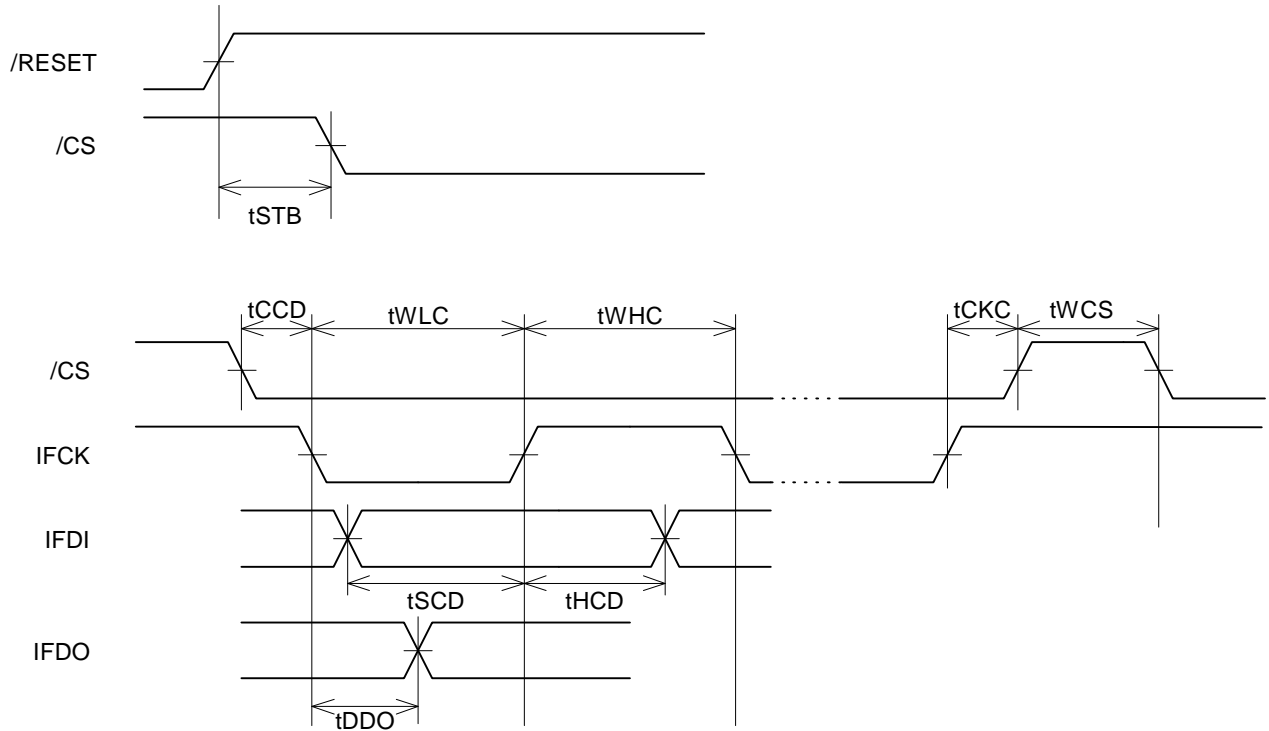
(3) Timing Output



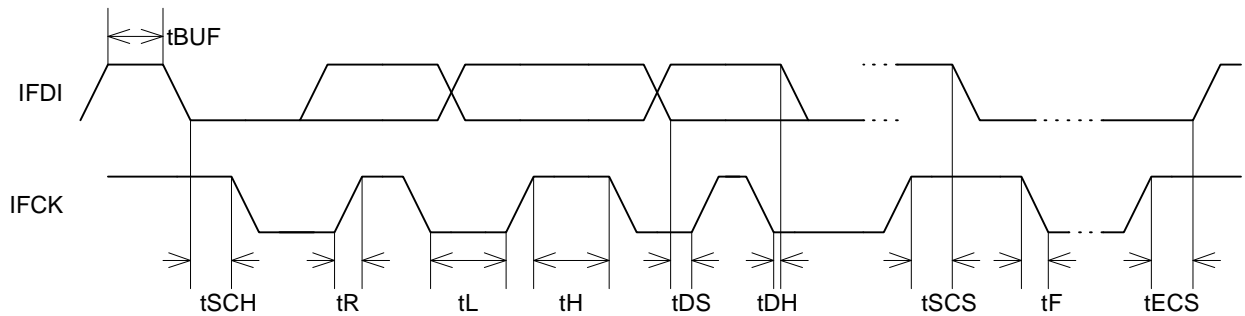
(4) Audio Serial Interface (ELRI, EBCI, DIN, ELRO, EBCO, DOUT)



(5) Micromicrocontroller Interface in Standard Transmission mode (/CS, IFCK, IFDI, IFDO)



(6) Micromicrocontroller Interface in I2C Mode (IFCK, IFDI)

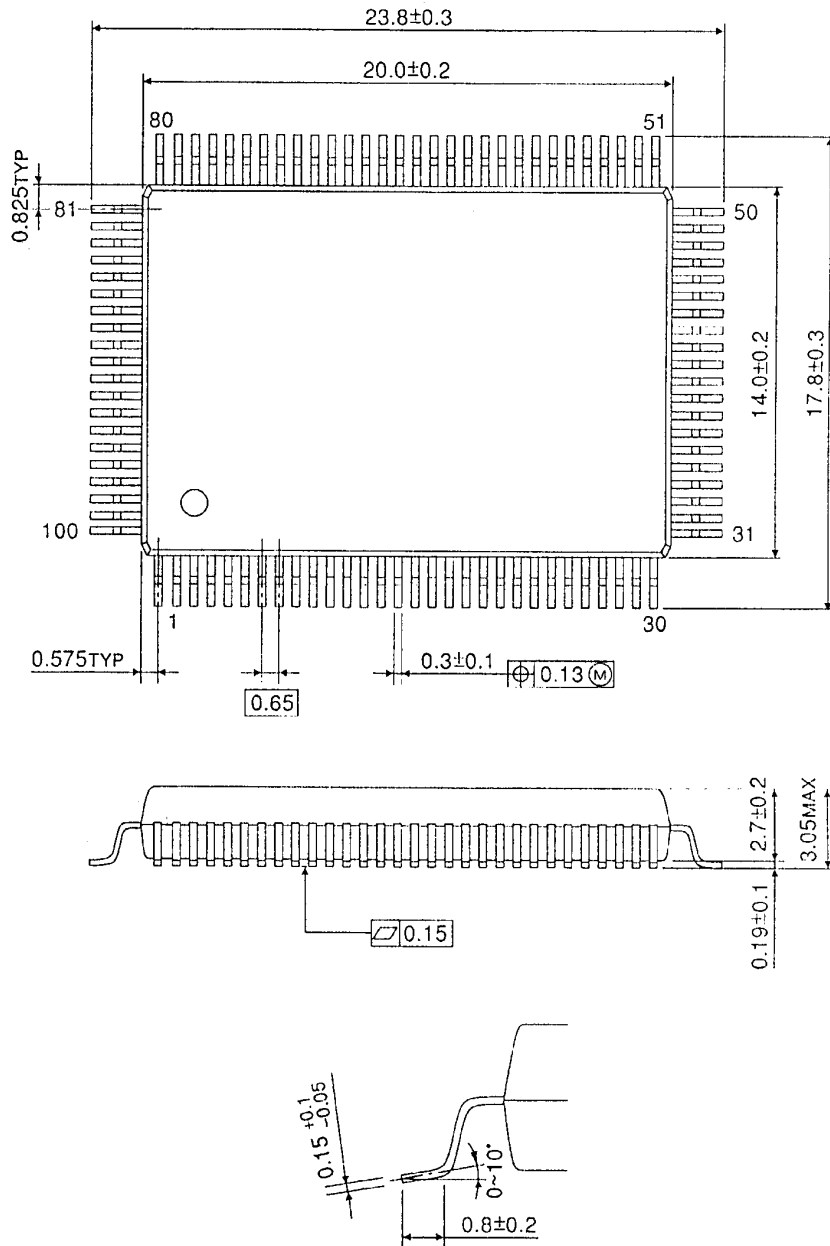


Purchase of TOSHIBA I2C components conveys a license under the Philips I2C Patent Right to use these components in an I2C system, provided that the system conforms to I2C Standard Specification as defined by Philips.

外形図

QFP100-P-1420-0.65A

単位 : mm



質量 : 1.57g (標準)