- **Organization**
  - Two 8K-Byte Parameter Blocks
  - One 96K-Byte Main Block
  - One 128K-Byte Main Block
  - One 16K-Byte Protected Boot Block
  - Top or Bottom Boot Locations
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time**

V_{CC} ± 5%	V_{CC} ± 10%	
'28F200BZ-6-x		60 ns
	'28F200BZ-70-x	70 ns
	'28F200BZ-80-x	80 ns
	'28F200BZ-90-x	90 ns

- **100000 and 10000 Program/Erase Cycle Versions**
- **Three Temperature Ranges**
  - Commercial . . . 0°C to 70°C
  - Extended . . . – 40°C to 85°C
  - Automotive . . . – 40°C to 125°C
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - Active Write . . . 330 mW (Byte Write)
  - Active Read . . . 330 mW (Byte Read)
  - Active Write . . . 358 mW (Word Write)
  - Active Read . . . 330 mW (Word Read)
  - Block Erase . . . 165 mW
  - Standby . . . 0.55 mW (CMOS-Input Levels)
  - Deep Power-Down Mode . . . 0.0066 mW
- **Fully Automated On-Chip Erase and Word/Byte Program Operations**
- **Write Protection for Boot Block**
- **Command State Machine (CSM)**
  - Erase Suspend/Resume
  - Algorithm-Selection Identifier

DBJ PACKAGE
(TOP VIEW)

V_{PP}	1	44	$\overline{RP}$
NC	2	43	$\overline{W}$
NC	3	42	A8
A7	4	41	A9
A6	5	40	A10
A5	6	39	A11
A4	7	38	A12
A3	8	37	A13
A2	9	36	A14
A1	10	35	A15
A0	11	34	A16
$\overline{E}$	12	33	$\overline{BYTE}$
V_{SS}	13	32	V_{SS}
$\overline{G}$	14	31	DQ15/A_{-1}
DQ0	15	30	DQ7
DQ8	16	29	DQ14
DQ1	17	28	DQ6
DQ9	18	27	DQ13
DQ2	19	26	DQ5
DQ10	20	25	DQ12
DQ3	21	24	DQ4
DQ11	22	23	V_{CC}

PIN NOMENCLATURE	
A0–A16	Address Inputs
$\overline{BYTE}$	Byte Enable
DQ0–DQ14	Data In/Out
DQ15/A_{-1}	Data In/Out (word-wide mode), Low-Order Address (byte-wide mode)
DU	Do Not Use
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{RP}$	Reset/Deep Power-Down
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply for Program/Erase
V_{SS}	Ground
$\overline{W}$	Write Enable

ADVANCE INFORMATION

description

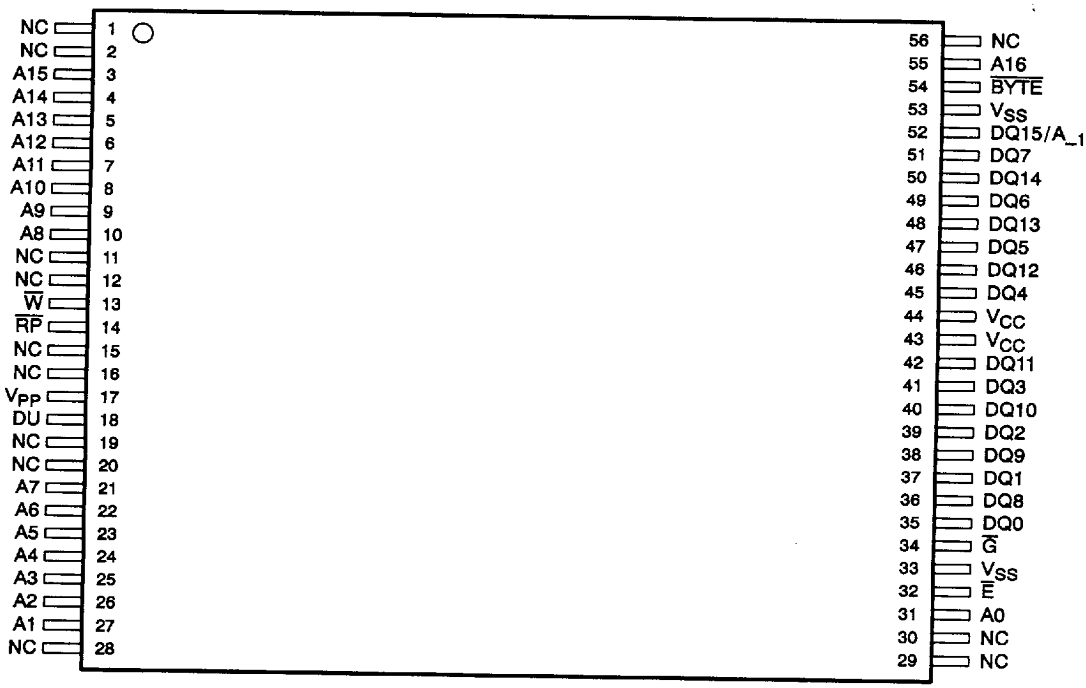
The TMS28F200BZx is a 2097152-bit, boot-block flash memory that can be electrically block erased and reprogrammed. The TMS28F200BZx is organized in a blocked architecture consisting of one 16K-byte protected boot block, two 8K-byte parameter blocks, one 96K-byte main block, and one 128K-byte main block. The device can be ordered with either a top or bottom boot-block configuration. Operation as a 256K-byte (8-bit) or a 128K-word (16-bit) organization is user-definable.

Embedded program and block-erase functions are fully automated by an on-chip write state machine (WSM), simplifying these operations and relieving the system microcontroller of these secondary tasks. WSM status can be monitored by an on-chip status register to determine progress of program/erase tasks. The device features user-selectable block erasure.

description (continued)

The TMS28F200BZx flash memory is offered in a 44-pin PSOP and a 56-pin TSOP package. It is available in three temperature ranges: 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C.

DBR PACKAGE
(TOP VIEW)



ADVANCE INFORMATION

device symbol nomenclature

TMS28F200BZT 6 C DBJ L

Temperature Range Designator
- L = 0°C to 70°C
- E = –40°C to 85°C
- Q = –40°C to 125°C

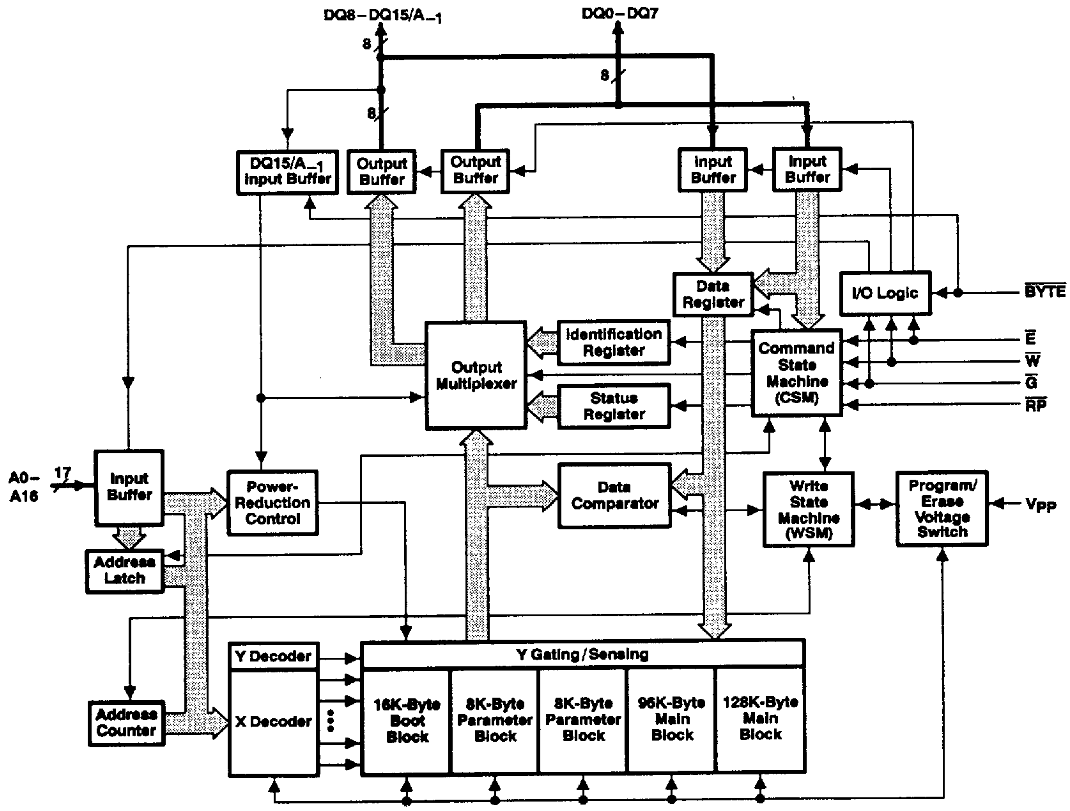
Package Designator
- DBJ = Plastic Small-Outline Package
- DBR = Thin Small-Outline Package

Program/Erase Endurance
- C = 100000 Cycles
- B = 10000 Cycles

Speed Designator
- 6 = 60 ns (±5% V_{CC} tolerance)
- 70 = 70 ns (±10% V_{CC} tolerance)
- 80 = 80 ns (±10% V_{CC} tolerance)
- 90 = 90 ns (±10% V_{CC} tolerance)

Boot Block Location Indicator
- T = Top Location
- B = Bottom Location

functional block diagram



architecture

The TMS28F200BZx uses a blocked architecture to allow independent erasure of selected memory blocks. Any address within a block address range selects that block for the required read, program, or erase operation.

block memory maps

The TMS28F200BZx is available with the block architecture mapped in either of two configurations: the boot block located at the top or at the bottom of the memory array, as required by different microprocessors. The TMS28F200BZB (bottom boot block) is mapped with the 16K-byte boot block located at the low-order address range (00000h to 01FFFh). The TMS28F200BZT (top boot block) is inverted with respect to the TMS28F200BZB with the boot block located at the high-order address range (1E000h to 1FFFFh). Both of these address ranges are for word-wide mode. Figure 2 and Figure 3 show the memory maps for these configurations.

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block memory maps (continued)

Address Range	×8 Configuration
3FFFFh – 3C000h	Boot Block 16K Addresses
3BFFFh – 3A000h	Parameter Block 8K Addresses
39FFFh – 38000h	Parameter Block 8K Addresses
37FFFh – 20000h	Main Block 96K Addresses
1FFFFh – 00000h	Main Block 128K Addresses

DQ15/A_{-1} Is LSB Address

×16 Configuration	Address Range
Boot Block 8K Addresses	1FFFFh – 1E000h
Parameter Block 4K Addresses	1DFFFh – 1D000h
Parameter Block 4K Addresses	1CFFFh – 1C000h
Main Block 48K Addresses	1BFFFh – 10000h
Main Block 64K Addresses	0FFFFh – 00000h

A0 Is LSB Address

Figure 1. TMS28F200BZT (Top Boot Block) Memory Map

Address Range	×8 Configuration
3FFFFh – 20000h	Main Block 128K Addresses
1FFFFh – 08000h	Main Block 96K Addresses
07FFFh – 06000h	Parameter Block 8K Addresses
05FFFh – 04000h	Parameter Block 8K Addresses
03FFFh – 00000h	Boot Block 16K Addresses

DQ15/A_{-1} Is LSB Address

×16 Configuration	Address Range
Main Block 64K Addresses	1FFFFh – 10000h
Main Block 48K Addresses	0FFFFh – 04000h
Parameter Block 4K Addresses	03FFFh – 03000h
Parameter Block 4K Addresses	02FFFh – 02000h
Boot Block 8K Addresses	01FFFh – 00000h

A0 Is LSB Address

Figure 2. TMS28F200BZB (Bottom Boot Block) Memory Map

boot-block data protection

The 16K-byte boot block is used to store key system data that is seldom changed in normal operation. To protect data within this memory sector, the $\overline{RP}$ terminal can be used to provide a lockout to eliminate accidental erase or program operations. When $\overline{RP}$ is operated with normal TTL/CMOS logic levels, the contents of the boot block cannot be erased or reprogrammed. Changes to the contents of the boot block can be made only when $\overline{RP}$ is at V_{HH} (nominally 12 V) during normal write/erase operations.

parameter block

Two parameter blocks of 8K bytes each can be used like a scratch pad to store frequently updated data. Alternately, the parameter blocks can be used for additional boot- or main-block data. If a parameter block is used to store additional boot-block data, caution should be exercised because the parameter block does not have the boot-block data-protection safety feature.

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main block

Primary memory on the TMS28F200BZx is located in two main blocks. One of the blocks has storage capacity of 128K bytes and the other block has storage capacity of 96K bytes.

command state machine (CSM)

The CSM is the interface between an external microprocessor and the write state machine and status register on the memory chip. When the WSM has completed a task, the WSM status (WSMS) bit (SB7) is set to a logic high (1), allowing the CSM to respond to the full command set.

status register (SR)

The status register provides a means of determining whether the state of a program/erase operation is pending or complete. The status register is read by writing a read-status command to the CSM and reading the resulting status code on I/O terminals DQ0–DQ7. This is valid for operation in either the byte- or word-wide mode. When the device is operating in the word-wide mode, the high order I/Os (DQ8–DQ15) are set to 00h when performing a read-status operation.

After a read-status command has been given, the data appearing on DQ0–DQ7 remains as the status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

Register data is updated on the falling edge of $\overline{G}$ or $\overline{E}$. The latest falling edge of either of these two signals updates the latch within a given read cycle. Latching data prevents errors from occurring should the register input change during a status-register read. To assure that the status-register output contains updated status data, $\overline{E}$ or $\overline{G}$ must be toggled for each subsequent status read.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSMS. Table 1 defines the status register bits and their functions.

status register (SR) (continued)

Table 1. Status Register Bit Definitions and Functions

STATUS BIT	FUNCTION	DATA	COMMENTS
SB7	Write-state-machine status (WSMS)	1 = Ready 0 = Busy	If SB7 = 0, the WSM has not completed an erase or programming operation. If SB7 = 1 (ready), other polling operations can be performed. SB7 does not automatically update WSM status at the completion of a WSM task. If the WSM status bit shows busy (0), the user must periodically toggle $\overline{E}$ or $\overline{G}$ to determine when the WSM has completed an operation (SB7 = 1).
SB6	Erase-suspend status (ESS)	1 = Erase suspended 0 = Erase in progress or completed	When an erase-suspend command is issued, the WSM halts execution and sets the ESS bit high (SB6 = 1) indicating that the erase operation has been suspended. The WSMS bit is also set high (SB7 = 1) indicating that the erase-suspend operation has been successfully completed. The ESS bit remains at a high level until an erase-resume command is input to the CSM (code D0h).
SB5	Erase status (ES)	1 = Block erase error 0 = Block erase good	SB5 = 0 indicates that a successful block erasure has occurred. SB5 = 1 indicates that an erase error has occurred. In this case, the WSM has completed the maximum allowed erase pulses determined by the internal algorithm, but this was insufficient to completely erase the device.
SB4	Program status (PS)	1 = Byte/word program error 0 = Byte/word program good	SB4 = 0 indicates successful programming has occurred at the addressed block location. SB4 = 1 indicates that the WSM was unable to correctly program the addressed block location.
SB3	V_{PP} status (V_{PPS})	1 = Program abort: V_{PP} too low 0 = V_{PP} good	SB3 provides information on the status of V_{PP} during programming. If V_{PP} is too low after a program or erase command has been issued, SB3 is set to a 1 indicating that the programming operation is aborted. The V_{PP} status bit is not assured to give accurate feedback between V_{PPH} and V_{PPL}.
SB2–SB0	Reserved		These bits should be masked out when reading the status register.

operation

Device operations are selected by entering standard JEDEC 8-bit command codes with conventional microprocessor timing into an on-chip command state machine (CSM) through I/O terminals DQ0–DQ7. When the device is powered up, internal reset circuitry initializes the chip to a read-array mode of operation. Changing the mode of operation requires a command code to be entered into the CSM. Table 2 lists the CSM codes for all modes of operation.

The on-chip status register allows the progress of various operations to be monitored. The status register is interrogated by entering a read-status-register command into the CSM (cycle 1) and reading the register data on I/O terminals DQ0–DQ7 (cycle 2). Status-register bits SB0 through SB7 correspond to DQ0 through DQ7.

operation (continued)

Table 2. Command State Machine Codes for Device Mode Selection

COMMAND CODE ON DQ0–DQ7†	DEVICE MODE
00h	Invalid/Reserved
10h	Alternate Program Setup
20h	Block-Erase Setup
40h	Program Setup
50h	Clear-Status Register
70h	Read-Status Register
90h	Algorithm Selection
B0h	Erase Suspend
D0h	Erase Resume/Block-Erase Confirm
FFh	Read Array

† DQ0 is the least significant bit. DQ8–DQ15 are any valid 2-state level.

command definition

Once a specific command code has been entered, the WSM executes an internal algorithm generating the necessary timing signals to program, erase, and verify data. See Table 3 for the CSM command definitions and data for each of the bus cycles.

Following the read-algorithm-selection-code command, two read cycles are required to access the manufacturer-equivalent code and the device-equivalent code as shown in Table 4 and Table 5.

Table 3. Command Definitions

COMMAND	BUS CYCLES REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	CSM INPUT	OPERATION	ADDRESS	DATA IN/OUT
Read Operations							
Read Array	1	Write	X	FFh	Read	X	Data Out
Read Algorithm-Selection Code	3	Write	X	90h	Read	A0	M/D
Read-Status Register	2	Write	X	70h	Read	X	SRB
Clear-Status Register	1	Write	X	50h			
Program Mode							
Program Setup/Program (byte/word)	2	Write	PA	40h or 10h	Write	PA	PD
Erase Operations							
Block-Erase Setup/ Block-Erase Confirm	2	Write	BEA	20h	Write	BEA	D0h
Erase Suspend/ Erase Resume	2	Write	X	B0h	Write	X	D0h

Legend:
- BEA Block-erase address. Any address selected within a block selects that block for erase.
- M/D Manufacturer-equivalent/device-equivalent code
- PA Address to be programmed
- PD Data to be programmed at PA
- SRB Status-register data byte that can be found on DQ0–DQ7

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byte-wide or word-wide mode selection

The memory array is divided into two parts: an upper half byte that outputs data through I/Os DQ8–DQ15, and a lower half byte that outputs data through DQ0–DQ7. Device operation in either byte-wide or word-wide mode is user-selectable and is determined by the logic state of $\overline{BYTE}$. When $\overline{BYTE}$ is at a logic high level, the device is in the word-wide mode and data is written to or read from I/Os DQ0–DQ15. When $\overline{BYTE}$ is at a logic low, the device is in the byte-wide mode and data is written to or read from I/Os DQ0–DQ7. In the byte-wide mode, I/Os DQ8–DQ14 are placed in the high-impedance state and DQ15/A_{-1} becomes the low-order address terminal and selects either the upper or lower half of the array. Array data from the upper half (DQ8–DQ15) and the lower half (DQ0–DQ7) are multiplexed and appear on DQ0–DQ7. Table 4 and Table 5 summarize operations for word-wide mode and byte-wide mode.

Table 4. Operation Modes for Word-Wide Mode ($\overline{BYTE}$ = V_{IH})

MODE	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ0–DQ15
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	Data out
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	Manufacturer-equivalent code 0089h
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	Device-equivalent code 2274h (top boot block)
								Device-equivalent code 2275h (bottom boot block)
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	High impedance
Standby	V_{IH}	X	V_{IH}	X	X	X	X	High impedance
Reset/deep power down	X	X	V_{IL}	X	X	X	X	High impedance
Write (see Note 1)	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	Data in

Table 5. Operation Modes for Byte-Wide Mode ($\overline{BYTE}$ = V_{IL})

MODE	$\overline{E}$	$\overline{G}$	$\overline{RP}$	$\overline{W}$	A9	A0	V_{PP}	DQ15/A_{-1}	DQ8–DQ14	DQ0–DQ7
Read lower byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IL}	Hi-Z	Data out
Read upper byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IH}	Hi-Z	Data out
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	X	Hi-Z	Manufacturer-equivalent code 89h
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	X	Hi-Z	Device-equivalent code 74h (top boot block)
										Device-equivalent code 75h (bottom boot block)
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z	High impedance
Standby	V_{IH}	X	V_{IH}	X	X	X	X	X	Hi-Z	High impedance
Reset/deep power down	X	X	V_{IL}	X	X	X	X	X	Hi-Z	High impedance
Write (see Note 1)	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	X	X	V_{PPL} or V_{PPH}	X	Hi-Z	Data in

NOTE 1: When writing commands to the '28F200BZx, V_{PP} must be V_{PPH} for block-erase or program commands to be executed and $\overline{RP}$ must be held at V_{HH} for the entire boot block program or erase operation.

command state machine (CSM) operations

The CSM decodes instructions for read, read algorithm-selection code, read status register, clear status register, program, erase, erase suspend, and erase resume. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 2 for CSM codes). During a program or erase cycle, the CSM informs the WSM that a program or erase cycle has been requested. During a program cycle, the WSM controls the program sequences and the CSM responds only to status reads.

During an erase cycle, the CSM responds to status reads and erase suspend. When the WSM has completed its task, the WSM status bit (SB7) is set to a logic high and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an erase or program operation only when V_{PP} is within its correct voltage range (V_{PPH}). For data protection, it is recommended that $\overline{RP}$ be held at a logic low during a CPU reset.

read operations

There are three read operations available: read array, read algorithm-selection code, and read status register.

read array

The array is read by entering the command code FFh on DQ0–DQ7. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}) to read data from the array. Data is available on DQ0–DQ15 (word-wide mode) or DQ0–DQ7 (byte-wide mode). Any valid address within any of the blocks selects that block and allows data to be read from the block.

read algorithm-selection code

Algorithm-selection codes are read by entering command code 90h on DQ0–DQ7. Two bus cycles are required for this operation: the first to enter the command code and a second to read the device-equivalent code. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}). Two identifier bytes are accessed by toggling A0. The manufacturer-equivalent code is obtained on DQ0–DQ7 with A0 at a logic low (V_{IL}). The device-equivalent code is obtained when A0 is set to a logic high (V_{IH}). Alternately, the manufacturer- and device-equivalent codes can be read by applying V_{ID} (nominally 12 V) to A9 and selecting the desired code by toggling A0 high or low. All other addresses are don't care (see Table 3, Table 4, and Table 5).

read status register

The status register is read by entering the command code 70h on DQ0–DQ7. Control terminals $\overline{E}$ and $\overline{G}$ must be at a logic low (V_{IL}) and $\overline{W}$ and $\overline{RP}$ must be at a logic high (V_{IH}). Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a given read cycle, status register contents are updated on the falling edge of $\overline{E}$ or $\overline{G}$, whichever occurs last within the cycle.

clear status register

The internal circuitry can set only the V_{PP} status (SB3), the program status (SB4), and the erase status (SB5) bits of the status register. The clear-status-register command (50h) allows the external microprocessor to clear these status bits and synchronize to internal operations. When the status bits are cleared, the device returns to the read array mode.

boot-block programming/erasing

Should changes to the boot block be required, $\overline{RP}$ must be set to V_{HH} (12 V) and V_{PP} to the programming voltage level (V_{PPH}). If an attempt is made to write, erase, or erase suspend the boot block without $\overline{RP}$ at V_{HH}, an error signal is generated on SB4 (program-status bit) or SB5 (erase-status bit).

A program-setup command can be aborted by writing FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing FFh or FFFFh during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic high, signifying termination of the nonprogram operation is terminated, all commands to the CSM become valid again.

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normal programming

There are two CSM commands for programming: program setup and alternate program setup (see Table 2 on page 7). After the desired command code is entered, the WSM takes over and correctly sequences the device to complete the program operation. During this time, the CSM responds only to status reads until the program operation has been completed, after which all commands to the CSM become valid again. Once a program command has been issued, the WSM cannot normally be interrupted until the program algorithm is completed (see Figure 4 and Figure 4). Taking $\overline{RP}$ to V_{IL} during programming aborts the program operation. During programming, V_{PP} must remain at V_{PPH}. Only 0s are written and compared during a program operation. If 1s are programmed, the memory cell contents do not change and no error occurs.

A program-setup command can be aborted by writing FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing all 1s during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic high, signifying the nonprogram operation is terminated, all commands to the CSM become valid again.

erase operations

There are two erase operations that can be performed by the TMS28F200BZx devices: block erase and erase suspend/erase resume. An erase operation must be used to initialize all bits in an array block to 1s. After block-erase confirm is issued, the CSM responds only to status reads or erase-suspend commands until the WSM completes its task.

block erasure

Block erasure inside the memory array sets all bits within the addressed block to logic 1s. Erasure is accomplished only by blocks; data at single address locations within the array cannot be individually erased. Any valid address within the parameter or main blocks acts as a block selector and allows that block to be erased. $\overline{RP}$ must be at V_{HH} for changing the data content of the boot block. Block erasure is initiated by a command sequence to the CSM: block-erase setup (20h) followed by block-erase confirm (D0h). A two-command erase sequence protects against accidental erasure of memory contents.

Erase setup and confirm commands are latched on the rising edge of $\overline{E}$ or $\overline{W}$, whichever occurs first. Block addresses are latched during the block-erase-confirm command on the rising edge of $\overline{E}$ or $\overline{W}$ (see Figure 5). When the block-erase-confirm command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally, verification is performed to assure that all bits are correctly erased. Monitoring of the erase operation is possible through the status register (see read status register).

erase suspend/erase resume

During the execution of an erase operation, the erase-suspend command (B0h) can be entered to direct the WSM to suspend the erase operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the read-array, read-status-register, and erase-resume commands. During the erase-suspend operation, array data should be read from a block other than the one being erased. To resume the erase operation, an erase-resume command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 5 and Figure 10).

automatic power-saving mode

Substantial power savings can be realized during periods when the array is not being read. During this time, the device switches to the automatic power-saving mode. When the device switches to this mode, I_{CC} is typically reduced from 40 mA to 1 mA (I_{OUT} = 0 mA). The low level of power is maintained until another read operation is initiated. In this mode, the I/O terminals retain the data from the last memory address read until a new address is read. This mode is entered automatically if no address or control pins toggle within a 200-ns time-out period. At least one transition on $\overline{E}$ must occur after power up to activate this mode.

reset/deep power-down mode

Very low levels of power consumption can be attained by using a special terminal, $\overline{RP}$, that disables internal device circuitry. When $\overline{RP}$ is at a CMOS logic low of 0.0 V ± 0.2 V, an I_{CC} value on the order of 0.2 µA (or 1 µW of power) is achievable. This is important in portable applications where extended battery life is of major concern.

A recovery time is required when exiting from deep power-down mode. For a read-array operation, a minimum of 300 ns is required before data is valid, and a minimum of 215 ns in deep power-down mode is required before data input to the CSM can be recognized. With $\overline{RP}$ at ground, the WSM is reset and the status register is cleared, effectively eliminating accidental programming to the array during system reset. After restoration of power, the device does not recognize any operation command until $\overline{RP}$ is returned to a V_{IH} or V_{HH} level.

Should $\overline{RP}$ become low during a program or erase operation, the device becomes nonfunctional (is in a power-down state) and data being written or erased is invalid or indeterminate, requiring that the operation be performed again after power restoration.

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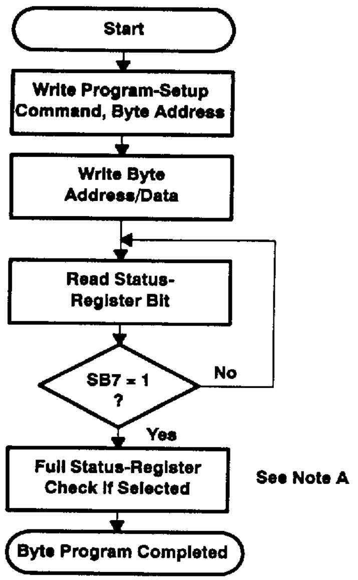
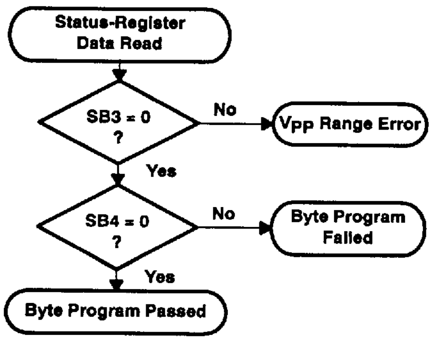


BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of byte to be programmed
Write	Write data	Data = Byte to be programmed Addr = Address of byte to be programmed
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy

Repeat for subsequent bytes.
Write FFh after the last byte-programming operation to reset the device to read-array mode.

FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Byte program error (see Note C)

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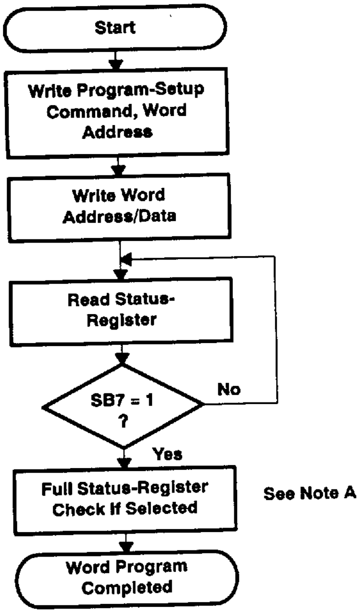
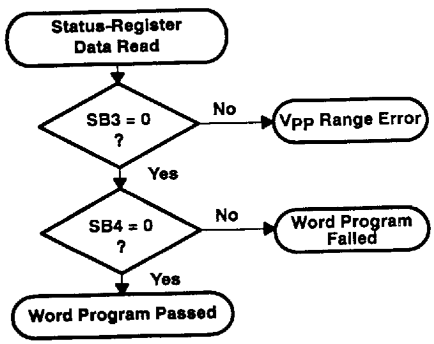
NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 3. Automated Byte-Programming Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of word to be programmed
Write	Write data	Data = Word to be programmed Addr = Address of word to be programmed
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word-programming operation to reset the device to read-array mode.		

FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect Vpp low (see Note B)
Standby		Check SB4 1 = Word program failed (see Note C)

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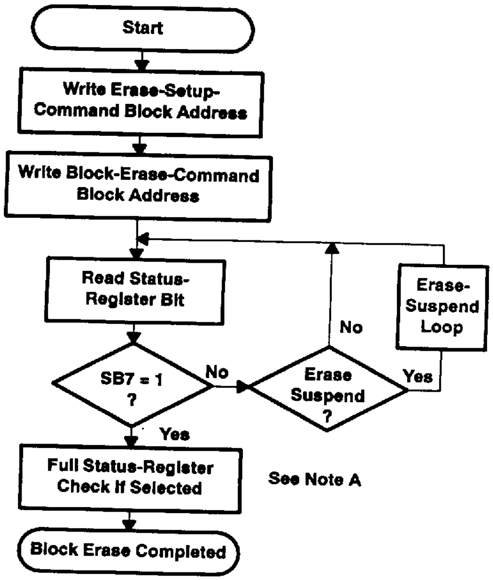
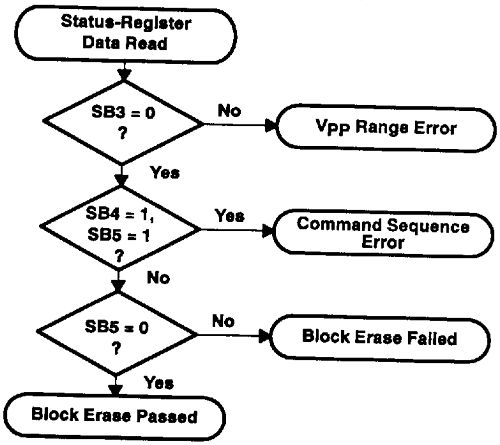
NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program / erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 4. Automated Word-Programming Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Write erase setup	Data = 20h Block Addr = Address within block to be erased
Write	Erase	Data = D0h Block Addr = Address within block to be erased
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last block-erase operation to reset the device to read-array mode.		

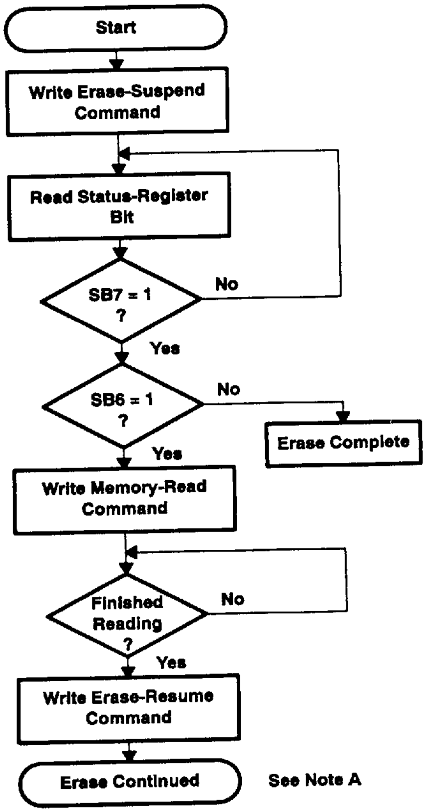
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 and SB5 1 = Block-erase command error
Standby		Check SB5 1 = Block-erase failed (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB5 is cleared only by the clear-status-register command in cases where multiple blocks are erased before full status is checked.

Figure 5. Automated Block-Erase Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase suspend	Data = B0h
Read		Status register data. Toggle $\overline{G}$ or $\overline{E}$ to update status register.
Standby		Check SB7 1 = Ready
Standby		Check SB6 1 = Suspended
Write	Read memory	Data = FFh
Read		Read data from block other than that being erased.
Write	Erase resume	Data = D0h

NOTE A: Refer to block-erase flowchart for complete erasure procedure.

Figure 6. Erase-Suspend/Resume Flowchart

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 2) .... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 2) .... – 0.6 V to 14 V
Input voltage range: All inputs except A9, $\overline{RP}$ .... – 0.6 V to V_{CC} + 1 V
$\overline{RP}$, A9 (see Note) .... – 0.6 V to 13.5 V
Output voltage range (see Note 4) .... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range, T_A, during read/erase/program: L suffix .... 0°C to 70°C
E suffix .... – 40°C to 85°C
Q suffix .... – 40°C to 125°C
Storage temperature range, T_{stg} .... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. All voltage values are with respect to V_{SS}.
3. The voltage on any input can undershoot to – 2 V for periods less than 20 ns.
4. The voltage on any output can overshoot to 7 V for periods less than 20 ns.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During write/read/erase/erase suspend	'28F200BZ-x-6	4.75	5	5.25	V
			All others	4.5	5	5.5	
V_{PP}	Supply voltage	During read only (V_{PPL})		0		6.5	V
		During write/erase/erase suspend (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.5		V_{CC} + 0.5	V
V_{IL}	Low-level dc input voltage		TTL	– 0.5		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	V
V_{LKO}	V_{CC} lock-out voltage from write/erase			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.5	12	13	V

word/byte-write and block-erase performance, T_A = 25°C, V_{PP} = 12 V (see Note 5)

PARAMETER	'28F200BZx-6			'28F200BZx-70			'28F200BZx-80			'28F200BZx-90			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Main-block erase time		2.2			2.2			2.2			2.2		s
Main-block byte-program time		3.2			3.2			3.2			3.2		s
Main-block word-program time		1.6			1.6			1.6			1.6		s
Parameter/boot-block erase time		0.32			0.32			0.32			0.32		s

NOTE 5: Excludes system-level overhead

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature using test conditions given in Table 6 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = – 2.5 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 5.8 mA		0.45	V
V_{ID}	A9 selection code voltage		11.5	13	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID}	V_{CC} = 5.5 V, V_I = 0 V to 5.5 V		±1	μA
I_{ID}	A9 selection code current	A9 = V_{ID}		500	μA
I_{RP}	$\overline{RP}$ boot-block unlock current			500	μA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}		±10	μA
I_{PPS}	V_{PP} standby current (standby)	$V_{PP} \le V_{CC}$		10	μA
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)	$\overline{RP}$ = V_{SS} ± 0.2 V		5	μA
I_{PP1}	V_{PP} supply current (read)	$V_{PP} > V_{CC}$		200	μA
I_{PP2}	V_{PP} supply current (active byte write)	V_{PP} = V_{PPH}, Programming in progress		30	mA
I_{PP3}	V_{PP} supply current (active word write)	V_{PP} = V_{PPH}, Programming in progress		40	mA
I_{PP4}	V_{PP} supply current (block erase)	V_{PP} = V_{PPH}, Block erase in progress		30	mA
I_{PP5}	V_{PP} supply current (erase suspend)	V_{PP} = V_{PPH}, Block erase suspended		200	μA
I_{CCS}	V_{CC} supply current (standby) – TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = $\overline{RP}$ = V_{IH}		1.5	mA
	V_{CC} supply current (standby) – CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = $\overline{RP}$ = V_{IH}		100	μA
I_{CCL}	V_{CC} supply current (reset/deep power-down mode) – 0°C to 70°C, – 40°C to 85°C	RP = V_{SS} ± 0.2 V		1.2	μA
	V_{CC} supply current (reset/deep power-down mode) – – 40°C to 125°C	RP = V_{SS} ± 0.2 V		8	μA
I_{CC1}	V_{CC} supply current (active read) – TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA		60	mA
	V_{CC} supply current (active read) – CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{SS} ± 0.2 V, f = 10 MHz, I_{OUT} = 0 mA		55	mA
I_{CC2}	V_{CC} supply current (active byte write) (see Notes 10 and 11)	V_{CC} = 5.5 V, Programming in progress		60	mA
I_{CC3}	V_{CC} supply current (active word write) (see Notes 10 and 11)	V_{CC} = 5.5 V, Programming in progress		65	mA
I_{CC4}	V_{CC} supply current (block erase) (see Notes 10 and 11)	V_{CC} = 5.5 V, Block erase in progress		30	mA
I_{CC5}	V_{CC} supply current (erase suspend) (see Notes 10 and 11)	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}, Block erase suspended		10	mA

NOTES: 6. Not 100% tested; characterization data available
7. All ac current values are RMS unless otherwise noted.

Table 6. AC Test Conditions

SPEED DESIGNATOR	I_{OL} (mA)	I_{OH} (mA)	V_Z† (V)	V_{OL} (V)	V_{OH} (V)	V_{IL} (V)	V_{IH} (V)	C_{LOAD} (pF)	t_f (ns)	t_r (ns)	TEMPERATURE
-6	5.8	– 2.5	1.5	1.5	1.5	0	3.0	30	<10	<10	0°C to 70°C
-70, -80, -90	5.8	– 2.5	1.5	0.8	2.0	0.45	2.4	100	<10	<10	– 40°C to 125°C

† V_Z is the measured value used to detect high impedance.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz, V_I = 0 V

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_i	Input capacitance			8	pF
C_o	Output capacitance	V_O = 0 V		12	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'28F200BZx-6		'28F200BZx-70		'28F200BZx-80		'28F200BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A16	t_{AVQV}		60		70		80		90	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ELQV}		60		70		80		90	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{GLQV}		30		35		40		45	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	60		70		80		90		ns
$t_{d(E)}$	Delay time, $\overline{E}$ low to low-impedance output	t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-impedance output	t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{E}$ to high-impedance output	t_{EHQZ}		20		25		30		35	ns
$t_{dis(G)}$	Disable time, $\overline{G}$ to high-impedance output	t_{GHQZ}		20		25		30		35	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A16, $\overline{E}$, or $\overline{G}$, whichever occurs first	t_{AXQX}	0		0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{E}$ low	t_{ELFL} t_{ELFH}		5		5		5		5	ns
$t_{d(RP)}$	Output delay time from $\overline{RP}$ high	t_{PHQV}		300		300		300		300	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in high-impedance state	t_{FLQV}		20		25		30		35	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ switching high	t_{FHQV}		60		70		80		90	ns

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

write/erase operations — $\overline{W}$-controlled writes

		ALT. SYMBOL	'28F200BZx-6		'28F200BZx-70		'28F200BZx-80		'28F200BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	60		70		80		90		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		7		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		0.4		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		0.4		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		0.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A16	t_{WHAX}	10		10		10		10		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	10		10		10		10		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status register bit	t_{QVPH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, A0–A16	t_{AVWH}	50		50		50		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	50		50		50		50		ns
$t_{su(E)}$	Setup time, $\overline{E}$ before write operation	t_{ELWL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{W}$ going high	t_{PHHWH}	100		100		100		100		ns
$t_{su(VPP)}$	Setup time, V_{PP} to $\overline{W}$ going high	t_{VPWH}	100		100		100		100		ns
$t_{w(W)}$	Pulse duration, $\overline{W}$ low	t_{WLWH}	50		50		50		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WLWL}	10		20		30		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{W}$ going low	t_{PHWL}	215		215		215		215		ns

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

write/erase operations — $\overline{E}$-controlled writes

		ALT. SYMBOL	'28F200BZx-6		'28F200BZx-70		'28F200BZx-80		'28F200BZx-90		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{E}$	t_{AVAV}	60		70		80		90		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation using $\overline{E}$	t_{EHQV1}	6		6		6		7		µs
$t_{c(E)ERB}$	Cycle time, erase operation using $\overline{E}$ (boot block)	t_{EHQV2}	0.3		0.3		0.3		0.4		s
$t_{c(E)ERP}$	Cycle time, erase operation using $\overline{E}$ (parameter block)	t_{EHQV3}	0.3		0.3		0.3		0.4		s
$t_{c(E)ERM}$	Cycle time, erase operation using $\overline{E}$ (main block)	t_{EHQV4}	0.6		0.6		0.6		0.7		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		100		100		100		100	ns
$t_{h(A)}$	Hold time, A0–A16	t_{EHAX}	10		10		10		10		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	10		10		10		10		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, A0–A16	t_{AVEH}	50		50		50		50		ns
$t_{su(D)}$	Setup time, DQ valid	t_{DVEH}	50		50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before $\overline{E}$	t_{WLEL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{E}$ going high	t_{PHHEH}	100		100		100		100		ns
$t_{su(VPP)}$	Setup time, V_{PP} to $\overline{E}$ going high	t_{VPEH}	100		100		100		100		ns
$t_{w(E)}$	Pulse duration, $\overline{E}$ low, write using $\overline{E}$	t_{ELEH}	50		50		50		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{E}$ high, write using $\overline{E}$	t_{EHEL}	10		20		30		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{E}$ going low	t_{PHEL}	215		215		215		215		ns

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PARAMETER MEASUREMENT INFORMATION

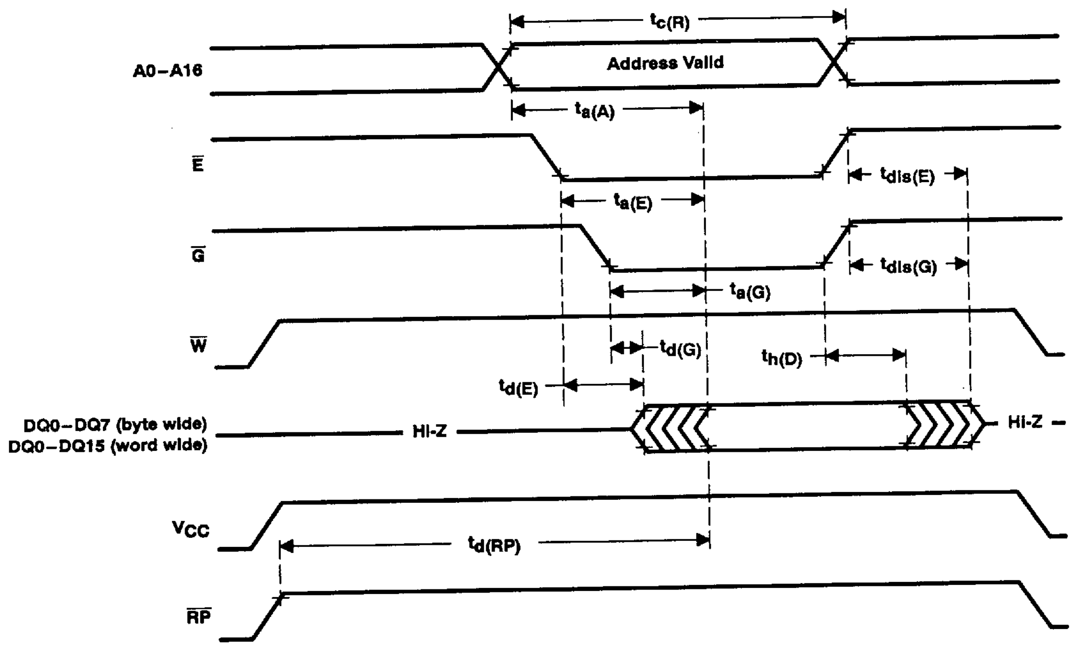

Figure 7. Read-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

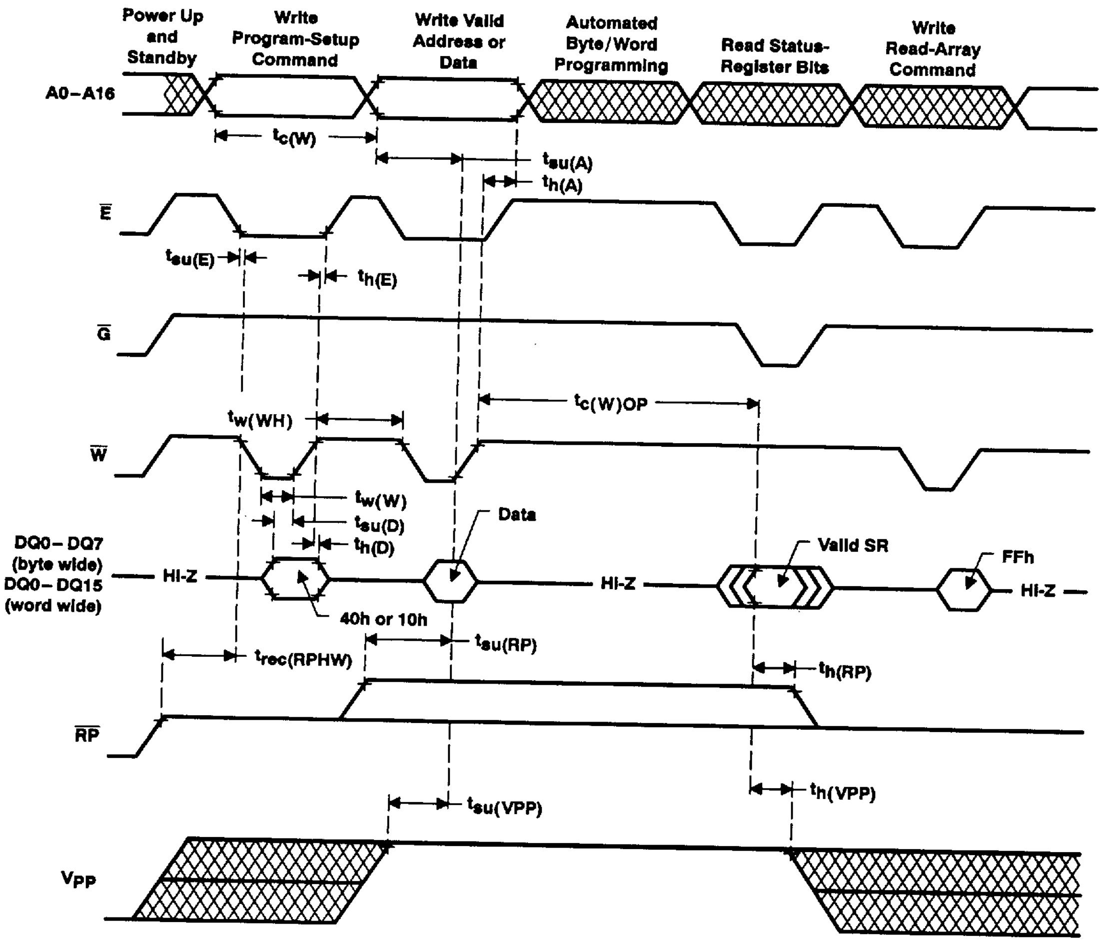

Figure 8. Write-Cycle Timing ($\overline{W}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

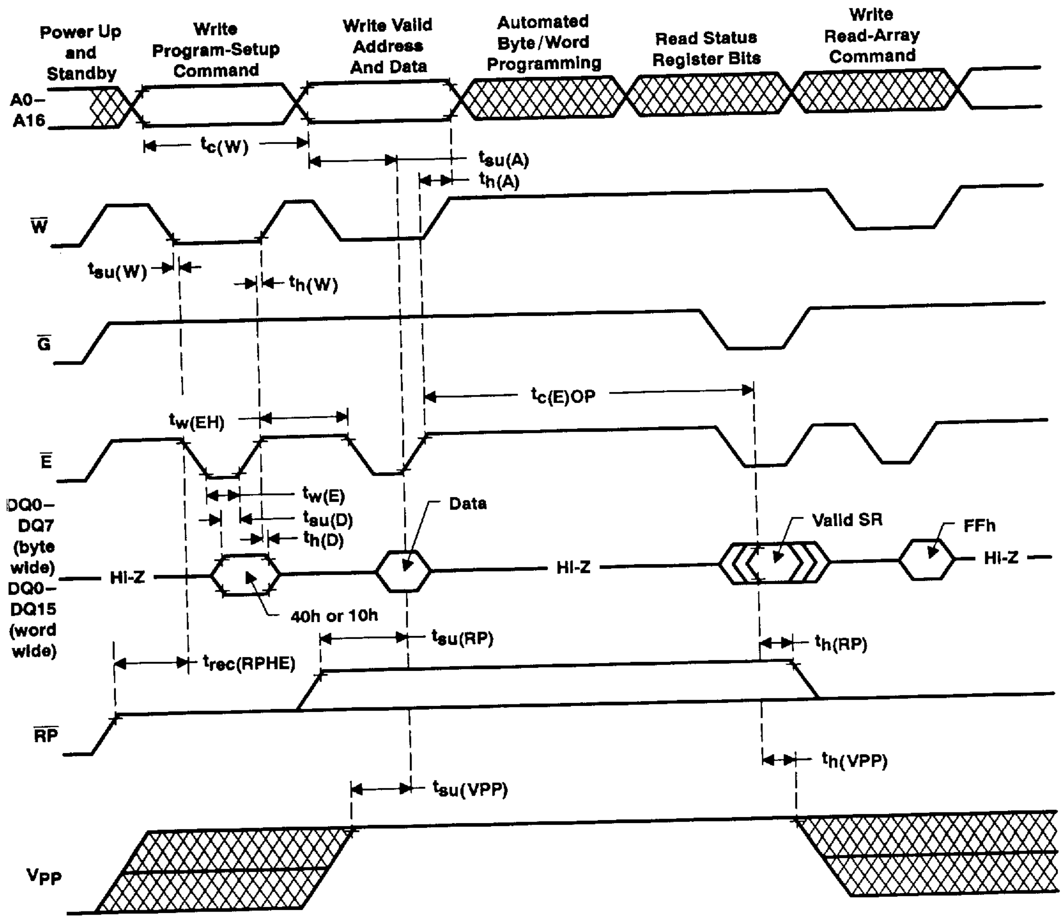

Figure 9. Write-Cycle Timing ($\overline{E}$-Controlled Write)

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PARAMETER MEASUREMENT INFORMATION

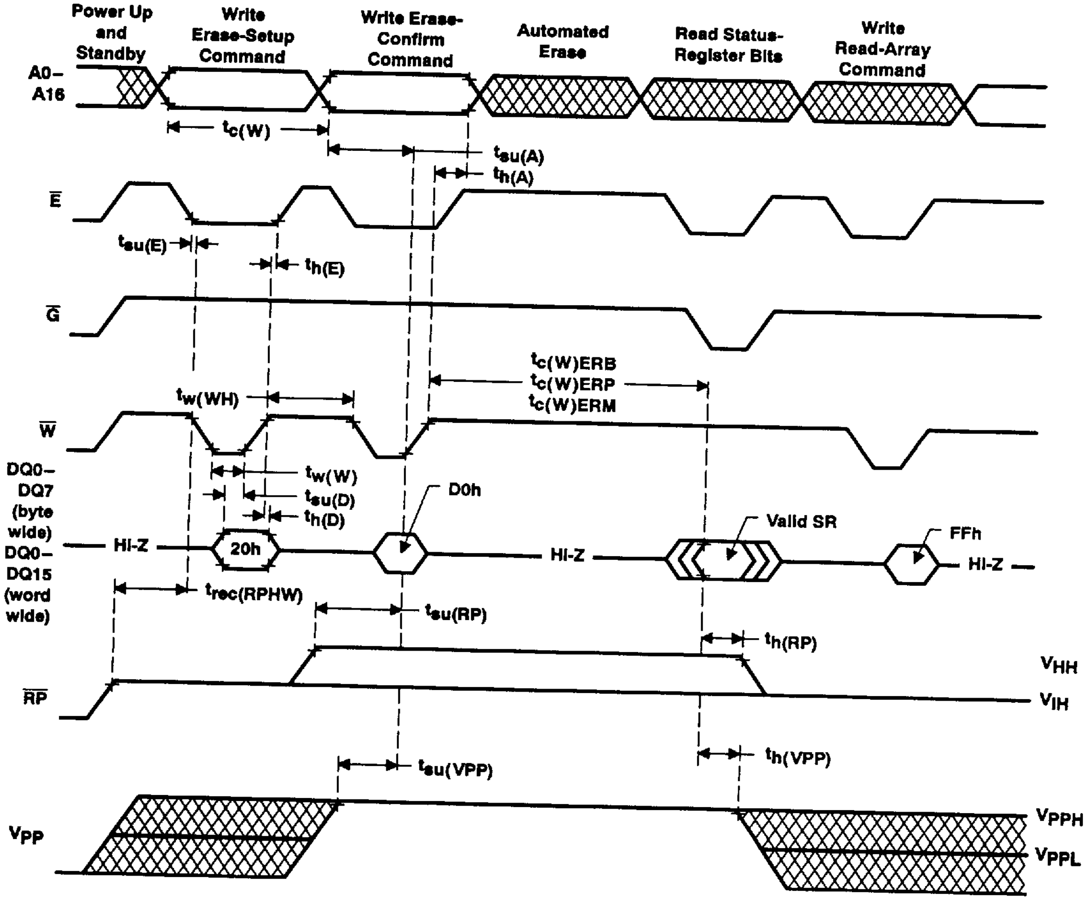

Figure 10. Erase-Cycle Timing (W-Controlled Write)

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PARAMETER MEASUREMENT INFORMATION

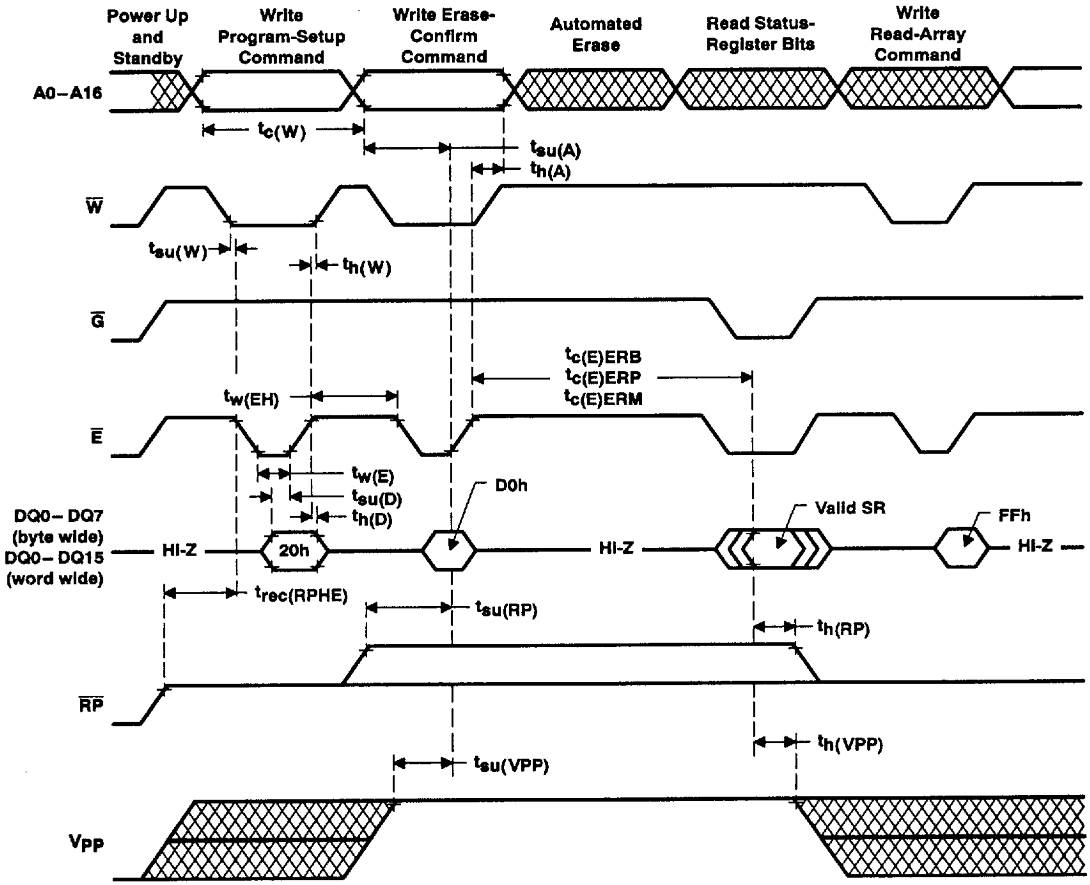

Figure 11. Erase-Cycle Timing (Ē-Controlled Write)

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PARAMETER MEASUREMENT INFORMATION

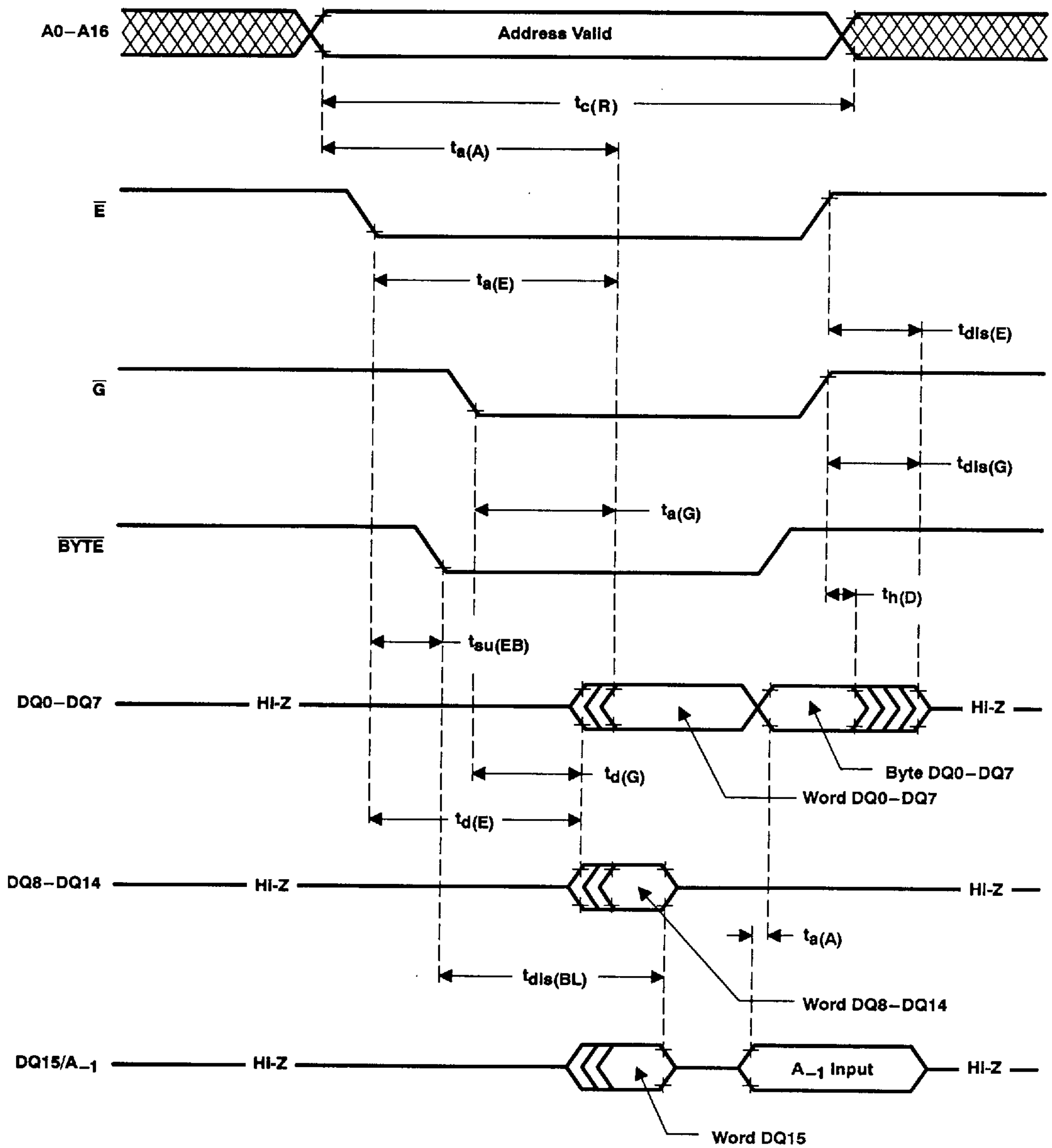

Figure 12. $\overline{\text{BYTE}}$ Timing, Changing From Word-Wide to Byte-Wide Mode

PARAMETER MEASUREMENT INFORMATION

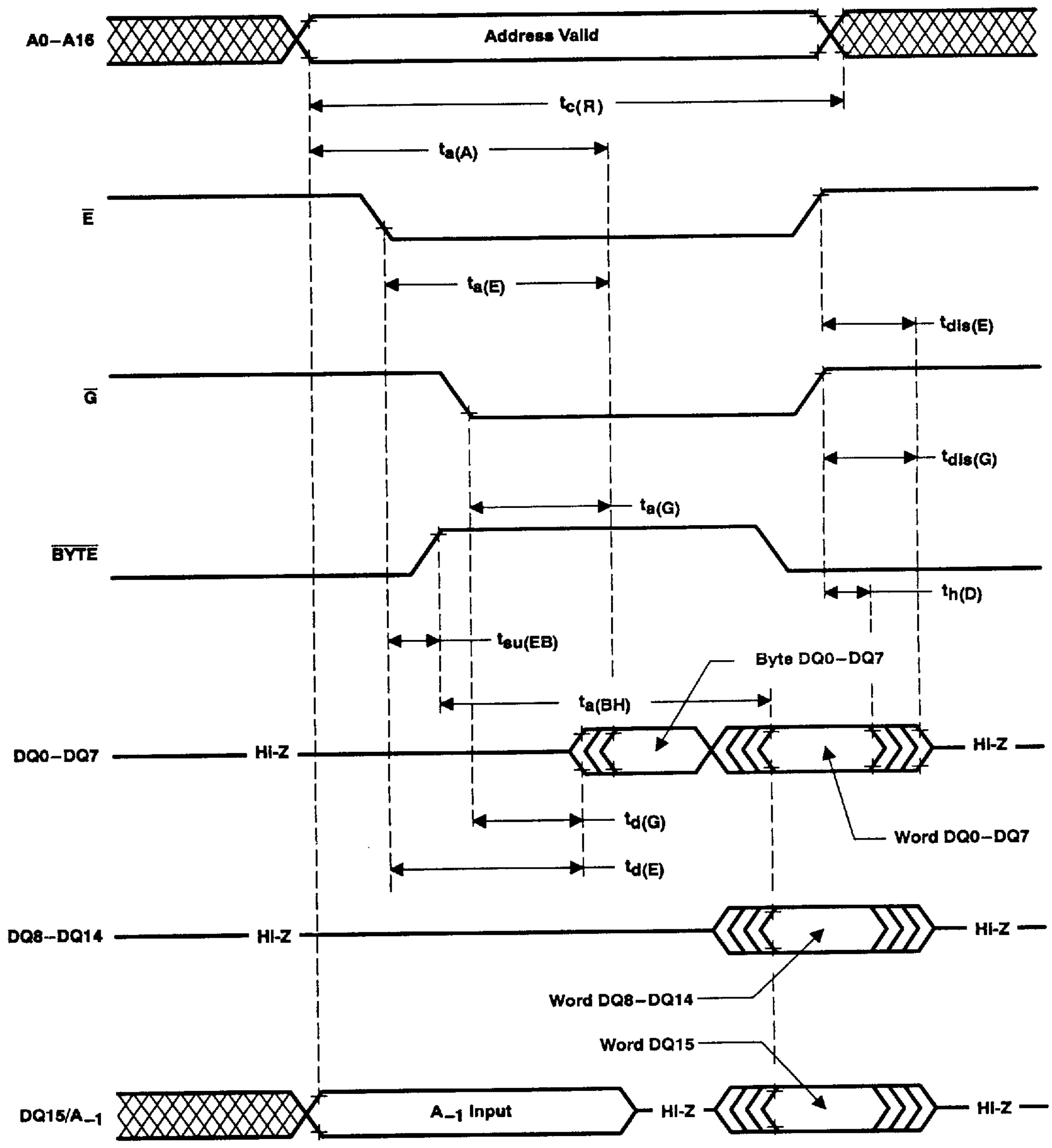

Figure 13. $\overline{\text{BYTE}}$ Timing, Changing From Byte-Wide to Word-Wide Mode

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