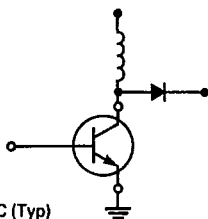


MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA
Designer's Data Sheet
SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 60 ns Inductive Fall Time — 75°C (Typ)
 - 70 ns Inductive Crossover Time — 75°C (Typ)
 - 500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +150°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents


MAXIMUM RATINGS

Rating	Symbol	2N6833	2N6834	Unit
Collector-Emitter Voltage*	V _{CEO(sus)}	450		Vdc
Collector-Emitter Voltage*	V _{CEV}	850		Vdc
Emitter Base Voltage*	V _{EB}	6.0		Vdc
Collector Current — Continuous*	I _C	5.0		Adc
— Peak (1)	I _{CM}	10		
Base Current — Continuous*	I _B	4.0		Adc
— Peak (1)	I _{BM}	8.0		
Total Power Dissipation @ T _C = 25°C*	P _D	80	125	Watts
@ T _C = 100°C*		32	71.5	
Derate above 25°C*		0.64	0.714	W/°C
Operating and Storage Junction Temperature Range*	T _J , T _{stg}	-65 to +150	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N6833	2N6834	Unit
Thermal Resistance, Junction to Case*	R _{θJC}	1.56	1.40	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds*	T _L		275	°C

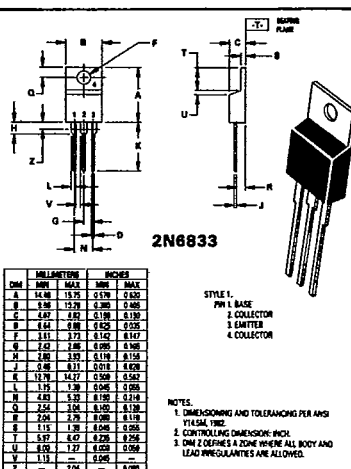
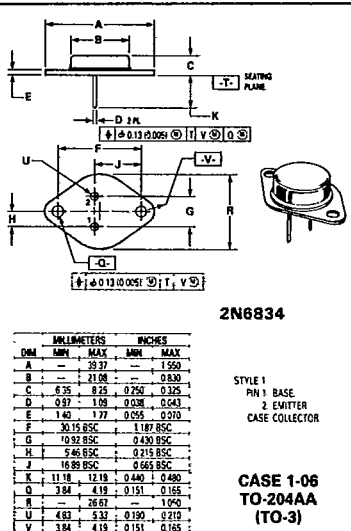
(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Indicate JEDEC Registered Data

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

2N6648
 See Page 3-195

2N6833
2N6834
5.0 AMPERE
NPN SILICON
POWER TRANSISTORS
450 VOLTS
80 and 125 WATTS

CASE 221A-04
TO-220AB

2N6834
STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR
CASE 1-06
TO-204AA
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450*	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25* 1.5*	mA _{dc}
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mA _{dc}
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0*	mA _{dc}

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figures 15* and 16*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 17			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 0.15\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5* 2.5*	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5* 1.5	Vdc
DC Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$) ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5* 5.0	— —	30* —	—

DYNAMIC CHARACTERISTICS (2)

Current Gain - Bandwidth Product ($V_{CE} = 10\text{ Vdc}$, $I_C = 0.25\text{ Adc}$, $f_{test} = 10\text{ MHz}$)	f_T	15*	—	75*	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	20*	—	200*	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	$(I_C = 3.0\text{ Adc},$ $V_{CC} = 250\text{ Vdc},$ $I_{B1} = 0.4\text{ Adc},$ $PW = 30\text{ }\mu\text{s},$ Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 0.8\text{ Adc},$ $R_{B2} = 8.0\text{ }\Omega)$	t_d	—	30	100*	ns
Rise Time			t_r	—	100	300*	
Storage Time			t_s	—	1000	3000*	
Fall Time			t_f	—	60	300*	
Storage Time			t_s	—	400	—	
Fall Time			t_f	—	130	—	
Inductive Load (Table 2)							
Storage Time	$(I_C = 3.0\text{ Adc},$ $I_{B1} = 0.4\text{ Adc},$ $V_{BE(off)} = 5.0\text{ Vdc},$ $V_{CE(pk)} = 400\text{ Vdc})$	$(T_C = 100^\circ\text{C})$	t_{sv}	—	500	1600*	ns
Fall Time			t_{fi}	—	100	200*	
Crossover Time			t_c	—	120	250*	
Storage Time		$(T_C = 150^\circ\text{C})$	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	

(1) Pulse Test $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.(2) $f_T = h_{FE} \cdot f_{test}$

*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

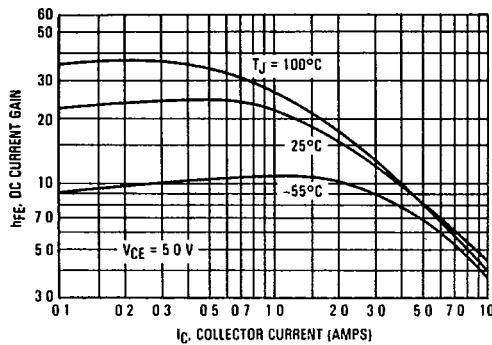


FIGURE 2 — COLLECTOR SATURATION REGION

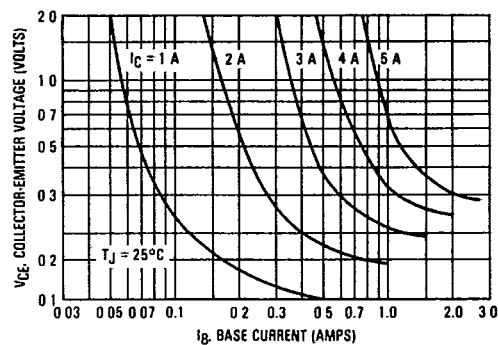


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

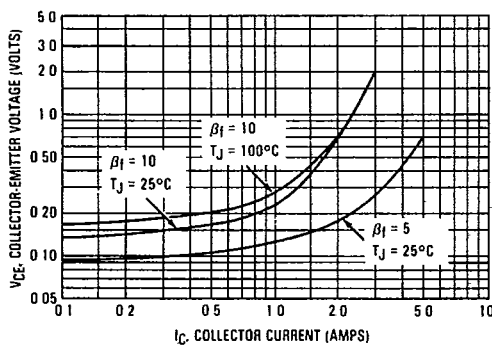


FIGURE 4 — BASE-EMITTER VOLTAGE

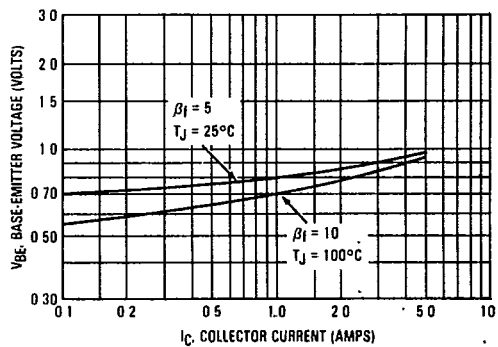


FIGURE 5 — COLLECTOR CUTOFF REGION

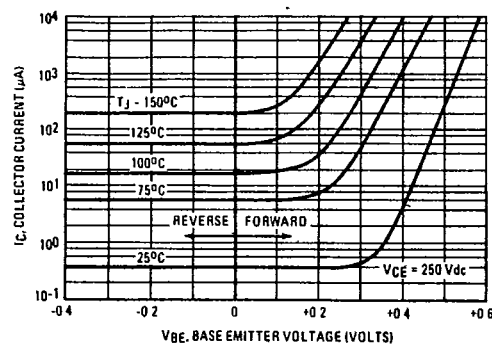
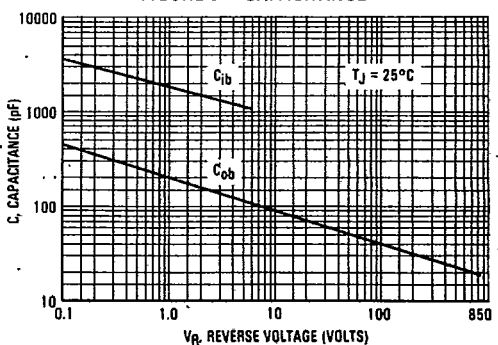


FIGURE 6 — CAPACITANCE



T-33-13

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

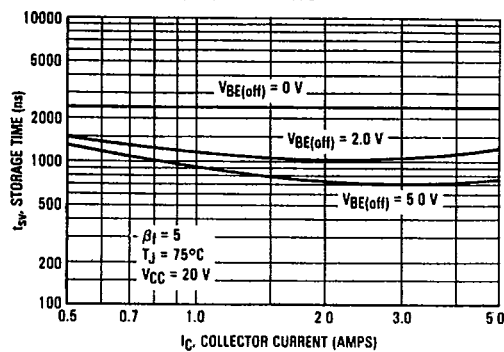


FIGURE 8 — STORAGE TIME

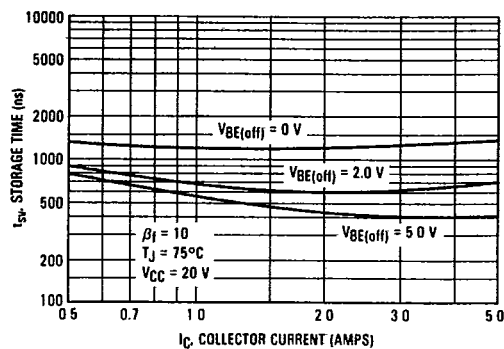


FIGURE 9 — COLLECTOR CURRENT FALL TIME

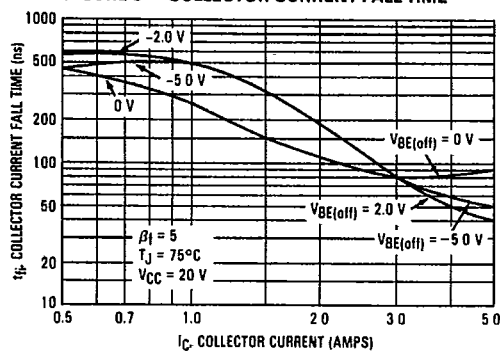


FIGURE 10 — COLLECTOR CURRENT FALL TIME

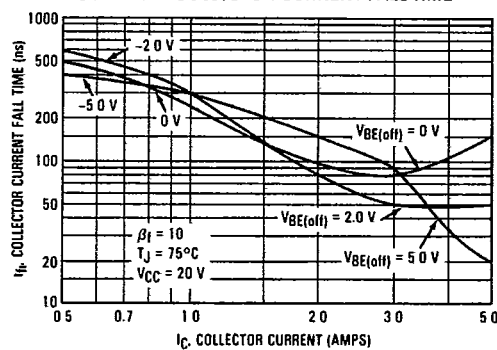


FIGURE 11 — CROSSOVER TIME

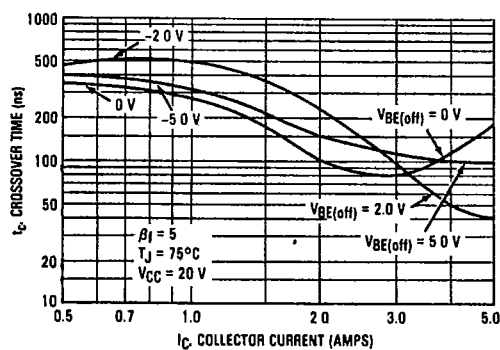
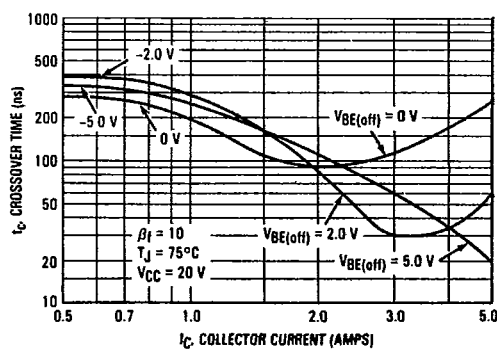


FIGURE 12 — CROSSOVER TIME



2N6833, 2N6834

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

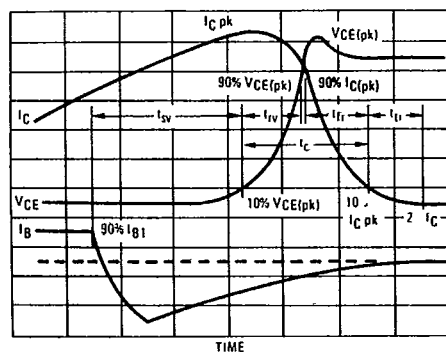
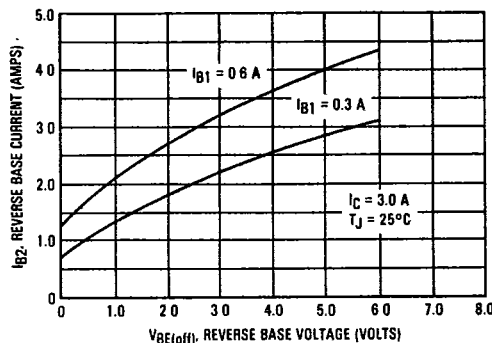
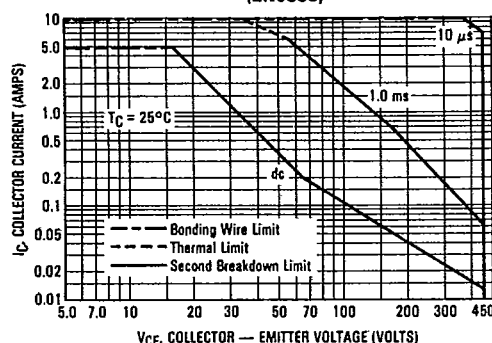
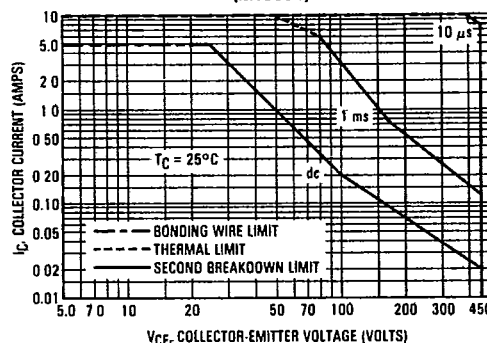


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS
SAFE OPERATING AREA
(2N6833)FIGURE 16 — MAXIMUM FORWARD BIAS
SAFE OPERATING AREA
(2N6834)

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 15 and 16 are based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 15 and 16 may be found at any case temperature by using the appropriate curve on Figures 18 or 19.

$T_{J(pk)}$ may be calculated from the data in Figures 20 or 21. At high case temperatures, thermal limitations will

reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

2N6833, 2N6834

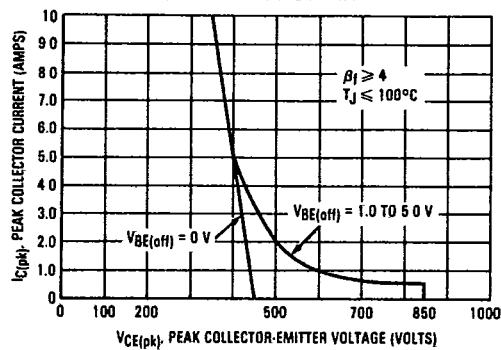
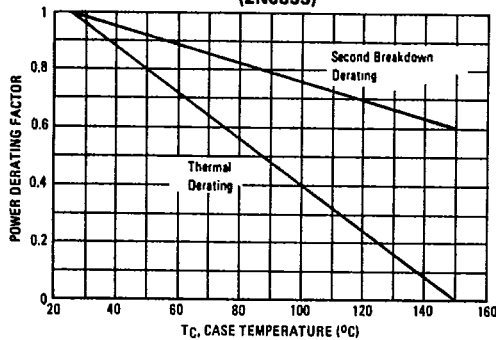
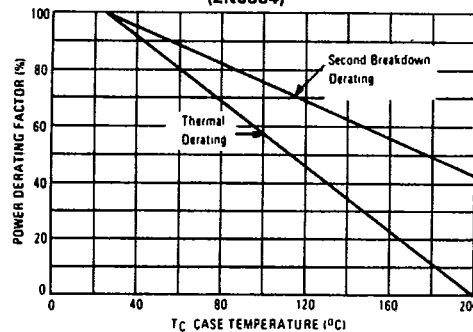
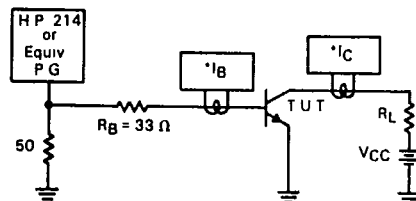
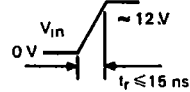
FIGURE 17 — MAXIMUM REVERSE BIAS
SAFE OPERATING AREAFIGURE 18 — POWER DERATING
(2N6833)FIGURE 19 — POWER DERATING
(2N6834)

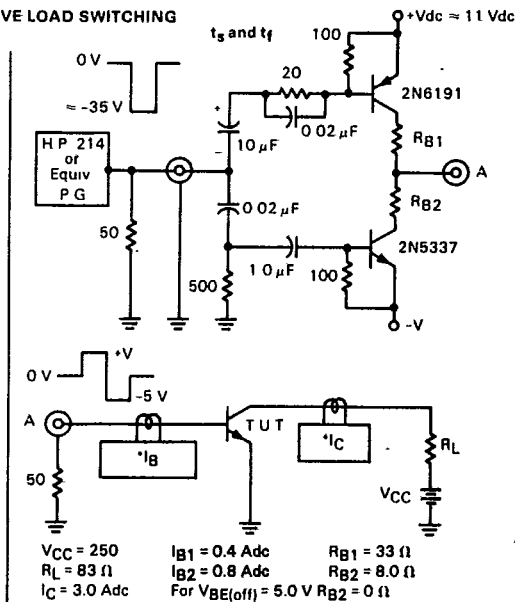
TABLE 1 — RESISTIVE LOAD SWITCHING

 t_d and t_r 

$V_{CC} = 250 \text{ Vdc}$
 $R_L = 83 \Omega$
 $I_C = 3.0 \text{ Adc}$
 $I_B = 0.4 \text{ Adc}$



*Tektronix
 P-6042 or
 Equivalent



*Note Adjust -V to obtain desired $V_{BE(off)}$ at Point A

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The figure consists of two parts: a circuit diagram and three waveforms.

Circuit Diagram:

- Top Section:** A push-pull output stage. The input is a square wave from an "HP 214 or Equiv PG" block. The signal passes through a 35V source and a 50Ω resistor to the base of a 2N6191 PNP transistor. The emitter is grounded. The collector is connected to a +V ≈ 11V supply through a 0.02μF capacitor and a 100Ω resistor. A 20Ω resistor is connected between the base and collector. The base is also biased through a 10μF capacitor and a 0.02μF capacitor to a 10μF capacitor, which is connected to a 500Ω resistor to ground. The collector is connected to a load resistor RB1, which is in series with a 2N5337 NPN transistor. The emitter of the 2N5337 is connected to a -V supply through a 100Ω resistor. The collector of the 2N5337 is connected to a load resistor RB2, which is in series with a 10μF capacitor to ground. The output is measured across RB2 with an ammeter A.
- Bottom Section:** An inductive switching circuit. The input is a square wave from an "HP 214 or Equiv PG" block. The signal passes through a 35V source and a 50Ω resistor to the base of a 2N6191 PNP transistor. The emitter is grounded. The collector is connected to a +V ≈ 11V supply through a 0.02μF capacitor and a 100Ω resistor. A 20Ω resistor is connected between the base and collector. The base is also biased through a 10μF capacitor and a 0.02μF capacitor to a 10μF capacitor, which is connected to a 500Ω resistor to ground. The collector is connected to a load resistor RB1, which is in series with a 2N5337 NPN transistor. The emitter of the 2N5337 is connected to a -V supply through a 100Ω resistor. The collector of the 2N5337 is connected to a load resistor RB2, which is in series with a 10μF capacitor to ground. The output is measured across RB2 with an ammeter A.

Waveforms:

- Top:** A square wave input signal with amplitude V and period T1.
- Middle:** A plot of collector current IC(pk) and collector-emitter voltage VCE(pk) versus time. IC(pk) is a square wave, and VCE(pk) is a square wave with a sharp transition during the switching event.
- Bottom:** A plot of base current IB1 and base current IB2 versus time. IB1 is a square wave, and IB2 is a square wave with a sharp transition during the switching event.

Component Values:

- HP 214 or Equiv PG
- 35V
- 50
- 0.02μF
- 100
- 20
- 10μF
- 0.02μF
- 10μF
- 500
- 100
- +V ≈ 11V
- 2N6191
- RB1
- A
- RB2
- 2N5337
- V
- T1
- V
- 0V
- V
- A
- 50
- IC
- VCE
- IC(pk)
- VCE(pk)
- IB1
- IB2
- MR856
- Vclamp
- VCC
- L
- UT

Inductive Switching

- L = 200 μH
- RB2 = 0
- VCC = 20 Volts
- RB1 selected for desired IB1

RBSOA

- L = 200 μH
- RB2 = 0
- VCC = 20 Volts
- RB1 selected for desired IB1

Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

t_{sv}

$I_C(pk) = 3.0 \text{ Amps}$
 $I_{B1} = 0.4 \text{ Amp}$
 $V_{BE(off)} = 5.0 \text{ Volts}$
 $V_{CE(pk)} = 400 \text{ Volts}$
 $T_C = 25^\circ\text{C}$
 Time Base = 20 ns/cm

t_{fi, t_c}

$I_C(pk) = 3.0 \text{ Amps}$
 $I_{B1} = 0.4 \text{ Amp}$
 $V_{BE(off)} = 5.0 \text{ Volts}$
 $V_{CE(pk)} = 400 \text{ Volts}$
 $T_C = 25^\circ\text{C}$
 Time Base = 20 ns/cm

THERMAL RESPONSE

FIGURE 20 — 2N6833

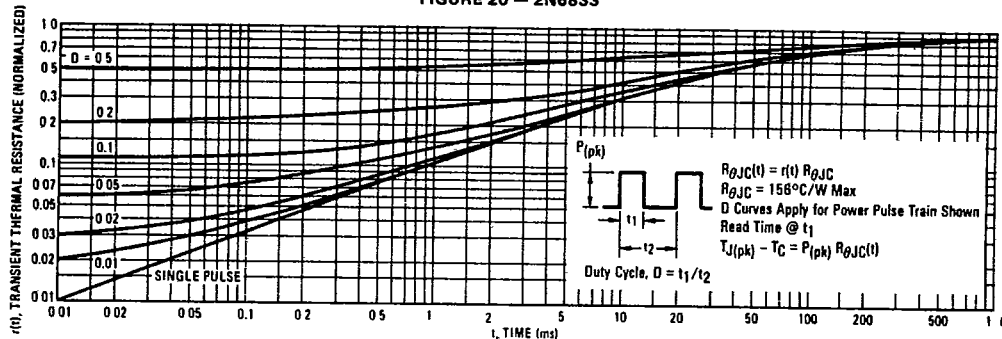


FIGURE 21 — 2N6834

