Jaguar 486SX/486DX/386DX Chipset Specifications

Process technology used	1.0μ CMOS
CPUs supported	Intel 80486, 80486SX AMD Am386DX Am486DX Cyrix 486DLC
CPU speed supported	16/20/25/33/40/50 MHz
Coprocessor supported in 386 system (No external PALS required)	Intel 80387/ Cyrix/IIT/ULSI/ WEITEK/3167
Coprocessors supported in 486 system (No external PALS required)	WEITEK 4167
AT clock generation	Async/Sync
Programmable AT bus clock	Yes
Hardware/Software turbo switching	Yes
Page Mode DRAM control	Yes
DRAM type supported	256K/1M/4M
Max physical memory	64MB
Mixing DRAMS	Yes
Hidden refresh	Yes
Shadow RAM range maximum size/block size	256 KB/64KB
Supported Local Bus	Yes
PQFP package	184
22cm x 22cm half baby AT board	Yes

Programmable wait states	Yes
On chip cache controller	Yes
Support 8kx8 and 8kx9 Tag RAM	Yes
Cache update scheme	Write back
Cache organization	Direct mapped
Data cache size	32KB-512KB
Non-cacheable support	Yes
Each non-cacheable region size	512KB-32MB
Zero wait state cache read hit	Yes
Zero wait state cache write hit	Yes
DRAM Burst mode support	Yes
External TTL component	12 ~ 15
SRAM Burst mode support 2-1-1-1, 2-2-2-2, 3-1-1-1, 3-2-2-2	Yes
SRAM speed required @ 50MHz	20ns
SRAM speed required @ 40MHz	20ns
SRAM speed required @ 33MHz	20ns
SRAM speed required @ 25MHz	35ns
Fast gate A20	Yes
Fast reset	Yes

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