Integrated Device Technology, Inc.

256K x 8 BiCMOS/CMOS STATIC RAM MODULE

IDT7M4068
IDT7MB4068

T-46-23-14

FEATURES:

- High density 2 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 256K x 8 static RAMs
- Fast access time: 10ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 250µA (max.)
  - — Data Retention: 150µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 32-pin, 600 mil ceramic or FR-4 DIP (Dual In-line Package) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

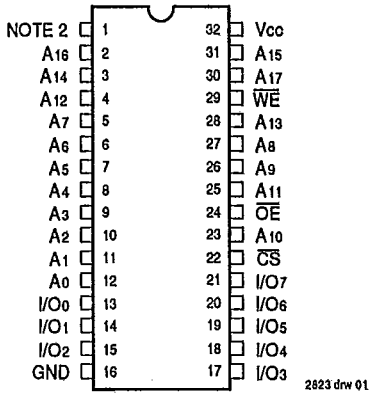
DESCRIPTION:

The IDT7M4068/7MB4068 is a 2 megabit (256K x 8) static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using two 1 Megabit static RAMs and a decoder. The IDT7MB4068 is available with access times as fast as 10ns. For low power applications, the IDT7M4068 version offers a data retention current of 150µA and a standby current of 250µA.

The IDT7M4068 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 2 megabits into the JEDEC DIP footprint. The IDT7MB4068 likewise is packaged in a 32-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7M4068 and 7MB4068 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

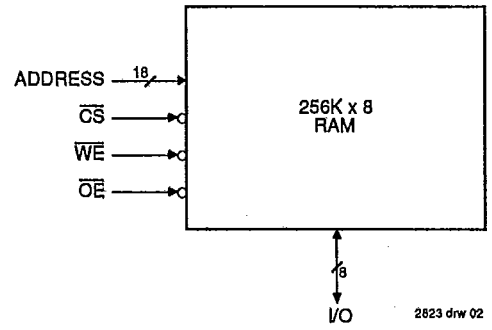
PIN CONFIGURATION(1)



DIP
TOP VIEW

NOTES:
1. For proper operation of the 7M4068LxxN module, Pin 1 must be connected to GND. For the 7MB4068xxP module, Pin 1 in a no connect.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2823 tbl 01

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2823 tbl 02

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	25	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	25	pF

NOTE: 2823 tbl 03
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	−10 to +85	°C
TSTG	Storage Temperature	−55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2823 tbl 05
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2823 tbl 04
1. VIL = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2823 tbl 06

DC ELECTRICAL CHARACTERISTICS
(VCC = 5V ± 10%, TA = 0°C to +70°C)

			7M4068LxxN		7MB4068SxxP				
					25 - 55ns		10 - 20ns[3]		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Unit
|ILI|	Input Leakage	VCC = Max., VIN = GND to VCC	—	2	—	10	—	10	µA
|ILO|	Output Leakage	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	2	—	10	—	10	µA
VOL	Output Low Voltage	VCC = Min., IOL = 2mA[1], IOL = 8mA[2]	—	0.4	—	0.4	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA[1], IOH = -4mA[2]	2.4	—	2.4	—	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ ≤ VIL; f = fMAX, Outputs Open	—	110	—	300	—	400	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ VIH, VCC = Max., f = fMAX, Outputs Open	—	6	—	120	—	120	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ VCC - 0.2V, VIN ≥ VCC - 0.2V or ≤ 0.2V	—	0.25	—	20	—	80	mA

NOTES: 2823 tbl 07
1. For 7M4068LxxN version only.
2. For 7MB4068SxxP, 7MB4068BxxP versions only.
3. Preliminary specifications only.

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DATA RETENTION CHARACTERISTICS[3]

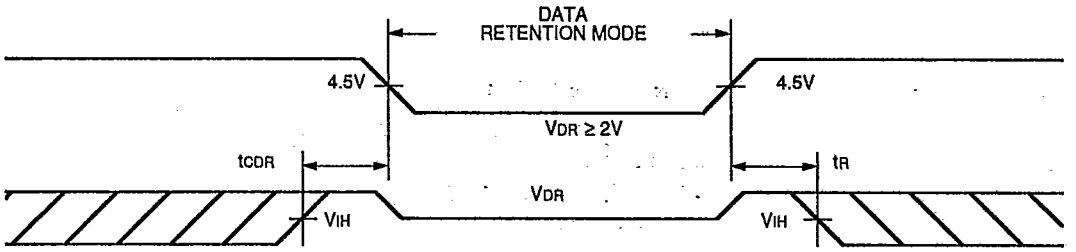
(TA = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. Vcc @ 2.0V	Unit
V_{DR}	Vcc for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	150	µA
t_{CDR}[2]	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R[2]	Operation Recovery Time	$V_{IN} \geq 0.2V$	t_{RC}[1]	—	ns

2823 tbl 08

NOTES:
1. t_{RC} = Read Cycle Time.
2. This parameter is guaranteed by design, but not tested.
3. For 7M4068LxxN version only.

DATA RETENTION WAVEFORM

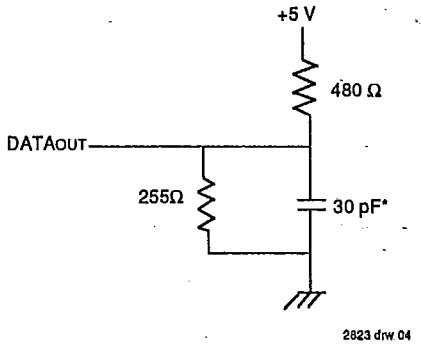


2823 drw 03

AC TEST CONDITIONS

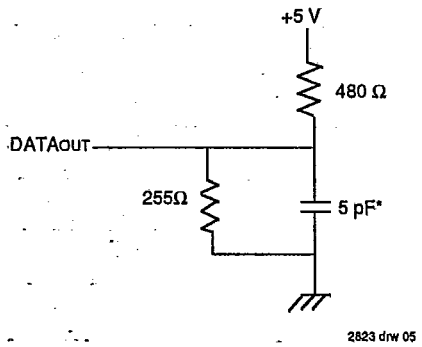
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2823 tbl 09



2823 drw 04

Figure 1. Output Load



2823 drw 05

Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

* Including scope and jig

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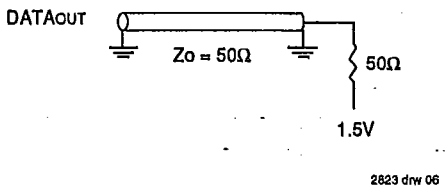

Figure 3. Alternate Output Load

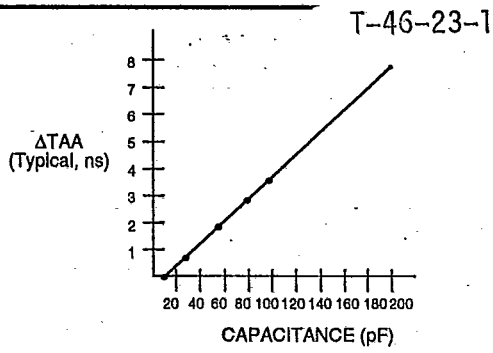

Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	7MB4068SxxP								Unit
		-10[2]		-12[2]		-15[2]		-17[2]		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	17	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	17	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	17	ns
tOE	Output Enable to Output Valid	—	6	—	6	—	7	—	8	ns
tOHZ[1]	Output Disable to Output in High Z	—	6	—	6	—	7	—	7	ns
tOLZ[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
tCLZ[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	5	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	10	—	10	—	12	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	17	—	ns
tWP	Write Pulse Width	10	—	10	—	12	—	14	—	ns
tAS	Address Set-up Time	3	—	3	—	3	—	0	—	ns
tAW	Address Valid to End of Write	10	—	12	—	15	—	14	—	ns
tCW	Chip Select to End of Write	10	—	12	—	15	—	14	—	ns
tDW	Data to Write Time Overlap	6	—	8	—	10	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	8	—	8	—	10	—	10	ns
tOW[1]	Output Active from End of Write	2	—	2	—	2	—	0	—	ns

2823 tbl 10

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB4068SxxP								Unit
		-20		-25		-30		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	15	—	15	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	10	—	12	—	12	—	15	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	10	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	12	—	25	—	30	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	15	—	17	—	20	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	16	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	17	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2823 tbl 11

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AC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	7MB4068SxxP				7M4068LxxN						Unit
		-45		-55		-60[2]		-65[2]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
tAA	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
tACS	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
tOE	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
tOHZ[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
tOLZ[1]	Output Enable to Output in Low Z	0	—	0	—	3	—	5	—	0	—	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	20	—	25	—	25	—	25	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
tWC	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
tWP	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tAW	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
tCW	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
tDW	Data to Write Time Overlap	25	—	25	—	30	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	25	—	25	—	25	—	25	—	30	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

2623 tbl 12

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

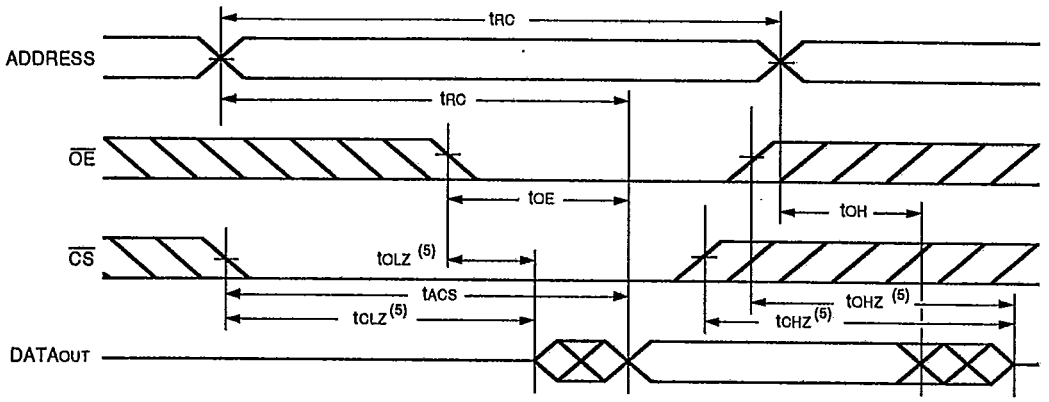
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7M4068LxxN						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

2823 tbl 13

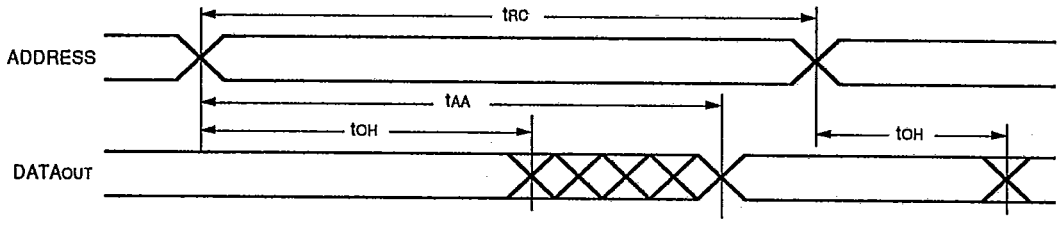
NOTE:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



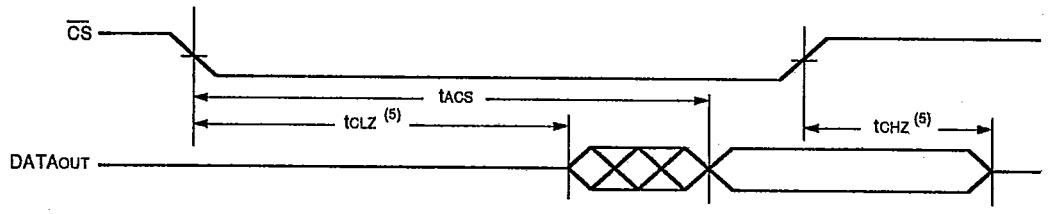
2823 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2823 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

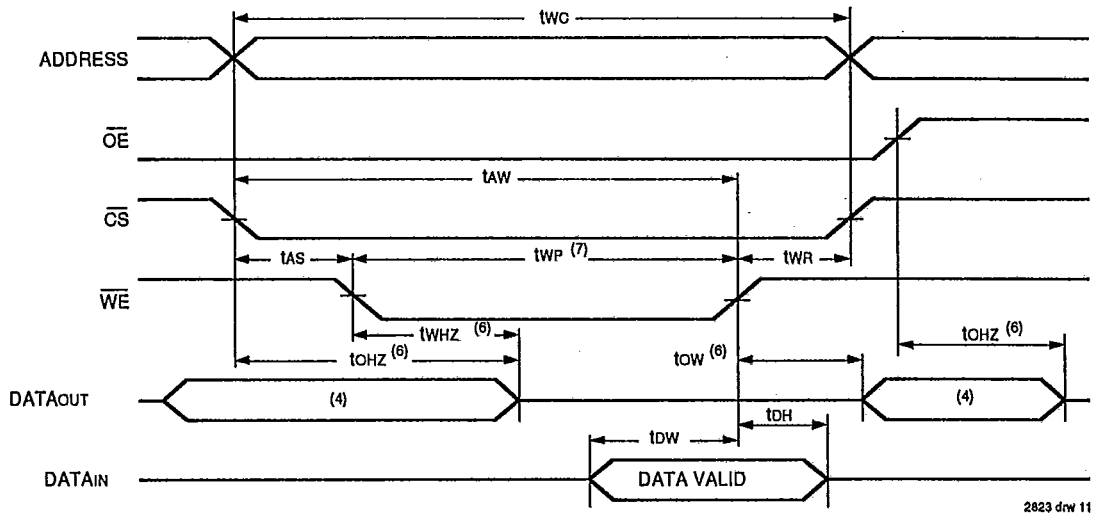


2823 drw 10

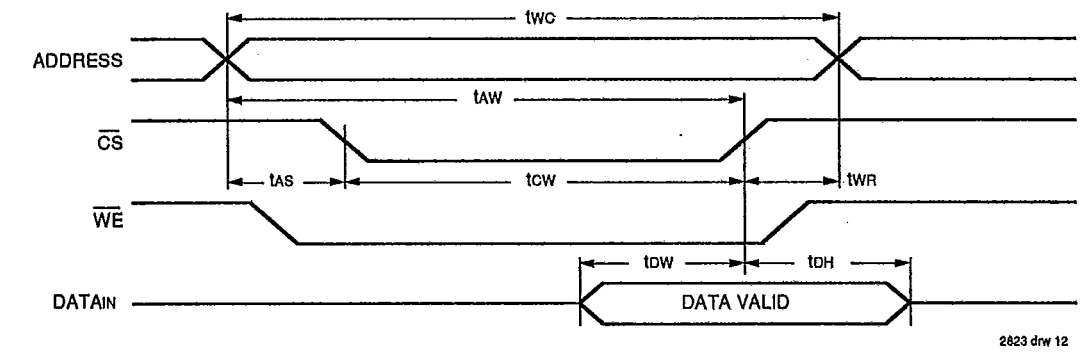
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

T-46-23-14



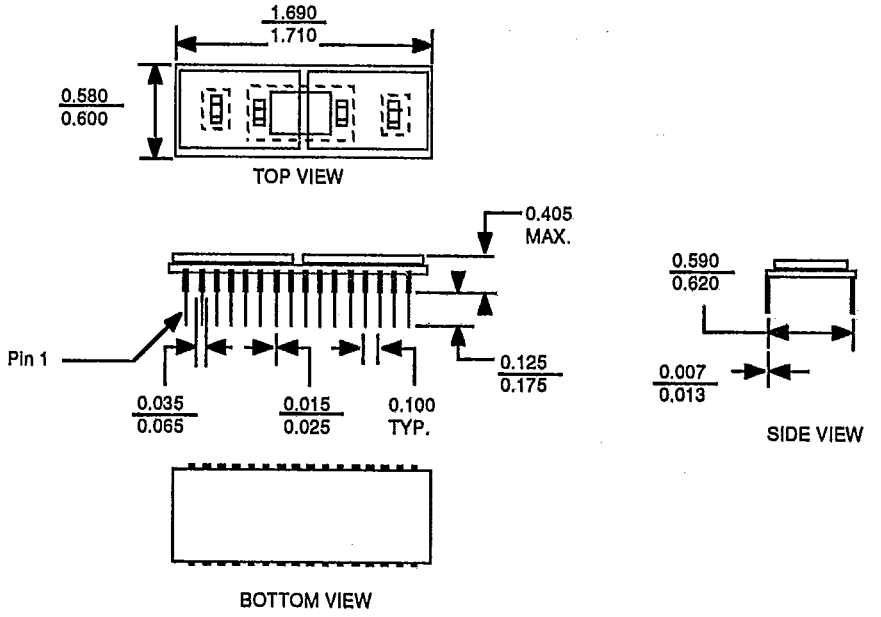
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tOW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tOW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS

7M4068LxxN



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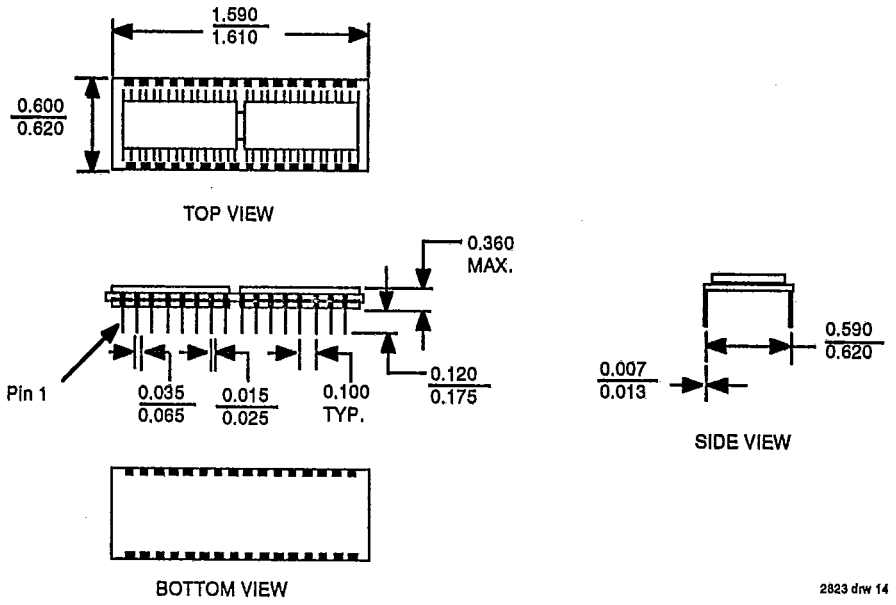
7MB4068SxxP



2823 drw 14