




32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

General Description

The MAX5732–MAX5735 are 32-channel, 16-bit, voltage-output, digital-to-analog converters (DACs). All devices accept a 3V external reference input. The devices include an internal offset DAC that allows all the outputs to be offset and a ground-sensing function, allowing output voltages to be referenced to a remote ground.

A 33MHz SPI™-/QSPI™-/MICROWIRE™- and digital signal processor (DSP)-compatible serial interface controls the MAX5732–MAX5735. Each DAC has a double-buffered input structure that helps minimize the digital noise feedthrough from the digital inputs to the outputs, and allows for synchronous or asynchronous updating of the outputs. The MAX5732–MAX5735 also provide a DOUT that allows for read-back or daisy chaining multiple devices. The devices provide separate power inputs for the analog and digital sections and provide separate power inputs for the output buffer amplifiers. The MAX5732–MAX5735 include proprietary deglitch circuits to prevent output glitches at power-up and eliminate the need for power sequencing. The devices provide a software-shutdown mode to allow efficient power management. The MAX5732–MAX5735 consume 50µA of supply current in shutdown.

The MAX5732–MAX5735 provide buffered outputs that can drive 10kΩ in parallel with 100pF. The MAX5732 has a 0 to +5V output range; the MAX5733 has a 0 to +10V range; the MAX5734 has a -2.5V to +7.5V range; the MAX5735 has a -5V to +5V range. The MAX5732–MAX5735 are available in a 56-pin, 8mm x 8mm, thin QFN package in both the commercial (0°C to +70°C) and extended (-40°C to +85°C) temperature ranges.

Applications

- Automatic Test Systems
- Optical Router Controls
- Industrial Process Controls
- Arbitrary Function Generators
- Avionics Equipment
- Digital Offset/Gain Adjustment

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

Pin Configuration and Selector Guide appear at end of data sheet.



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Features

- ◆ Guaranteed Monotonic to 16 Bits
- ◆ 32 Individual DACs in an 8mm x 8mm, 56-Pin, Thin QFN Package
- ◆ Four Output Voltage Ranges
 - 0 to +5V
 - 0 to +10V
 - 2.5V to +7.5V
 - 5V to +5V
- ◆ Buffered Voltage Outputs Capable of Driving 10kΩ || 100pF
- ◆ Glitch-Free Power-Up
- ◆ SPI-/QSPI-/MICROWIRE-/DSP-Compatible 33MHz Serial Interface

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5732ACTN*	0°C to +70°C	56 Thin QFN-EP**
MAX5732BCTN	0°C to +70°C	56 Thin QFN-EP**
MAX5732AETN*	-40°C to +85°C	56 Thin QFN-EP**
MAX5732BETN	-40°C to +85°C	56 Thin QFN-EP**
MAX5733ACTN*	0°C to +70°C	56 Thin QFN-EP**
MAX5733BCTN	0°C to +70°C	56 Thin QFN-EP**
MAX5733AETN*	-40°C to +85°C	56 Thin QFN-EP**
MAX5733BETN	-40°C to +85°C	56 Thin QFN-EP**
MAX5734ACTN*	0°C to +70°C	56 Thin QFN-EP**
MAX5734BCTN	0°C to +70°C	56 Thin QFN-EP**
MAX5734AETN*	-40°C to +85°C	56 Thin QFN-EP**
MAX5734BETN	-40°C to +85°C	56 Thin QFN-EP**
MAX5735ACTN*	0°C to +70°C	56 Thin QFN-EP**
MAX5735BCTN	0°C to +70°C	56 Thin QFN-EP**
MAX5735AETN*	-40°C to +85°C	56 Thin QFN-EP**
MAX5735BETN	-40°C to +85°C	56 Thin QFN-EP**

*Future product—contact factory for availability. Specifications are preliminary.

**EP = Exposed paddle (internally connected to Vss).

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ABSOLUTE MAXIMUM RATINGS

AVCC to VSS, AGND, DGND, REFGND-0.3V to +12V
 VSS to AGND, DGND-6V to +0.3V
 AVDD, DVDD to AGND, DGND, REFGND-0.3V to +6V
 AGND to DGND-0.3V to +0.3V
 REF to AGND, DGND,
 REFGND-0.3V to the lower of (AVDD + 0.3V) and +6V
 REFGND to AGND-0.3V to +0.3V
 Digital Inputs to AGND, DGND,
 REFGND-0.3V to the lower of (DVDD + 0.3V) and +6V
 DOUT to DGND-0.3V to the lower of (DVDD + 0.3V) and +6V
 OUT_ to VSS-0.3V to the lower of (AVCC + 0.3V) and +12V

GS to AGND-1V to +1V
 Maximum Current into REF±10mA
 Maximum Current into Any Pin±50mA
 Continuous Power Dissipation (TA = +70°C)
 Thin QFN (derate 31.3mW/°C above +70°C)2.5W
 Operating Temperature Ranges
 MAX573_CTN0°C to +70°C
 MAX573_ETN-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5732 (0 to +5V Output Voltage Range)

(AVCC = +5.25V to +5.5V (Note 1), AVDD = +5V ±5%, DVDD = +2.7V to AVDD, VSS = AGND = DGND = REFGND = GS = 0, VREF = +3.0V, RL = ∞, CL = 50pF referenced to ground, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		16			Bits
Integral Nonlinearity	INL	MAX5732B (Note 2)		±8	±16	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 3)			±1	LSB
Zero-Scale Error	VOS	VSS = -0.5V, AVCC = +5.25V (Note 4)		±8	±40	mV
Full-Scale Error		(Note 4)		±8	±50	mV
Gain Error				±0.1	±0.5	%FSR
Gain Temperature Coefficient				20	40	ppm FSR/°C
DC Crosstalk		VSS = -0.5V, AVCC = +5V (Note 5)		50	250	μV
DYNAMIC CHARACTERISTICS						
Output-Voltage Settling Time		Full-scale change to ±0.5 LSB		20		μs
Voltage-Output Slew Rate				1		V/μs
Digital Feedthrough		(Note 6)		5		nV-s
Digital Crosstalk		(Note 7)		5		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition		120		nV-s
DAC-to-DAC Crosstalk		(Note 8)		15		nV-s
Output Noise Spectral Density at 1kHz		Full-scale code		250		nV/√Hz
ANALOG OUTPUTS (OUT0 to OUT31)						
Output Voltage Range		VSS = -0.5V, AVCC = +5V	0		5	V
Resistive Load to Ground			10	50		kΩ

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ELECTRICAL CHARACTERISTICS—MAX5732 (0 to +5V Output Voltage Range) (continued)

(AVCC = +5.25V to +5.5V (Note 1), AVDD = +5V ±5%, DVDD = +2.7V to AVDD, VSS = AGND = DGND = REFGND = GS = 0, VREF = +3.0V, RL = ∞, CL = 50pF referenced to ground, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitive Load to Ground				50	100	pF
DC Output Impedance				0.1		Ω
Short-Circuit Current		Sourcing, full-scale code, output connected to AGND		5		mA
		Sinking, zero-scale code, output connected to AVCC		-5		
GROUND-SENSE ANALOG INPUT (GS)						
Input Voltage Range	VGS	Relative to AGND	-0.5		+0.5	V
GS Gain	AGS		0.995	1.000	1.005	V/V
Input Resistance		-0.5V ≤ VGS ≤ +0.5V, VSS = -0.5V	35			kΩ
REFERENCE INPUT (REF)						
Input Resistance			1			MΩ
Reference Input Voltage Range	VREF	Referred to REFGND	2.900	3.000	3.100	V
DIGITAL INPUTS (CS, SCLK, DIN, LDAC, CLR, DSP)						
Input-Voltage High	VIH	DVDD = +2.7V to +3.6V	0.7 × DVDD			V
		DVDD = +4.75V to +5.25V	2.4			
Input-Voltage Low	VIL				0.8	V
Input Capacitance	CIN			10		pF
Input Current	IIN	Digital inputs = 0 or DVDD			±1	μA
POWER REQUIREMENTS (AVCC, VSS, AGND, AVDD, DVDD, DGND)						
Output-Amplifier Positive Supply Voltage	AVCC		4.75		5.50	V
Output-Amplifier Negative Supply Voltage	VSS		-0.5		0	V
Output-Amplifier Supply Voltage Difference		AVCC - VSS			5.75	V
Analog Supply Voltage	AVDD		4.75		5.25	V
Digital Supply Voltage	DVDD		2.70		5.25	V
Analog Supply Current	AIDD	VOUT0 through VOUT31 = 0		10	15	mA
		Software shutdown		10		
Digital Supply Current	DIDD	VIH = DVDD, VIL = 0, fSCLK = 20MHz		2.5	3.5	mA
		VIH = +2.4V, VIL = +0.8V, fSCLK = 20MHz		5	6.5	
Output-Amplifier Positive Supply Current	AICC	VOUT0 through VOUT31 = 0		4	10	mA
		Software shutdown		20		
Output-Amplifier Negative Supply Current	ISS	VSS = -0.5V	VOUT0 through VOUT31 = 0	-4	-10	mA
			Software shutdown	-20		
Power-Supply Rejection Ratio	PSRR			-95		dB

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ELECTRICAL CHARACTERISTICS—MAX5733 (0 to +10V Output Voltage Range)

(AVCC = +10.5V to +11V, AVDD = 5V ±5%, DVDD = +2.7V to AVDD, VSS = AGND = DGND = REFGND = GS = 0, VREF = +3.0V, RL = ∞, CL = 50pF referenced to ground, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		16			Bits
Integral Nonlinearity	INL	MAX5733B (Note 2)		±8	±16	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 3)			±1	LSB
Zero-Scale Error	VOS	VSS = -0.5V, AVCC = +10V (Note 4)		±8	±40	mV
Full-Scale Error		(Note 4)		±8	±50	mV
Gain Error				±0.1	±0.5	% FSR
Gain Temperature Coefficient				20		ppm FSR/°C
DC Crosstalk		VSS = -0.5V, AVCC = +10V (Note 5)		50	250	μV
DYNAMIC CHARACTERISTICS						
Output-Voltage Settling Time		Full-scale change to ±0.5 LSB		20		μs
Voltage-Output Slew Rate				1		V/μs
Digital Feedthrough		(Note 6)		5		nV-s
Digital Crosstalk		(Note 7)		5		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition		120		nV-s
DAC-to-DAC Crosstalk		(Note 8)		15		nV-s
Output Noise Spectral Density at 1kHz		Full-scale code		250		nV/√Hz
ANALOG OUTPUTS (OUT0 to OUT31)						
Output Voltage Range		VSS = -0.5V, AVCC = +10.5V	0		10	V
Resistive Load to Ground			10	50		kΩ
Capacitive Load to Ground				50	100	pF
DC Output Impedance				0.1		Ω
Short-Circuit Current		Sourcing, full scale, output connected to AGND		5		mA
		Sinking, zero scale, output connected to AVCC		-5		
GROUND-SENSE ANALOG INPUT (GS)						
Input Voltage Range	VGS	Relative to AGND	-0.5		+0.5	V
GS Gain	AGS		0.995	1.000	1.005	V/V
Input Resistance		-0.5V ≤ VGS ≤ +0.5V, VSS = -0.5V	70			kΩ
REFERENCE INPUT (REF)						
Input Resistance			1			MΩ
Reference Input Voltage Range	VREF	Referred to REFGND	2.900	3.000	3.100	V

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

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ELECTRICAL CHARACTERISTICS—MAX5733 (0 to +10V Output Voltage Range) (continued)

(AVCC = +10.5V to +11V, AVDD = 5V ±5%, DVDD = +2.7V to AVDD, VSS = AGND = DGND = REFGND = GS = 0, VREF = +3.0V, RL = ∞, CL = 50pF referenced to ground, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (CS, SCLK, DIN, LDAC, CLR, DSP)						
Input-Voltage High	VIH	DVDD = +2.7V to +3.6V	0.7 × DVDD			V
		DVDD = +4.75V to +5.25V	2.4			
Input-Voltage Low	VIL				0.8	V
Input Capacitance	CIN			10		pF
Input Current	IIN	Digital inputs = 0 or DVDD			±1	μA
POWER REQUIREMENTS (AVCC, VSS, AGND, AVDD, DVDD, DGND)						
Output-Amplifier Positive Supply Voltage	AVCC		10		11	V
Output-Amplifier Negative Supply Voltage	VSS		-0.5		0	V
Output-Amplifier Supply Voltage Difference		AVCC - VSS			11	V
Analog Supply Voltage	AVDD		4.75		5.25	V
Digital Supply Voltage	DVDD		2.70		5.25	V
Analog Supply Current	AIDD	VOUT0 through VOUT31 = 0		10	15	mA
		Software shutdown		10		
Digital Supply Current	DIDD	VIH = DVDD, VIL = 0, fSCLK = 20MHz		2.5	3.5	mA
		VIH = +2.4V, VIL = +0.8V, fSCLK = 20MHz		5	6.5	
Output-Amplifier Positive Supply Current	AICC	VOUT0 through VOUT31 = 0		4	10	mA
		Software shutdown		20		
Output-Amplifier Negative Supply Current	ISS	VSS = -0.5V	VOUT0 through VOUT31 = 0	-4	-10	mA
			Software shutdown	-20		
Power-Supply Rejection Ratio	PSRR				-95	dB

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX5734 (-2.5V to +7.5V Output Voltage Range)

(AVCC = +7.75V to +8.25V, AVDD = +5V ±5%, DVDD = +2.7V to AVDD, VSS = -2.75V to -3.25V, AGND = DGND = REFGND = GS = 0, program the offset DAC to 4000hex. VREF = +3.0V, RL = ∞, CL = 50pF referenced to ground, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		16			Bits
Integral Nonlinearity	INL	MAX5734B (Note 2)		±8	±16	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 3)			±1	LSB
Zero-Scale Error	VOS	VSS = -3.25V, AVCC = +7.75V (Note 4)		±8	±40	mV
Full-Scale Error		(Note 4)		±8	±50	mV
Gain Error				±0.1	±0.5	%FSR
Gain Temperature Coefficient				20		ppm FSR/°C
DC Crosstalk		VSS = -3.25V, AVCC = +7.75V (Note 4)		50	250	μV
DYNAMIC CHARACTERISTICS						
Output-Voltage Settling Time		Full-scale change to ±0.5 LSB		20		μs
Voltage-Output Slew Rate				1		V/μs
Digital Feedthrough		(Note 6)		5		nV-s
Digital Crosstalk		(Note 7)		5		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition		120		nV-s
DAC-to-DAC Crosstalk		(Note 8)		15		nV-s
Output Noise Spectral Density at 1kHz		Full-scale code		250		nV/√Hz
ANALOG OUTPUTS (OUT0 to OUT31)						
Output Voltage Range		VSS = -2.75V, AVCC = +7.75V	-2.5		+7.5	V
Resistive Load to Ground			10	50		kΩ
Capacitive Load to Ground				50	100	pF
DC Output Impedance				0.1		Ω
Short-Circuit Current		Sourcing, full scale, output connected to AGND		5		mA
		Sinking, zero scale, output connected to AVCC		-5		
GROUND-SENSE ANALOG INPUT (GS)						
Input Voltage Range	VGS	Relative to AGND	-0.5		+0.5	V
GS Gain	AGS		0.995	1.000	1.005	V/V
Input Resistance		-0.5V ≤ VGS ≤ +0.5V, VSS = -0.5V	70			kΩ
REFERENCE INPUT (REF)						
Input Resistance			1			MΩ
Reference Input Voltage Range	VREF	Referred to REFGND	2.900	3.000	3.100	V

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

MAX5732-MAX5735

ELECTRICAL CHARACTERISTICS—MAX5734 (-2.5V to +7.5V Output Voltage Range) (continued)

(AVCC = +7.75V to +8.25V, AVDD = +5V ±5%, DVDD = +2.7V to AVDD, VSS = -2.75V to -3.25V, AGND = DGND = REFGND = GS = 0, program the offset DAC to 4000hex. VREF = +3.0V, RL = ∞, CL = 50pF referenced to ground, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
DIGITAL INPUTS (CS, SCLK, DIN, LDAC, CLR, DSP)							
Input-Voltage High	VIH	DVDD = +2.7V to +3.6V	0.7 × DVDD			V	
		DVDD = +4.75V to +5.25V	2.4				
Input-Voltage Low	VIL				0.8	V	
Input Capacitance	CIN			10		pF	
Input Current	IIN	Digital inputs = 0 or DVDD			±1	μA	
POWER REQUIREMENTS (AVCC, VSS, AGND, AVDD, DVDD, DGND)							
Output-Amplifier Positive Supply Voltage	AVCC		7.50		8.25	V	
Output-Amplifier Negative Supply Voltage	VSS		-3.25		-2.50	V	
Output-Amplifier Supply Voltage Difference		AVCC - VSS			11	V	
Analog Supply Voltage	AVDD		4.75		5.25	V	
Digital Supply Voltage	DVDD		2.70		5.25	V	
Analog Supply Current	AIDD	VOUT0 through VOUT31 = 0		10	15	mA	
		Software shutdown		10		μA	
Digital Supply Current	DIDD	VIH = DVDD, VIL = 0, fSCLK = 20MHz		2.5	3.5	mA	
		VIH = +2.4V, VIL = +0.8V, fSCLK = 20MHz		5	6.5		
Output-Amplifier Positive Supply Current	AICC	VOUT0 through VOUT31 = 0		4	10	mA	
		Software shutdown		20		μA	
Output-Amplifier Negative Supply Current	ISS	VSS = -2.75V	VOUT0 through VOUT31 = 0		-4	-10	mA
			Software shutdown		-20		μA
Power-Supply Rejection Ratio	PSRR			-95		dB	

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX5735 (-5V to +5V Output Voltage Range)

(AVCC = +5.25V to +5.5V, AVDD = +5V ±5%, DVDD = +2.7V to AVDD, VSS = -5.25V to -5.5V, AGND = DGND = REFGND = GS = 0, program the offset DAC to 8000hex. VREF = +3.0V, RL = ∞, CL = 50pF referenced to ground, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		16			Bits
Integral Nonlinearity	INL	MAX5735B (Note 2)		±8	±16	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 3)			±1	LSB
Zero-Scale Error	VOS	VSS = -5.25V, AVCC = +5.25V (Note 4)		±8	±40	mV
Full-Scale Error		(Note 4)		±8	±50	mV
Gain Error				±0.1	±0.5	%FSR
Gain Temperature Coefficient				20		ppm FSR/°C
DC Crosstalk		VSS = -5.75V, AVCC = +5.25V (Note 5)		50	250	μV
DYNAMIC CHARACTERISTICS						
Output-Voltage Settling Time		Full-scale change to ±0.5 LSB		20		μs
Voltage-Output Slew Rate				1		V/μs
Digital Feedthrough		(Note 6)		5		nV-s
Digital Crosstalk		(Note 7)		5		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition		120		nV-s
DAC-to-DAC Crosstalk		(Note 8)		15		nV-s
Output Noise Spectral Density at 1kHz		Full-scale code		250		nV/√Hz
ANALOG OUTPUTS (OUT0 through OUT31)						
Output Voltage Range		VSS = -5.25V, AVCC = +5.25V	-5		+5	V
Resistive Load to Ground			10	50		kΩ
Capacitive Load to Ground				50	100	pF
DC Output Impedance				0.1		Ω
Short-Circuit Current		Sourcing, full scale, output connected to AGND		5		mA
		Sinking, zero scale, output connected to AVCC		-5		
GROUND-SENSE ANALOG INPUT (GS)						
Input Voltage Range	VGS	Relative to AGND	-0.5		+0.5	V
GS Gain	AGS		0.995	1.000	1.005	V/V
Input Resistance		-0.5V ≤ VGS ≤ +0.5V, VSS = -0.5V	70			kΩ
REFERENCE INPUT (REF)						
Input Resistance			1			MΩ
Reference Input Voltage Range	VREF	Referred to REFGND	2.900	3.000	3.100	V

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MAX5732-MAX5735

ELECTRICAL CHARACTERISTICS—MAX5735 (-5V to +5V Output Voltage Range) (continued)

(AV_{CC} = +5.25V to +5.5V, AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = -5.25V to -5.5V, AGND = DGND = REFGND = GS = 0, program the offset DAC to 8000hex. V_{REF} = +3.0V, R_L = ∞, C_L = 50pF referenced to ground, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
DIGITAL INPUTS (CS, SCLK, DIN, LDAC, CLR, DSP)							
Input-Voltage High	V _{IH}	DV _{DD} = +2.7V to +3.6V	0.7 × DV _{DD}			V	
		DV _{DD} = +4.75V to 5.25V	2.4				
Input-Voltage Low	V _{IL}				0.8	V	
Input Capacitance	C _{IN}			10		pF	
Input Current	I _{IN}	Digital inputs = 0 or DV _{DD}			±1	μA	
POWER REQUIREMENTS (AV_{CC}, V_{SS}, AGND, AV_{DD}, DV_{DD}, DGND)							
Output-Amplifier Positive Supply Voltage	AV _{CC}		4.75		5.50	V	
Output-Amplifier Negative Supply Voltage	V _{SS}		-5.50		-4.75	V	
Output-Amplifier Supply Voltage Difference		AV _{CC} - V _{SS}			11	V	
Analog Supply Voltage	AV _{DD}		4.75		5.25	V	
Digital Supply Voltage	DV _{DD}		2.70		5.25	V	
Analog Supply Current	AI _{DD}	V _{OUT0} through V _{OUT31} = 0		10	15	mA	
		Software shutdown		10		μA	
Digital Supply Current	DI _{DD}	V _{IH} = DV _{DD} , V _{IL} = 0, f _{SCLK} = 20MHz		2.5	3.5	mA	
		V _{IH} = +2.4V, V _{IL} = +0.8V, f _{SCLK} = 20MHz		5	6.5		
Output-Amplifier Positive Supply Current	AI _{CC}	V _{OUT0} through V _{OUT31} = 0		4	10	mA	
		Software shutdown		20		μA	
Output-Amplifier Negative Supply Current	ISS	V _{SS} = -0.5V	V _{OUT0} through V _{OUT31} = 0		-4	-10	mA
			Software shutdown		-20		μA
Power-Supply Rejection Ratio	PSRR			-95		dB	

Note 1: AV_{CC} should be at least 0.25V higher than the maximum output voltage required from the DAC. Full-scale output is 5V for the MAX5732.

Note 2: Linearity guaranteed from code 4047 to full scale and from (V_{SS} + 0.3V) to (AV_{CC} - 0.3V).

Note 3: DNL guaranteed over all codes for (V_{SS} + 0.3V) to (AV_{CC} - 0.3V).

Note 4: Zero-scale error is measured at code 0. Full-scale error is measured at code FFFFhex.

Note 5: DC crosstalk is the change in the output level of one DAC at midscale in response to the full-scale output change of all other DACs.

Note 6: Digital feedthrough is a measure of the impulse injected into the analog outputs from the digital control inputs when the device is not being written to. It is measured with a worst-case change on the digital inputs.

Note 7: Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale while a full-scale code change is written into another DAC.

Note 8: DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog output change at another converter.

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

TIMING CHARACTERISTICS—DV_{DD} = +4.75V to +5.25V

(Figures 2 and 3, AV_{DD} = +4.75V to +5.25V, DV_{DD} = +4.75V to +5.25V, AGND = DGND = REFGND = GS = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f _{SCLK}		0		33	MHz
SCLK Pulse-Width High	t _{CH}		10			ns
SCLK Pulse-Width Low	t _{CL}		10			ns
SCLK Fall to $\overline{\text{CS}}$ Fall Setup Time	t _{SCS}		6			ns
$\overline{\text{CS}}$ Fall to SCLK Fall Setup Time	t _{CSS}		5			ns
$\overline{\text{CS}}$ Rise to SCLK Fall	t _{CS1}	At end of cycle in SPI mode only	15			ns
SCLK Fall to $\overline{\text{CS}}$ Rise Setup Time	t _{CS2}		0			ns
DIN to SCLK Fall Setup Time	t _{DS}		10			ns
DIN to SCLK Fall Hold Time	t _{DH}		2			ns
SCLK Fall to DOUT Fall	t _{SCL}	Load capacitance = 20pF			20	ns
SCLK Fall to DOUT Rise	t _{SDH}	Load capacitance = 20pF			20	ns
$\overline{\text{CS}}$ Pulse-Width High	t _{CSPWH}		50			ns
$\overline{\text{CS}}$ Pulse-Width Low	t _{CSPWL}		20			ns
$\overline{\text{LDAC}}$ Pulse-Width Low	t _{LDAC}		20			ns
$\overline{\text{CLR}}$ Pulse-Width Low	t _{CLR}		20			ns

TIMING CHARACTERISTICS—DV_{DD} = +2.7V to +5.25V

(Figures 2 and 3, AV_{DD} = +4.75V to +5.25V, DV_{DD} = +2.7V to +5.25V, AGND = DGND = REFGND = GS = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

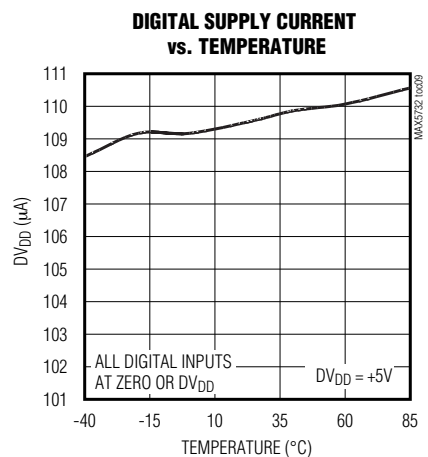
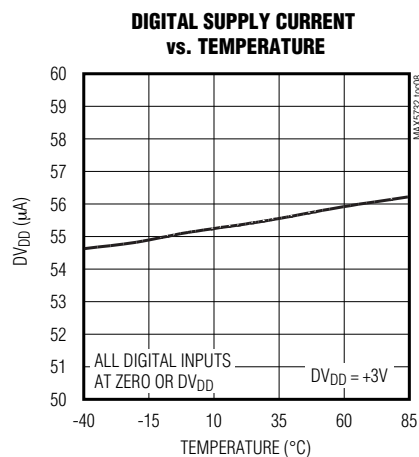
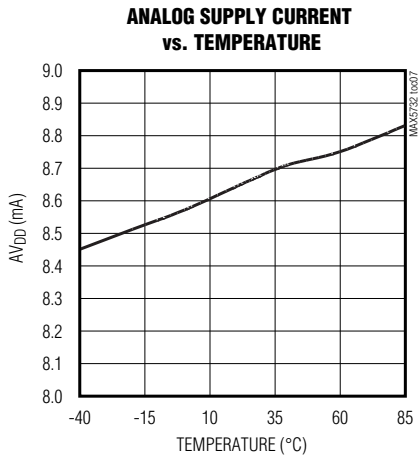
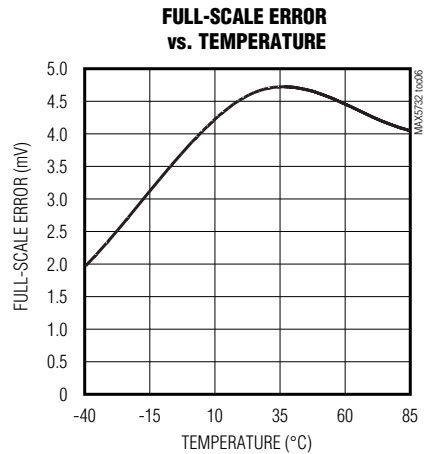
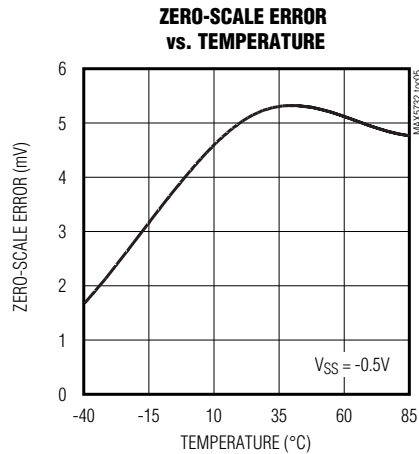
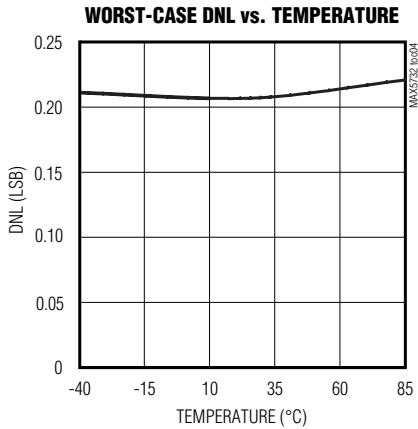
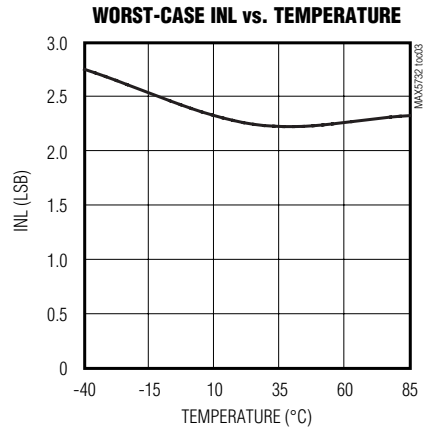
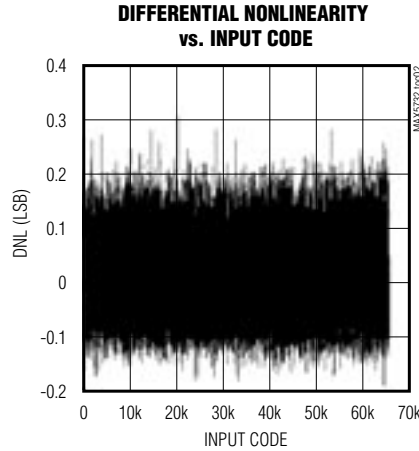
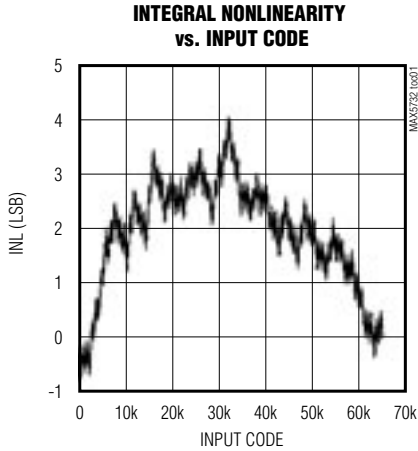
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f _{SCLK}		0		25	MHz
SCLK Pulse-Width High	t _{CH}		10			ns
SCLK Pulse-Width Low	t _{CL}		10			ns
SCLK Fall to $\overline{\text{CS}}$ Fall Setup Time	t _{SCS}		10			ns
$\overline{\text{CS}}$ Fall to SCLK Fall Setup Time	t _{CSS}		10			ns
$\overline{\text{CS}}$ Rise to SCLK Fall	t _{CS1}	At end of cycle in SPI mode only	18			ns
SCLK Fall to $\overline{\text{CS}}$ Rise Setup Time	t _{CS2}		0			ns
DIN to SCLK Fall Setup Time	t _{DS}		10			ns
DIN to SCLK Fall Hold Time	t _{DH}		2			ns
SCLK Fall to DOUT Fall	t _{SCL}	Load capacitance = 20pF			25	ns
SCLK Fall to DOUT Rise	t _{SDH}	Load capacitance = 20pF			25	ns
$\overline{\text{CS}}$ Pulse-Width High	t _{CSPWH}		50			ns
$\overline{\text{CS}}$ Pulse-Width Low	t _{CSPWL}		20			ns
$\overline{\text{LDAC}}$ Pulse-Width Low	t _{LDAC}		20			ns
$\overline{\text{CLR}}$ Pulse-Width Low	t _{CLR}		20			ns

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

Typical Operating Characteristics

($V_{CC} = +10.5V \pm 5\%$, $V_{DD} = +5V \pm 5\%$, $DV_{DD} = +5V$, $V_{SS} = AGND = DGND = REFGND = GS = 0$, $V_{REF} = +3.000V$, $R_L = \infty$, $C_L = 50pF$ referenced to ground, output gain = 2.5, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$).

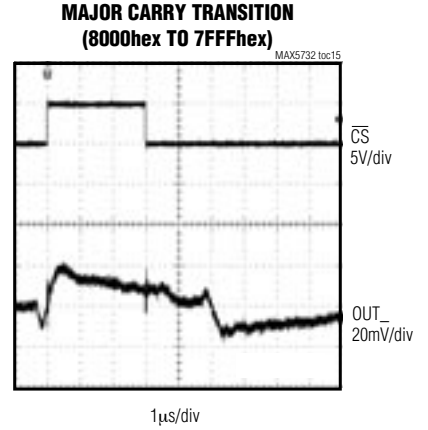
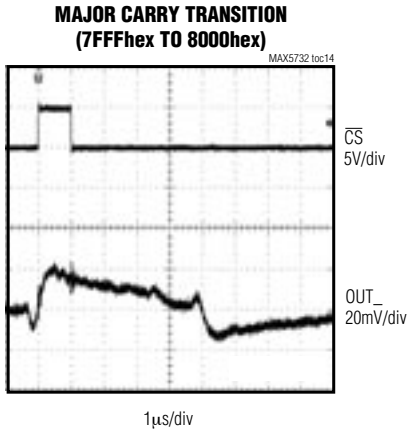
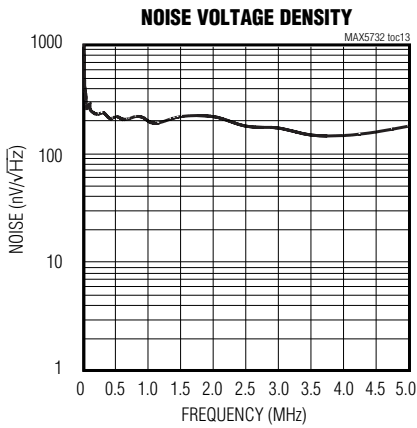
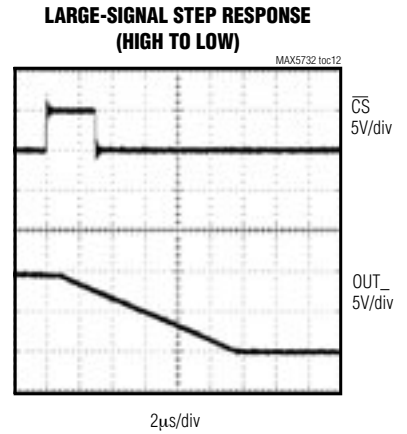
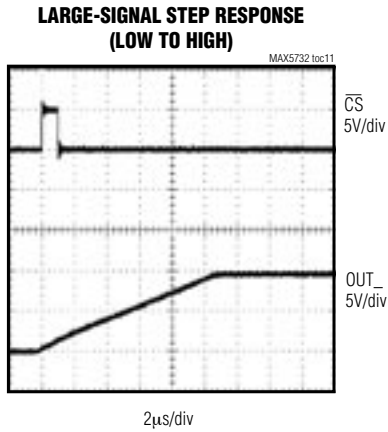
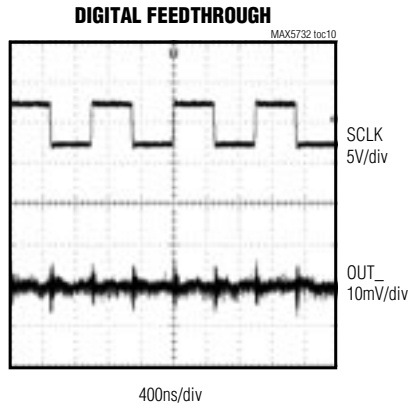
MAX5732-MAX5735



32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

(AVCC = +10.5V ±5%, AVDD = +5V ±5%, DVDD = +5V, VSS = AGND = DGND = REFGND = GS = 0, VREF = +3.000V, RL = ∞, CL = 50pF referenced to ground, output gain = 2.5, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C).



32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

Pin Description

MAX5732-MAX5735

PIN	NAME	FUNCTION
1, 42, 48	AV _{CC}	Output-Amplifier Positive Supply Input. Bypass to V _{SS} with a 0.1μF capacitor.
2	OUT9	DAC9 Buffered Analog Output Voltage
3	OUT8	DAC8 Buffered Analog Output Voltage
4	OUT7	DAC7 Buffered Analog Output Voltage
5	N.C.	No Connection. Internally connected. Do not make any connections to N.C.
6	OUT6	DAC6 Buffered Analog Output Voltage
7	OUT5	DAC5 Buffered Analog Output Voltage
8	OUT4	DAC4 Buffered Analog Output Voltage
9, 38	AGND	Analog Ground
10	OUT3	DAC3 Buffered Analog Output Voltage
11, 28, 39	V _{SS}	Output-Amplifier Negative Supply Input
12	OUT2	DAC2 Buffered Analog Output Voltage
13	OUT1	DAC1 Buffered Analog Output Voltage
14	OUT0	DAC0 Buffered Analog Output Voltage
15	$\overline{\text{DSP}}$	Digital Serial-Interface-Select Input. Drive low for DSP-interface mode. Drive high for SPI-interface mode.
16	$\overline{\text{CS}}$	Active-Low Digital Chip-Select Input
17	DOUT	Digital Serial-Data Output. Use DOUT to daisy chain and read the contents of the DAC registers.
18	SCLK	Digital Serial-Clock Input
19	DIN	Digital Serial-Data Input
20	DV _{DD}	Digital Power-Supply Input. Bypass to DGND with a 0.1μF capacitor.
21	DGND	Digital Ground
22	$\overline{\text{LDAC}}$	Active-Low Digital Load DAC Input. Drive this asynchronous input low to transfer the contents of the input register to their respective DAC registers and set all DAC outputs accordingly.
23	$\overline{\text{CLR}}$	Active-Low Digital Clear Input. Drive this asynchronous input low to clear the contents of the input and DAC registers and set all the DAC outputs to zero.
24	GS	Ground-Sense Analog Input. Offsets the DAC amplifier outputs by ±0.5V to compensate for a remote system ground potential difference.
25, 49	REFGND	Reference Ground
26	REF	Analog Reference Voltage Input
27, 50	AV _{DD}	Analog Power-Supply Input. Bypass to AGND with a 0.1μF capacitor.
29	OUT31	DAC31 Buffered Analog Output Voltage
30	OUT30	DAC30 Buffered Analog Output Voltage
31	OUT29	DAC29 Buffered Analog Output Voltage
32	OUT28	DAC28 Buffered Analog Output Voltage
33	OUT27	DAC27 Buffered Analog Output Voltage
34	OUT26	DAC26 Buffered Analog Output Voltage
35	OUT25	DAC25 Buffered Analog Output Voltage
36	OUT24	DAC24 Buffered Analog Output Voltage
37	OUT23	DAC23 Buffered Analog Output Voltage

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

Pin Description (continued)

PIN	NAME	FUNCTION
40	OUT22	DAC22 Buffered Analog Output Voltage
41	OUT21	DAC21 Buffered Analog Output Voltage
43	OUT20	DAC20 Buffered Analog Output Voltage
44	OUT19	DAC19 Buffered Analog Output Voltage
45	OUT18	DAC18 Buffered Analog Output Voltage
46	OUT17	DAC17 Buffered Analog Output Voltage
47	OUT16	DAC16 Buffered Analog Output Voltage
51	OUT15	DAC15 Buffered Analog Output Voltage
52	OUT14	DAC14 Buffered Analog Output Voltage
53	OUT13	DAC13 Buffered Analog Output Voltage
54	OUT12	DAC12 Buffered Analog Output Voltage
55	OUT11	DAC11 Buffered Analog Output Voltage
56	OUT10	DAC10 Buffered Analog Output Voltage
—	EP	Exposed Paddle. Internally connected to V _{SS} . Connect externally to a metal pad for improved thermal dissipation.

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

MAX5732-MAX5735

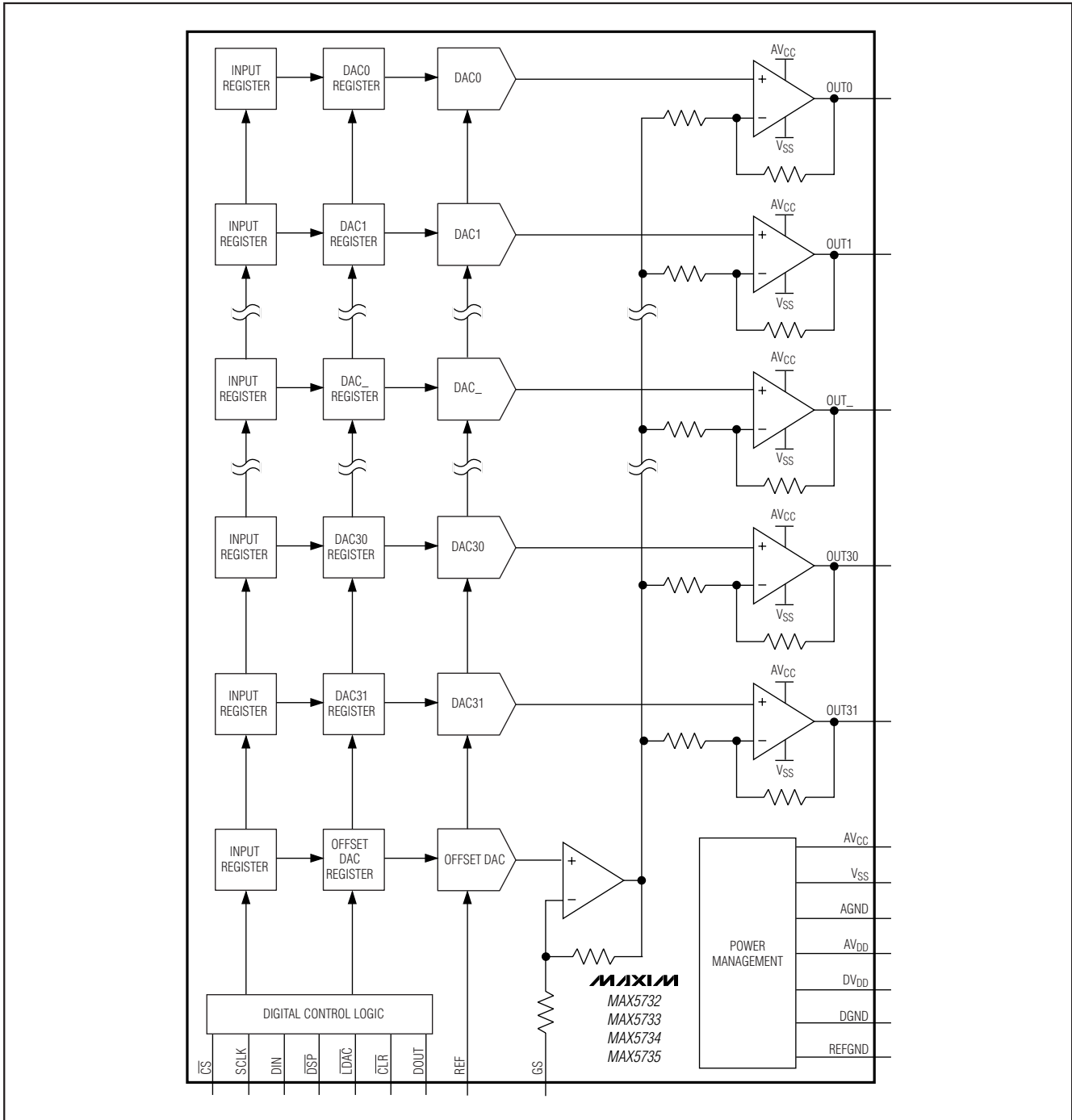


Figure 1. Functional Diagram

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

Detailed Description

The MAX5732–MAX5735 are 32-channel, 16-bit, voltage-output DACs (Figure 1). The devices accept a 3V external reference input at REF. An internal offset DAC allows all outputs to be offset (see Table 1). The devices provide a ground-sensing function that allows the output voltages to be referenced to a remote ground.

A 33MHz SPI-/QSPI-/MICROWIRE- and DSP-compatible serial interface controls the MAX5732–MAX5735 (Figure 2). Each DAC includes a double-buffered input structure to minimize the digital noise feedthrough from the digital inputs to the outputs, and allows for synchronous or asynchronous updating of the outputs. The two buffers are organized as an input register followed by a DAC register that stores the contents of the output. Input registers update the DAC registers independently or simultaneously with a single software or hardware command. The MAX5732–MAX5735 also have a DOUT that allows for read-back or daisy chaining multiple devices.

The MAX5732–MAX5735 analog and digital sections have separate power inputs. Separate power inputs are also provided for the output buffer amplifiers. Proprietary deglitch circuits prevent output glitches at power-up and eliminate the need for power sequencing. A software-shutdown mode allows efficient power management. The MAX5732–MAX5735 consume 50 μ A of supply current in shutdown.

All DACs provide buffered outputs that can drive 10k Ω in parallel with 100pF. The MAX5732 has a 0 to +5V output range; the MAX5733 has a 0 to +10V output

range; the MAX5734 has a -2.5V to +7.5V output range; and the MAX5735 has a -5V to +5V output range.

The MAX5732–MAX5735 are available in a 56-pin 8mm x 8mm thin QFN package and are specified over the extended -40°C to +85°C temperature range.

External Reference Input (REF)

The REF voltage sets the full-scale output voltage for all 32 DACs. REF accepts a +3V \pm 3% input. Reference voltages outside these limits can result in a degradation of device performance.

REF is a buffered input. The typical input impedance is 10M Ω , and it does not vary with code. Use a high-accuracy, low-noise voltage reference such as the MAX6126AASA30 (3ppm/°C temp drift and 0.02% initial accuracy) to improve static accuracy. REF does not accept AC signals.

Ground Sense (GS)

The MAX5732–MAX5735 include a GS that allows the output voltages to be referenced to a remote ground. The GS input voltage range (V_{GS}) is -0.5V to +0.5V. V_{GS} is added to the output voltage with unity gain. The resulting output voltage must be within the valid output-voltage range set by the power supplies. See the *Output Amplifiers (OUT0–OUT31)* section for the effect of the GS inputs on the DAC outputs.

Offset DAC

The MAX5732–MAX5735 feature an offset DAC that determines the output voltage range. While each part number has an output voltage range associated with it,

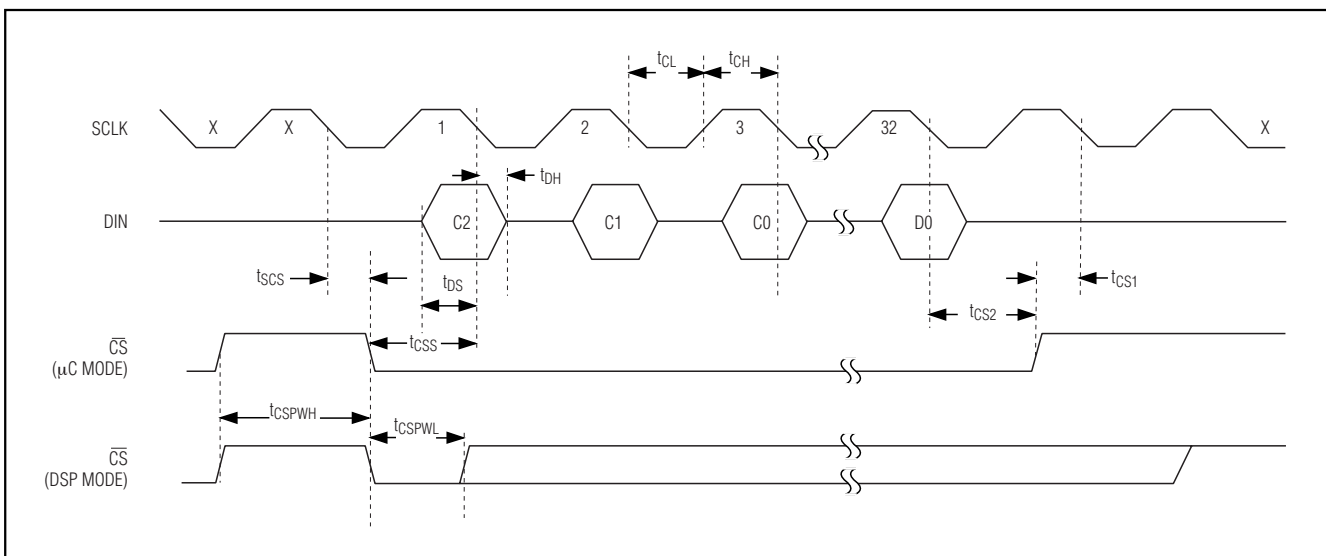


Figure 2. Serial-interface Timing

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

Table 1. Offset DAC Codes

PART NUMBER	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MAX5732	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MAX5733	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MAX5734	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MAX5735	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: For the MAX5732, the maximum code for the offset DAC is 16384. For the MAX5733/MAX5734/MAX5735, the maximum code for the offset DAC is 40000.

it is the offset DAC that determines the end-point voltages of the range. Table 1 shows the offset DAC code required during power-up.

Note: The offset DAC of every device can be programmed with any of the four output voltage ranges. However, the specifications in the *Electrical Characteristics* table are only guaranteed (production tested) for the offset code associated with each particular part number. For example, the MAX5734 specifications are only valid with the MAX5734 offset- DAC code shown in Table 1.

The offset DAC is summed with GS (Figure 1). The offset DAC can also cancel the offset of the output buffers. Any change in the offset DAC affects all 32 DACs.

The offset DAC is also configured identically to the other 32 DACs with an input and DAC register. Write to the offset DAC through the serial interface by using control bits C2, C1, and C0 = 001 followed by the data bits D15–D0. The CLR command affects the offset DAC as well as the other DACs.

The data format for the offset DAC codes are: control bits C2, C1, and C0 = 011, address bits A5–A0 = 100000, 7 don't-care bits, and 16 data bits as shown in Table 2.

Output Amplifiers (OUT0–OUT31)

All DAC outputs are internally buffered. The internal buffers provide gain, improved load regulation, and transition glitch suppression for the DAC outputs. The output buffers slew at 1V/μs and can drive 10kΩ in parallel with 100pF. The output buffers are powered by AVCC and

Table 2. Serial Data Format

CONTROL BITS	ADDRESS BITS	DON'T-CARE BITS	DATA BITS
C2, C1, AND C0	A5–A0	—	D15–D0
011	100000	XXXXXXX	See table 1

VSS. AVCC and VSS determine the maximum output voltage range of the device.

The input code, the voltage reference, the offset DAC output, the voltage on GS, and the gain of the output amplifier determine the output voltage. Calculate VOUT as follows:

$$V_{OUT} = \frac{GAIN \times V_{REF} \times (DAC \text{ code} - \text{offset DAC code})}{2^{16}} + V_{GS}$$

where GAIN = 5/3 for the MAX5732, or GAIN = 10/3 for the MAX5733/MAX5734/MAX5735.

Load-DAC (LDAC) Input

The MAX5732–MAX5735 feature an active-low LDAC logic input that allows the outputs OUT_n to update asynchronously. Keep LDAC high during normal operation (when the device is controlled only through the serial interface). Drive LDAC low to simultaneously update all DAC outputs with data from their respective input registers. Figure 3 shows the LDAC timing with respect to OUT_n.

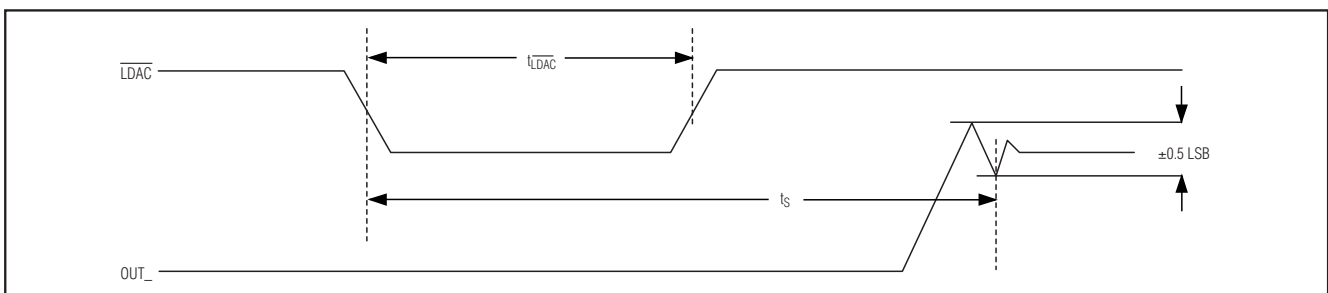


Figure 3. LDAC Timing

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

A software command can also activate the $\overline{\text{LDAC}}$ operation. To activate $\overline{\text{LDAC}}$ by software, set control bits C2, C1, and C0 = 010, address bits A5–A0 = 111111, and all data bits to don't care. See Table 3 for the data format. This operation updates all DAC outputs.

Note: The software load DAC does not affect the offset DAC.

Clear ($\overline{\text{CLR}}$)

The MAX5732–MAX5735 feature an active-low $\overline{\text{CLR}}$ logic input that sets all channels including the offset DAC to 0V (code 0000hex). The offset DAC needs to be reprogrammed after $\overline{\text{CLR}}$ is asserted. Driving $\overline{\text{CLR}}$ low clears the contents of both the input and DAC registers. The serial interface can also issue a software clear command. Setting the control bits C2, C1, and C0 = 111 (Table 4) performs the same function as driving logic-input $\overline{\text{CLR}}$ low. Table 4 shows the clear-data format for the software-controlled clear command. This register-reset process cannot be interrupted. All serial input data is ignored until the entire reset process is complete.

Table 3. Load-DAC Data Format

CONTROL BITS	ADDRESS BITS	DON'T-CARE BITS	DATA BITS
C2, C1, AND C0	A5–A0	—	D15–D0
010	111111	XXXXXXXX	XXXXXXXXXXXXXXXXXXXX

Table 4. Clear-Data Format

CONTROL BITS	ADDRESS BITS	DON'T-CARE BITS	DATA BITS
C2, C1, AND C0	A5–A0	—	D15–D0
111	See table 7	XXXXXXXX	XXXXXXXXXXXXXXXXXXXX

Table 5. Serial-Data Format

CONTROL BITS	ADDRESS BITS	DON'T-CARE BITS	DATA BITS
MSB		LSB	
C2, C1, and C0	A5–A0	XXXXXXXX	D15–D0

Serial Interface

A 3-wire SPI-/QSPI-/MICROWIRE- and DSP-compatible serial interface controls the MAX5732–MAX5735. The interface requires a 32-bit command word to control the device. The command word consists of 3 control bits, 6 address bits, 7 don't-care bits, and 16 data bits. Table 5 shows the general serial-data format. The control bits control various write and read commands as well as the load DAC and clear commands. Table 6 shows the control-bit functions. The address bits select the register(s) to be written. Table 7 shows the address functions. The data bits control the value of the DAC outputs.

Table 6. Control-Bit Functions

CONTROL BITS			CONTROL-BIT DESCRIPTION
C2	C1	C0	
0	0	0	No operation (NOP); no internal registers change state. The NOP command can be passed to DOUT depending on the state of the configuration register. Address bits A5–A0 and data bits D15–D0 are ignored.
0	0	1	Loads D15–D0 into the input register(s) for the selected address. Depending on the address bits, this command could write to: The configuration register (A[5:0] = 100001) One of the input registers of the 32 DAC channels All 32 DAC input registers (A[5:0] = 111111) The offset DAC input register (A[5:0] = 100000)
0	1	0	Loads DAC register(s) from the input register(s). Depending on the address bits, this command can update one or all of the DAC registers from the stored input register value(s). Data bits D15–D0 are ignored.
0	1	1	Write-through; loads D15–D0 into the input and DAC registers, depending on the address bits.
1	0	0	Read command; depending on the address bits, one of the DAC-register values or the configuration-register value may be read back through DOUT. Data bits D15–D0 are ignored.
1	0	1	Reserved for internal testing; do not use.
1	1	0	Reserved for internal testing; do not use.
1	1	1	Clear register(s); depending on the address bits, one or all registers (except the offset-DAC registers) are cleared to zero. Data bits D15–D0 are ignored.

32-Channel, 16-Bit, Voltage-Output DACs with Serial Interface

Table 7. Address-Bit Functions

ADDRESS BITS						CONTROL FUNCTION
A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	DAC0
0	0	0	0	0	1	DAC1
0	0	0	0	1	0	DAC2
0	0	0	0	1	1	DAC3
0	0	0	1	0	0	DAC4
0	0	0	1	0	1	DAC5
0	0	0	1	1	0	DAC6
0	0	0	1	1	1	DAC7
0	0	1	0	0	0	DAC8
0	0	1	0	0	1	DAC9
0	0	1	0	1	0	DAC10
0	0	1	0	1	1	DAC11
0	0	1	1	0	0	DAC12
0	0	1	1	0	1	DAC13
0	0	1	1	1	0	DAC14
0	0	1	1	1	1	DAC15
0	1	0	0	0	0	DAC16
0	1	0	0	0	1	DAC17
0	1	0	0	1	0	DAC18
0	1	0	0	1	1	DAC19
0	1	0	1	0	0	DAC20
0	1	0	1	0	1	DAC21
0	1	0	1	1	0	DAC22
0	1	0	1	1	1	DAC23
0	1	1	0	0	0	DAC24
0	1	1	0	0	1	DAC25
0	1	1	0	1	0	DAC26
0	1	1	0	1	1	DAC27
0	1	1	1	0	0	DAC28
0	1	1	1	0	1	DAC29
0	1	1	1	1	0	DAC30
0	1	1	1	1	1	DAC31
1	0	0	0	0	0	Offset DAC
1	0	0	0	0	1	Configuration register; control bits C2, C1, and C0 = 010 and C2, C1, and C0 = 011 set the error flag in the configuration register. Do not use these control bits with these address bits.

ADDRESS BITS						CONTROL FUNCTION
A5	A4	A3	A2	A1	A0	
1	0	0	0	1	0	Command reserved; do not use.
1	0	0	0	1	1	Command reserved; do not use.
1	0	0	1	0	0	Command reserved; do not use.
1	0	0	1	0	1	Command reserved; do not use.
1	0	0	1	1	0	Command reserved; do not use.
1	0	0	1	1	1	Command reserved; do not use.
1	0	1	0	0	0	Command reserved; do not use.
1	0	1	0	0	1	Command reserved; do not use.
1	0	1	0	1	0	Command reserved; do not use.
1	0	1	0	1	1	Command reserved; do not use.
1	0	1	1	0	0	Command reserved; do not use.
1	0	1	1	0	1	Command reserved; do not use.
1	0	1	1	1	0	Command reserved; do not use.
1	0	1	1	1	1	Command reserved; do not use.
1	1	0	0	0	0	Command reserved; do not use.
1	1	0	0	0	1	Command reserved; do not use.
1	1	0	0	1	0	Command reserved; do not use.
1	1	0	0	1	1	Command reserved; do not use.
1	1	0	1	0	0	Command reserved; do not use.
1	1	0	1	0	1	Command reserved; do not use.
1	1	0	1	1	0	Command reserved; do not use.
1	1	0	1	1	1	Command reserved; do not use.
1	1	1	0	0	0	Command reserved; do not use.
1	1	1	0	0	1	Command reserved; do not use.
1	1	1	0	1	0	Command reserved; do not use.
1	1	1	0	1	1	Command reserved; do not use.
1	1	1	1	0	0	Command reserved; do not use.
1	1	1	1	0	1	Command reserved; do not use.
1	1	1	1	1	0	Command reserved; do not use.
1	1	1	1	1	1	All channels (DAC31–DAC0); used for write commands only. Read commands cannot be used with these address bits.

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Table 8. Configuration-Register Data Format

16 DATA BITS															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ERRF	SING	GLT	DT	SHDN	X	X	X	X	X	X	X	X	X	X	X

X = Don't care.

Table 9. Configuration-Register Commands

DATA BIT	NAME	DESCRIPTION
D15	ERRF	Error flag; ERRF goes logic-high when an invalid command is attempted. ERRF is cleared each time the configuration register is read back to DOUT. Clear-register commands C2, C1, and C0 = 111 resets ERRF. Conditions that trigger ERRF include: Attempted read of address bits A5–A0 = 111111 (all 32 DACs) Access to reserved addresses Access to the configuration register (address bits A5–A0 = 100001 when used with control bits C2, C1, and C0 = 010 and 011) Default is logic-low (no error flags); ERRF is read only.
D14	SING	Single device; SING determines the manner in which data is output to DOUT. A logic-high sets the device to operate in stand-alone mode or in parallel; only the 16 data bits are output to DOUT. A logic-low sets the device to operate in a daisy chain of devices. In this case, the entire 32-bit command word is output to DOUT. Default is logic-low (daisy-chain mode); SING is read/write.
D13	GLT	Glitch-suppression enable; the MAX5732–MAX5735 feature glitch-suppression circuitry on the analog outputs that minimizes the output glitch during a major carry transition. A logic-low disables the internal glitch-suppression circuitry, which improves settling time. A logic-high enables glitch-suppression, suppressing up to 120nV-s glitch impulse on the DAC outputs. Default is logic-low (glitch suppression disabled); GLT is read/write.
D12	DT	Digital output enable; a logic-low enables DOUT. A logic-high disables DOUT. Disabling DOUT reduces power consumption and digital noise feedthrough to the DAC outputs from the DOUT output buffer. Default is logic-low (DOUT enabled); DT is read/write.
D11	SHDN	Shutdown; a logic-high shuts down all 32 DACs. The logic interface remains active, and the data is retained in the input and DAC registers. Read/write operations can be performed while the device is disabled; however, no changes can occur at the device outputs. A logic-low powers up all 32 DACs if the device was previously in shutdown. Upon waking up, the DAC outputs return to the last stored value in the DAC registers. Default is logic-low (normal operation); SHDN is read/write.
D10–D0	X	Don't care.

DSP Mode (\overline{DSP})

The MAX5732–MAX5735 provide a hardware-selectable DSP-interface mode. DSP mode, when active, allows chip select (\overline{CS}) to go high before the entire 32-bit command word is clocked in. The active-low DSP logic input selects microcontroller (μ C)- or DSP-interface mode. Drive \overline{DSP} low for DSP-interface mode. Drive \overline{DSP} high for μ C-interface mode. Figure 2 illustrates serial timing for both μ C- and DSP-interface modes.

Configuration Register

The configuration register controls the advanced features of the MAX5732–MAX5735. Write to the configuration register by setting the control bits C2, C1, and C0 = 001 and address bits A5–A0 = 100001. Table 8 shows the configuration-register data format for the D15–D0 data bits. Table 9 shows the commands controlled by the configuration register.

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SING

When SING = 0 (default power-up mode), the device is in daisy-chain mode. DOUT follows DIN after 32 clock cycles. For the read command, DOUT provides the read data in the next cycle following CS rising edge. The 16 data bits of the previous command word are clocked out on the last 16 clock cycles of the current command word.

When SING = 1, the device is in stand-alone mode. To reduce the time it takes to read data out, the read data is provided at DOUT as the 16 data bits of the current command are clocked in. The device acts on an incoming command word independent of the rising edge of CS.

Daisy Chain Operation

Any number of the MAX5732–MAX5735 devices can be daisy chained by connecting the DOUT of one device to the DIN of another device in a chain. All devices must be in SING = 0 mode. Connecting the CS inputs of all devices together eliminates the need to issue NOP commands to devices early in the chain (see Figure 4).

Data Readback

The contents of the MAX5732–MAX5735 DAC and configuration registers can be read on DOUT by issuing a read-data command. Setting control bits C2, C1, and C0 = 100, puts the device in read-data mode. The address bits select the register to be read. The contents of the register (16 data bits) are clocked out at DOUT. The output-data format depends on the status of DSP and SING. Table 10 shows the manner in which

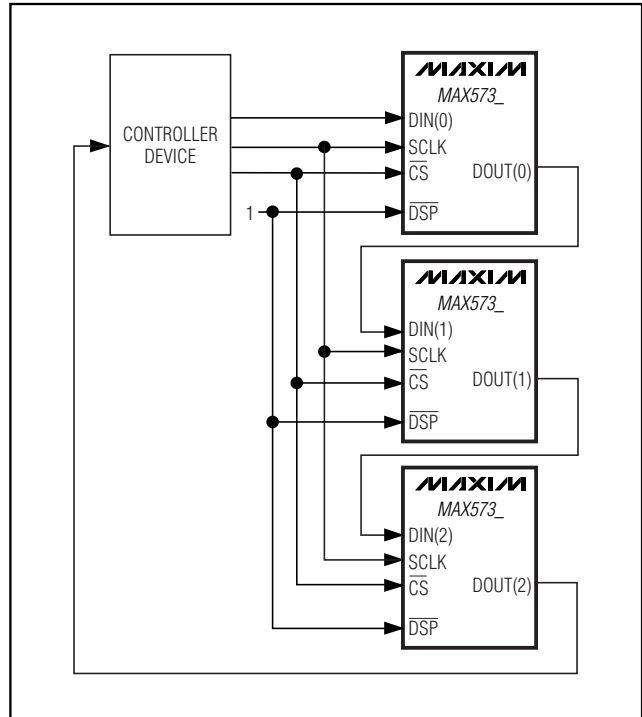


Figure 4. Daisy-Chain Configuration

data is written to DOUT. Note that when the device is in DSP mode (DSP = 0), only the 16-bit data of the selected register is written to DOUT.

Table 10. Read-Data Modes with SING and DSP Controls

DSP	SING	CONFIGURATION DESCRIPTION	READ DATA AT DOUT
0	0	Stand alone	DOUT provides the 16 data bits from the previous command word. Data appears at DOUT on the last 16 clock edges of the current command word. See Figure 7.
0	1	Stand alone	DOUT provides the 16 data bits from the current command word. Data appears at DOUT on the last 16 clock edges of the current command word. See Figure 7.
1	0	Daisy chain	Data on DOUT follows the current command word after 32 clock cycles. For read commands, the read data from the previous command word appears at DOUT on the last 16 clock edges of the current command word. See Figure 4.
1	1	Multiple DOUTs connected in parallel (not daisy chained)	DOUT provides the 16 data bits from the current command word. Data appears at DOUT on the last 16 clock edges of the current command word. For read commands, the read data from the current command word appears at DOUT on the last 16 clock edges of the current command word. See Figures 8 and 9.

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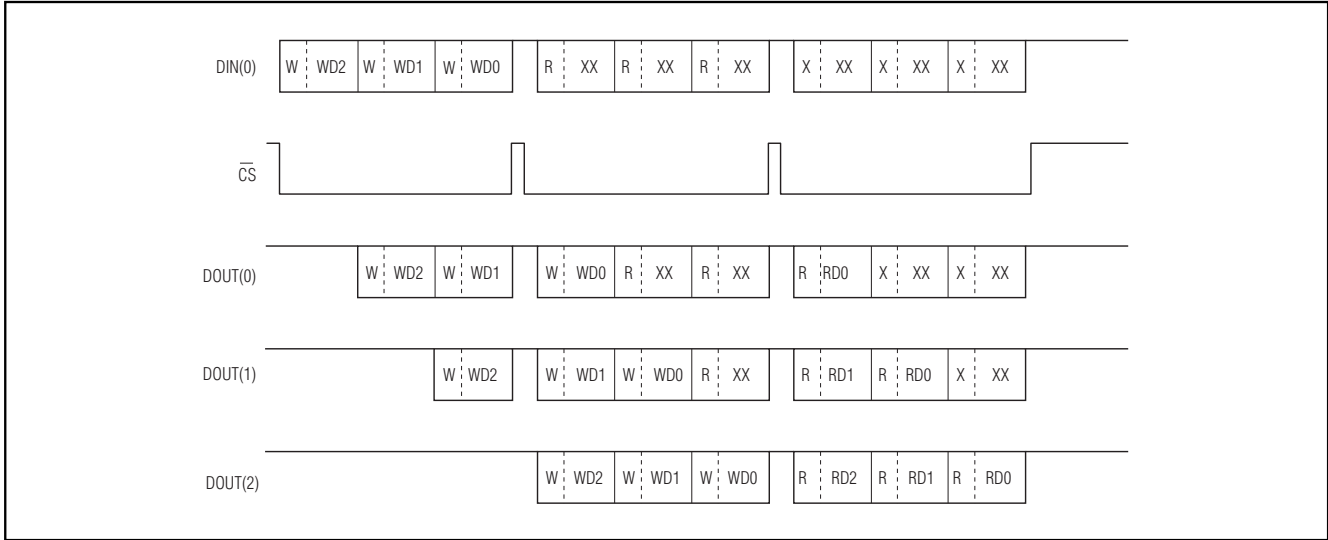


Figure 5. Example 1 of a Daisy-Chain Data Sequence

W/WD0 = 32-bit word with a write command; WD0 writes data for device 0. The 0 refers to the position in the daisy chain (0 is closest to the bus master). Devices 1 and 2 are devices further down the chain.

R/RD2 = 32-bit word with a read command; RD2 reads data from device 2.

X = Don't care (for X in the data or command position).

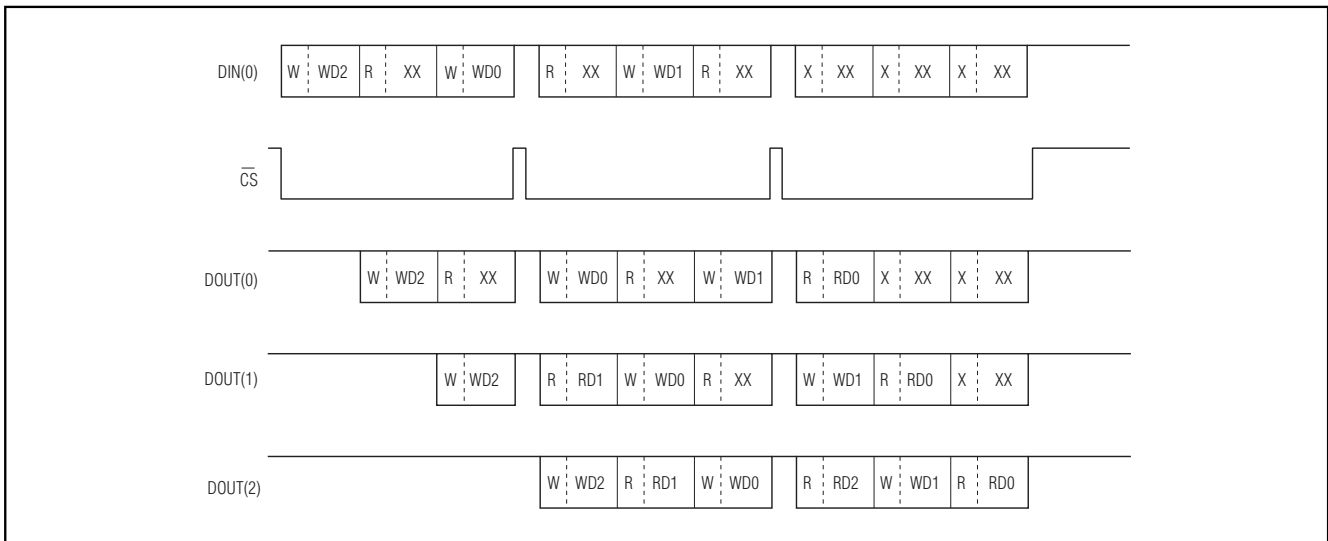


Figure 6. Example 2 of a Daisy-Chain Data Sequence

W/WD0 = 32-bit word with a write command; WD0 writes data for device 0. The 0 refers to the position in the daisy chain (0 is closest to the bus master). Devices 1 and 2 are devices further down the chain.

R/RD2 = 32-bit word with a read command; RD2 reads data from device 2.

X = Don't care (for X in the data or command position).

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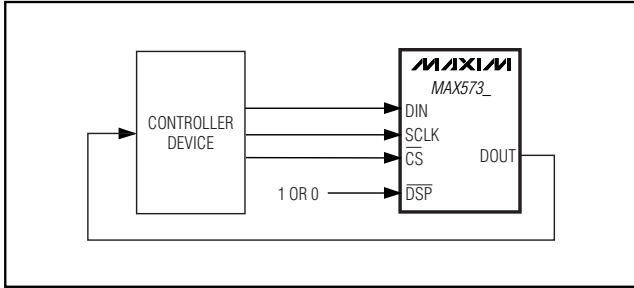


Figure 7. Stand-Alone Configuration

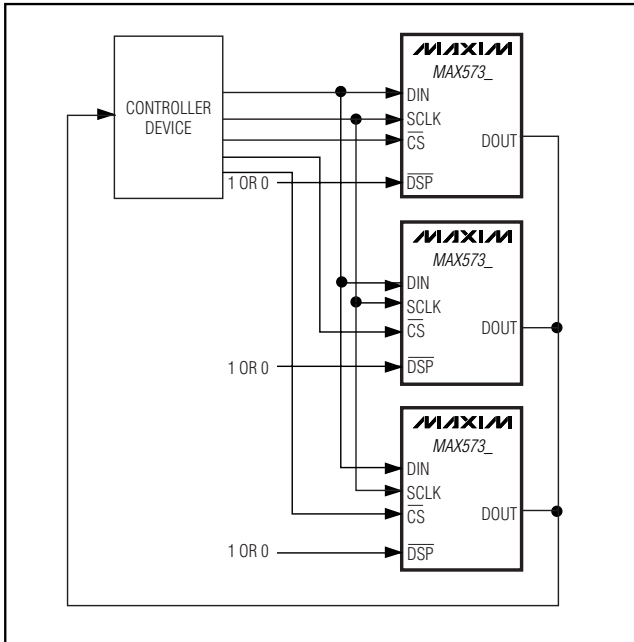


Figure 8. Example of a Parallel Configuration with Read-Back

Read-Data Format

The MAX5732–MAX5735 support daisy-chain connections of multiple devices. The default (power-up) configuration for the MAX5732–MAX5735 assumes that the device may be part of a daisy chain of devices. DOUT follows DIN after 32 clock cycles. For a read command, DOUT provides read data (instead of the data value shifted in) in the next cycle following a \overline{CS} rising edge. Figures 5 and 6 show examples of daisy-chain data sequences.

Shutdown Mode

The MAX5732–MAX5735 feature a software-controlled low-power shutdown mode. When bit 11 of the configuration register is a logic high, the analog section of the device is disabled, and the outputs go high impedance. In shutdown, supply current is reduced to 50 μ A. Data stored in the DAC and input registers is retained, and the device outputs return to their previous values when the device is brought out of shutdown. The serial interface remains active while the device is in shutdown.

Power-Up State

The MAX5732–MAX5735 monitor the four power supplies and maintain the output buffers in a known state until sufficient voltage is available to ensure that no output glitches occur. Once the minimum voltage threshold has been passed, the device outputs come up in the clear state (all outputs = 0). For proper power sequencing, V_{SS} must be applied first. Power sequencing is not necessary if V_{SS} is connected to AGND.

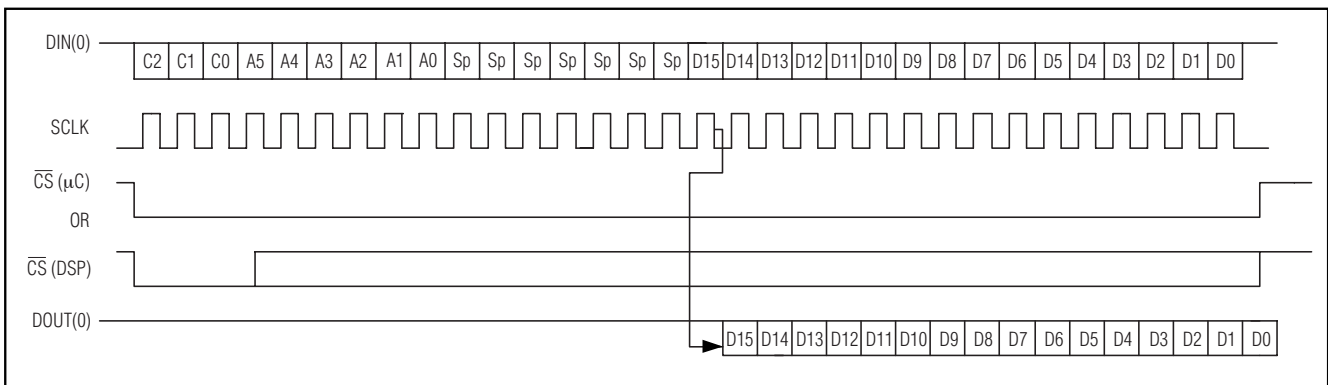


Figure 9. Read Data Timing When Not Daisy Chained

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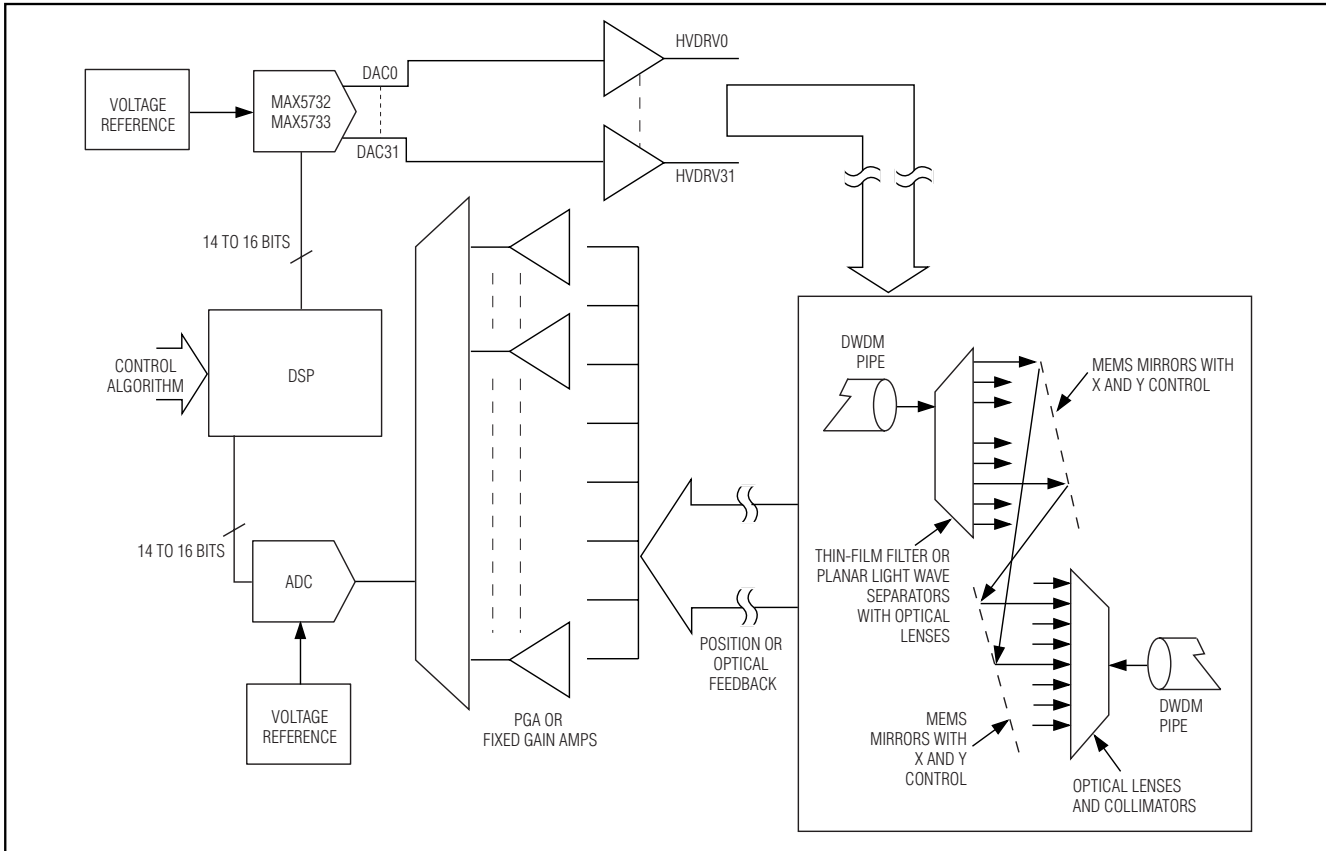


Figure 10. MEMS Mirror Control

Applications Information

MEMS Micromirror Control

The MAX5732/MAX5733 are the highest resolution 32-channel DACs available in the smallest footprint, making the devices ideal for optical MEMS mirror control (Figure 10). A high-resolution DAC forms the core analog block for controlling the X and Y position of the mirror. As the density of the optical cross-connects increases, the number of DAC channels also increases. By offering the highest resolution and the greatest density, the MAX5732/MAX5733 improve performance and reduce the board footprint.

Automatic Test Equipment (ATE) Applications

The MAX5734 includes many features suited for ATE applications. The device is the most compact level-setting solution available for high-density pin electronics boards. The MAX5734 provides a -2.5V to +7.5V output voltage range (required by most ATE applications).

The offset DAC simultaneously adjusts the voltage range of all 32 DACs, allowing optimization to the application. The remote-sense feature allows the pin electronic voltages to be referenced to the ground potential at the DUT site.

The B grade linearity error of $\pm 2.44\text{mV}$ (max) is more than sufficient for most ATE applications. The A grade device cuts this error to $\pm 1.22\text{mV}$ (max) for higher accuracy.

The pipelined register architecture allows all 32 DACs to be updated simultaneously. This is valuable during test setups, as all values in the tester can be set and then updated in unison with a single command. This feature can be accessed through the serial port or the LDAC input.

The low output noise of the MAX5734 allows direct connection to the pin electronics, eliminating the cost and PC board area of external filtering.

Modern pin electronics integrated circuits (PEICs) are typically fabricated on high-speed processes with low

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breakdown voltages. Some devices require external protection on their reference inputs to satisfy absolute maximum ratings. The MAX5734 features outputs that are almost Rail-to-Rail®. This allows the AVCC and VSS supplies to be set to voltages within the absolute maximum ratings of the PEIC. This guarantees that the PEIC is protected in all situations.

Additional protection is provided by the MAX5734 glitch-free power-up into the clear state with all DAC outputs set to approximately 0V. Either the serial port or the $\overline{\text{CLR}}$ input can assert the clear function.

Power Supplies, Bypassing, Decoupling, and Layout

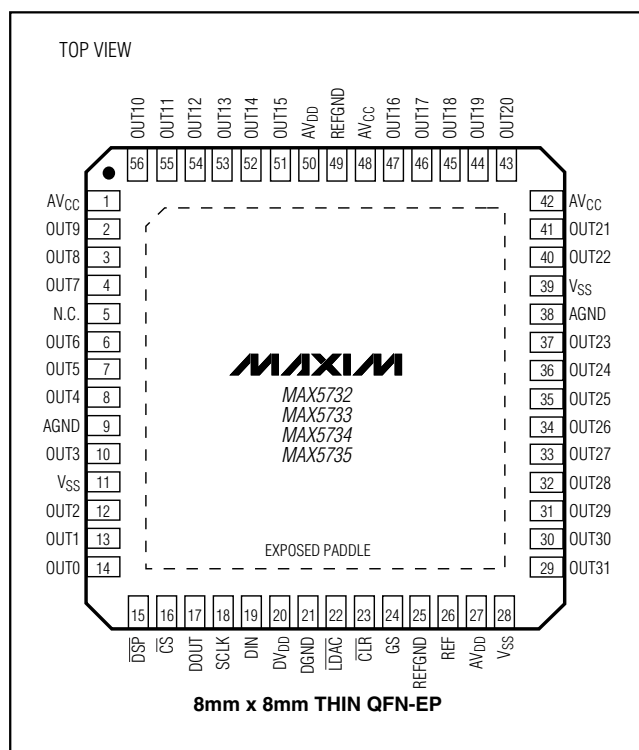
Grounding and power-supply decoupling strongly influence device performance. Digital signals can couple through the reference input, power supplies, and ground connection. Proper grounding and layout can reduce

digital feedthrough and crosstalk. Bypass all power supplies with an additional 0.1 μ F and 1 μ F on each pin, as close to the device as possible. Refer to the MAX5732-MAX5735 evaluation kit for a suggested layout.

The MAX5732-MAX5735 have four separate power supplies. AVDD powers the internal analog circuitry (except for the output buffers) and DVDD powers the digital section of the device. AVCC and VSS power the output buffers.

The MAX5732-MAX5735 feature an exposed paddle on the backside of the package for improved power dissipation. The exposed paddle is electrically connected to VSS, and should be soldered to a large copper plane that shares the same potential. For more information on the exposed paddle QFN package, refer to the following website: <http://pdfserv.maxim-ic.com/arpdf/AppNotes/4hfan081.pdf>

Pin Configuration



Selector Guide

PART	INL (MAX LSB)	OUTPUT VOLTAGE RANGE (V)
MAX5732ACTN	±8	0 to +5
MAX5732BCTN	±16	0 to +5
MAX5732AETN	±8	0 to +5
MAX5732BETN	±16	0 to +5
MAX5733ACTN	±8	0 to +10
MAX5733BCTN	±16	0 to +10
MAX5733AETN	±8	0 to +10
MAX5733BETN	±16	0 to +10
MAX5734ACTN	±8	-2.5 to +7.5
MAX5734BCTN	±16	-2.5 to +7.5
MAX5734AETN	±8	-2.5 to +7.5
MAX5734BETN	±16	-2.5 to +7.5
MAX5735ACTN	±8	-5 to +5
MAX5735BCTN	±16	-5 to +5
MAX5735AETN	±8	-5 to +5
MAX5735BETN	±16	-5 to +5

Chip Information

TRANSISTOR COUNT: 152,000

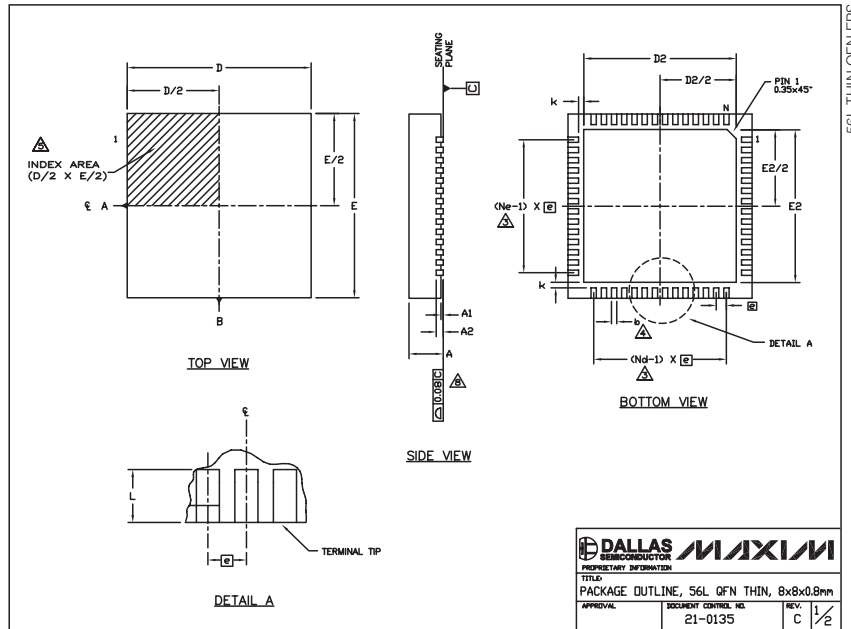
PROCESS: BiCMOS

Rail-to-Rail is a registered trademark of Nippon Motorola, Inc.

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



<small>PROPRIETARY INFORMATION</small>		
<small>TITLE</small> PACKAGE OUTLINE, 56L QFN THIN, 8x8x0.8mm		
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small> 21-0135	<small>REV.</small> C 1/2

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.225mm MAXIMUM (0.009 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE WITHIN HATCHED AREA AS SHOWN. EITHER AN INDENTATION MARK OR INK/LASER MARK IS ACCEPTABLE.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. PACKAGE WARPAGE MAX 0.01mm.
8. APPLIES TO EXPOSED PAD AND TERMINALS. EXCLUDES INTERNAL DIMENSION OF EXPOSED PAD.
9. MEETS JEDEC MO220.

DIM.	56L 8x8			UNIT
	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
b	0.20	0.25	0.30	4
D	7.90	8.00	8.10	
E	7.90	8.00	8.10	
REF	0.50 BSC			
N	56			3
Nd	14			3
Ne	14			3
L	0.30	0.40	0.50	
A1	0.00	0.02	0.05	
A2	0.20 REF			
k	0.25	--	--	

PKG. CODE	EXPOSED PAD VARIATION						JEDEC
	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T5688-1	6.50	6.65	6.70	6.50	6.65	6.70	WLD-5

<small>PROPRIETARY INFORMATION</small>		
<small>TITLE</small> PACKAGE OUTLINE, 56L QFN THIN, 8x8x0.8mm		
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small> 21-0135	<small>REV.</small> C 2/2

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