

MAXIM

Low-Cost μ P Supervisory Circuits with Battery Backup

MAX703/MAX704

General Description

The MAX703 and MAX704 microprocessor (μ P) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in μ P systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX703/MAX704 are available in 8-pin DIP and SO packages and provide four functions:

- 1) An active-low reset during power-up, power-down, and brownout conditions.
- 2) Battery-backup switching for CMOS RAM, CMOS μ Ps, or other low-power logic circuitry.
- 3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
- 4) An active-low manual-reset input.

The MAX703 and MAX704 differ only in their supply-voltage monitor levels. The MAX703 generates a reset when the supply drops below 4.65V, while the MAX704 generates a reset below 4.4V.

Applications

- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical μ P Power Monitoring

Features

- ◆ Battery-Backup Power Switching
- ◆ Precision Supply-Voltage Monitor
4.65V (MAX703)
4.40V (MAX704)
- ◆ 200ms Reset Pulse Width
- ◆ Debounced TTL-/CMOS-Compatible Manual-Reset Input
- ◆ 200 μ A Quiescent Current
- ◆ 50nA Quiescent Current in Battery-Backup Mode
- ◆ Voltage Monitor for Power-Fail or Low-Battery Warning
- ◆ 8-Pin DIP and SO Packages
- ◆ Guaranteed RESET Assertion to $V_{CC} = 1V$

Ordering Information

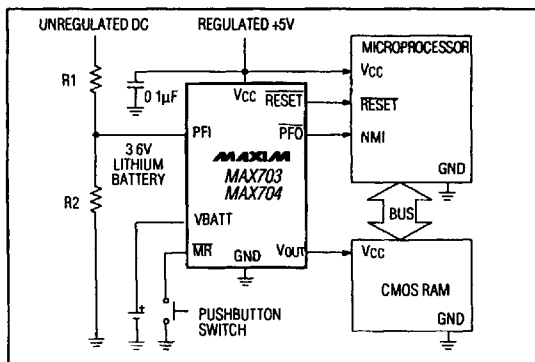
PART	TEMP. RANGE	PIN-PACKAGE
MAX703CPA	0°C to +70°C	8 Plastic DIP
MAX703CSA	0°C to +70°C	8 SO
MAX703C/D	0°C to +70°C	Dice*
MAX703EPA	-40°C to +85°C	8 Plastic DIP
MAX703ESA	-40°C to +85°C	8 SO
MAX703MJA	-55°C to +125°C	8 CERDIP**

Ordering information continued on last page.

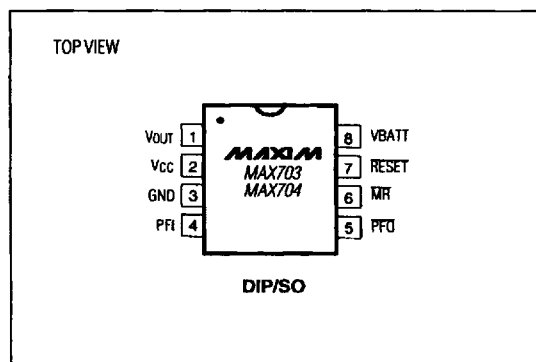
* Dice are tested at $T_A = +25^\circ\text{C}$ only.

** Contact factory for availability and processing to MIL-STD-883

Typical Operating Circuit



Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)		Rate-of-Rise, VCC, VBATT	100V/ μ s
VCC	-0.3V to 6.0V	Continuous Power Dissipation (TA = +70°C)	
VBATT	-0.3V to 6.0V	Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
All Other Inputs (Note 1)	-0.3V to (VCB + 0.3V)	SO (derate 5.88mW/°C above +70°C)	471mW
Input Current		CERDIP (derate 8.00mW/°C above +70°C)	640mW
VCC	200mA	Operating Temperature Ranges:	
VBATT	50mA	MAX70_C_	0°C to +70°C
GND	20mA	MAX70_E_	-40°C to +85°C
Output Current		MAX70_MJA	-55°C to +125°C
VOUT	Short-Circuit Protected for up to 10 sec	Storage Temperature Range	-65°C to +160°C
All Other Outputs	20mA	Lead Temperature (soldering, 10 sec)	+300°C

Note 1: VCB is the greater of VCC and VBATT. The input voltage limits on PFI and \overline{MR} may be exceeded if the current into these pins is limited to less than 10mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

(VCC = +4.75V to +5.5V for MAX703, VCC = +4.5V to +5.5V for MAX704, VBATT = 2.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOLS	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Voltage Range VCC, VBATT (Note 2)			0		5.5	V	
Supply Current (Excluding IOUT)	ISUPPLY	MAX70_C		200	350	μ A	
		MAX70_E/M		200	500	μ A	
ISUPPLY in Battery-Backup Mode (Excluding IOUT)		VCC = 0V, VBATT = 2.8V	TA = +25°C	0.05	1.0	μ A	
			TA = TMIN to TMAX		5.0	μ A	
VBATT Standby Current (Note 3)		5.5V > VCC > VBATT + 0.2V	TA = +25°C	-0.1	0.02	μ A	
			TA = TMIN to TMAX	-1.0	0.02	μ A	
VOUT Output		IOUT = 5mA	VCC-0.05	VCC-0.025		V	
		IOUT = 50mA	VCC-0.5	VCC-0.25		V	
VOUT in Battery-Backup Mode		IOUT = 250 μ A, VCC < VBATT-0.2V	VBATT-0.1	VBATT-0.02		V	
Battery-Switch Threshold (VCC - VBATT)		VCC < VRST	Power-Up	20		mV	
			Power-Down	-20		mV	
Battery-Switchover Hysteresis				40		mV	
RESET Threshold	VRST	MAX703	4.50	4.65	4.75	V	
		MAX704	4.25	4.40	4.50	V	
RESET Threshold Hysteresis				40		mV	
RESET Pulse Width	trST		140	200	280	ms	
RESET Output Voltage	VOH	ISOURCE = 800 μ A	VCC-1.5			V	
	VOL	ISINK = 3.2mA		0.4			
		MAX70_C, VCC = 1V, VCC falling, VBATT = 0V, ISINK = 50 μ A			0.3		
		MAX70_E/M, VCC = 1.2V, VCC falling, VBATT = 0V, ISINK = 100 μ A			0.3		

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +4.75V$ to $+5.5V$ for MAX703, $V_{CC} = +4.5V$ to $+5.5V$ for MAX704, $V_{BATT} = 2.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

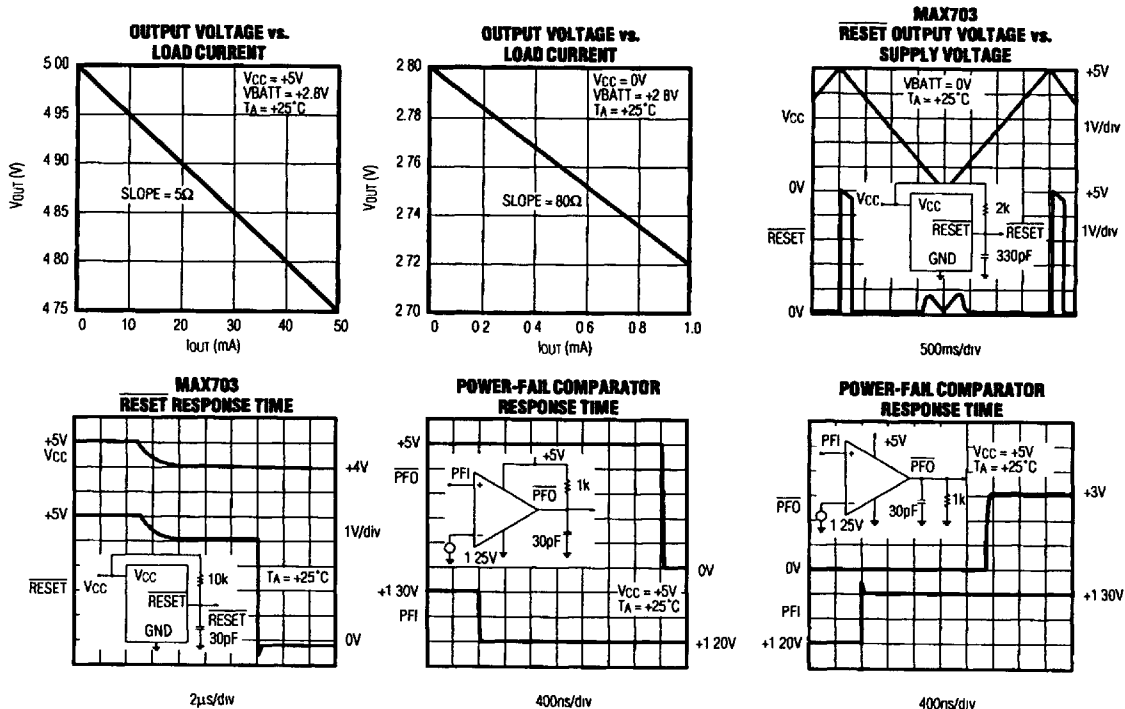
PARAMETER	SYMBOLS	CONDITIONS	MIN	TYP	MAX	UNITS
MR Input Threshold	V_{IL}				0.8	V
MR Pulse Width	tMR		150			ns
MR to RESET Delay	tMD				250	ns
MR Pull-Up Current		$\overline{MR} = 0V$	100	250	600	μA
PFI Input Threshold		$V_{CC} = 5V$	1.20	1.25	1.30	V
PFI Input Current			-25	0.01	25	nA
PFO Output Voltage	V_{OH}	$I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$			V
	V_{OL}	$I_{SINK} = 3.2mA$			0.4	

Note 2: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2.0V.

Note 3: "-" = battery-charging current, "+" = battery-discharging current.

Typical Operating Characteristics

($V_{CC} = +5V$, $V_{BATT} = +2.8V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN	NAME	FUNCTION
1	V _{OUT}	Supply Output for CMOS RAM. When V _{CC} is above the reset threshold, V _{OUT} connects to V _{CC} through a P-channel MOSFET switch. When V _{CC} is below the reset threshold, the higher of V _{CC} or V _{BATT} is connected to V _{OUT} .
2	V _{CC}	+5V Supply Input
3	GND	Ground
4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, P _{FO} goes low, otherwise P _{FO} remains high. Connect PFI to GND or V _{CC} when not used.
5	P _{FO}	Power-Fail Output goes low and sinks current when PFI is less than 1.25V, otherwise P _{FO} remains high.
6	M _R	Manual-Reset Input generates a reset pulse when pulled below 0.8V. This active-low input is TTL/CMOS compatible and can be shorted to ground with a switch. It has an internal 250 μ A pull-up current. Leave floating when not used.
7	RESET	Reset Output remains low while V _{CC} is below the reset threshold (4.65V for the MAX703, 4.40V for the MAX704). It remains low for 200ms after V _{CC} rises above the reset threshold (Figure 2) or M _R goes from low to high.
8	V _{BATT}	Backup-Battery Input. When V _{CC} falls below the reset threshold, V _{BATT} is switched to V _{OUT} if V _{BATT} is 20mV greater than V _{CC} . When V _{CC} rises 20mV above V _{BATT} , V _{CC} is switched to V _{OUT} . The 40mV hysteresis prevents repeated switching if V _{CC} fails slowly.

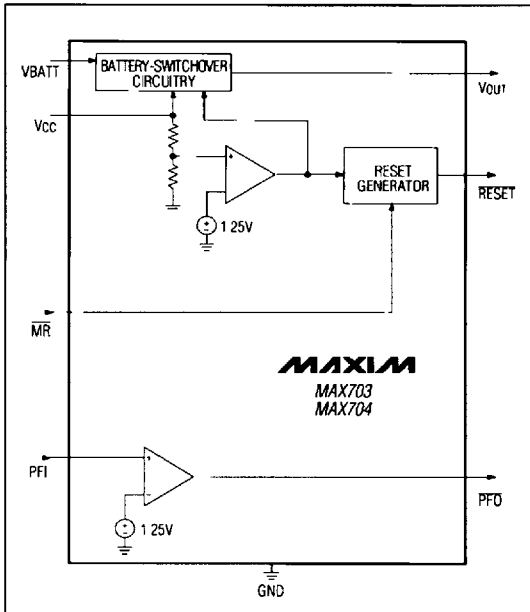


Figure 1 Block Diagram

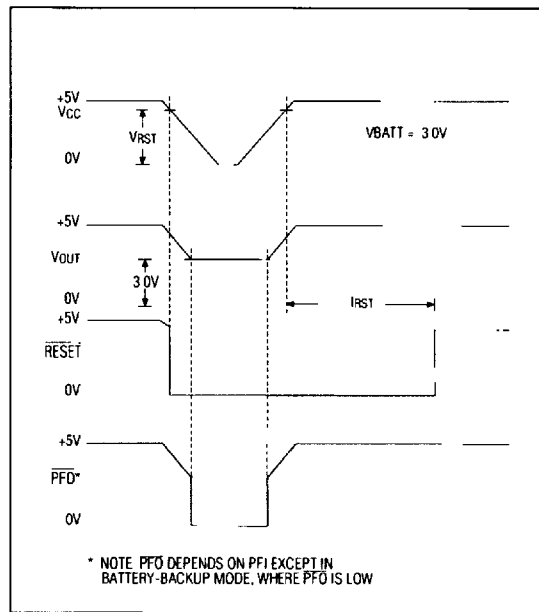


Figure 2 Timing Diagram

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MAX703/MAX704

Detailed Description

RESET Output

A μ P's reset input starts the μ P in a known state. Whenever the μ P is in an unknown state, it should be held in reset. The MAX703/MAX704 assert reset when VCC is low, preventing code-execution errors during power-up, power-down, or brownout conditions.

When VBATT is 2V or more, RESET is always valid, irrespective of VCC. On power-up, as VCC rises, RESET remains low. When VCC exceeds the reset threshold, an internal timer holds RESET low for a time equal to the reset pulse width (typically 200ms), after this interval, RESET goes high (Figure 2). If a power-fail or brownout condition occurs (i.e. VCC drops below the reset threshold), RESET is asserted. As long as VCC remains below the reset threshold, the internal timer is continually restarted, causing the RESET output to remain low. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the end of the last interruption.

Power-Fail Comparator

The PFI input is compared to an internal reference. If PFI is less than 1.25V, PFO goes low. The power-fail comparator can be used as an undervoltage detector to signal a failing power supply. In the *Typical Operating Circuit*, an external voltage divider at PFI is used to monitor the unregulated DC voltage from which the regulated +5V supply is derived.

The voltage divider can be chosen so the voltage at PFI falls below 1.25V just before the +5V regulator drops out. PFO is then used as an interrupt to prepare the μ P for power-down.

To conserve power, the power-fail comparator is turned off and PFO is forced low when the MAX703/MAX704 enter battery-backup mode.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at VBATT, the MAX703/MAX704 automatically switch RAM to backup power when VCC fails.

As long as VCC exceeds the reset threshold, VCC connects to VOUT through a 5 Ω P-channel MOSFET power switch. Once VCC falls below the reset threshold, RESET goes low and VCC or VBATT (whichever is higher) switches to VOUT. Note that VBATT switches to VOUT (through an 80 Ω switch) only if VCC is below the reset-threshold voltage and VBATT is greater than VCC. When VCC exceeds the reset threshold, it is connected to the MAX703/MAX704 substrate, regardless of the voltage

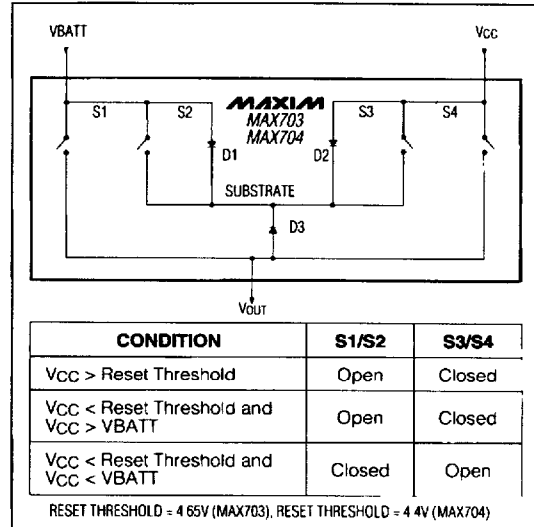


Figure 3. Backup-Battery Switchover Block Diagram

applied to VBATT (Figure 3). During this time, diode D1 (between VBATT and the substrate) conducts current from VBATT to VCC if VBATT \geq (VCC + 0.6V).

When the battery-backup mode is activated, VBATT connects to VOUT. In this mode, the substrate connects to VBATT and internal circuitry is powered from the battery (Figure 3). Table 1 shows the status of the MAX703/MAX704 inputs and outputs in battery-backup mode.

When VCC is below, but within, 1V of VBATT, the internal switchover comparator draws about 30 μ A. Once VCC drops to more than 1V below VBATT, the internal switchover comparator shuts off and the supply current falls to less than 1 μ A.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
VCC	Disconnected from VOUT
VOUT	Connected to VBATT through an internal 80 Ω P-channel MOSFET switch
VBATT	Connected to VOUT. Supply current is < 1 μ A when VCC < (VBATT - 1V)
RESET	Logic low
PFI	Power-fail comparator is disabled.
PFO	Logic low
MR	Disabled

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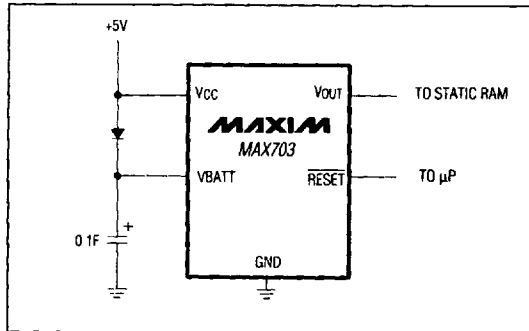


Figure 4. Using a SuperCap as a Backup Power Source with a MAX703 and a +5V \pm 5% Supply

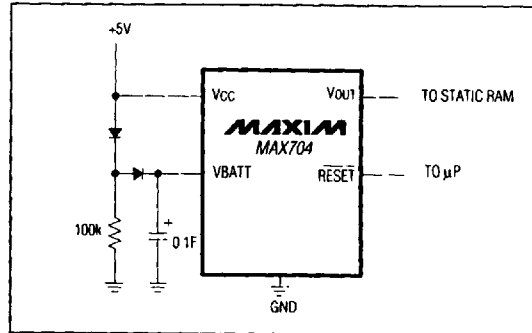


Figure 5. Using a SuperCap as a Backup Power Source with the MAX704 and a +5V \pm 10% Supply

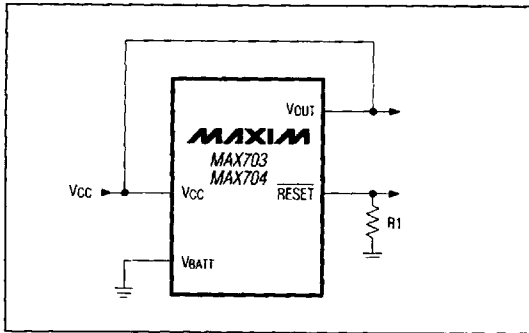


Figure 6. RESET Valid to Ground Circuit

Manual Reset

The manual-reset input (\overline{MR}) allows RESET to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. Because it is TTL/CMOS compatible, \overline{MR} can be driven by an external logic line.

Applications Information

Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values (on the order of 0.1 Farad). When using SuperCaps, if V_{CC} exceeds the MAX703/MAX704 reset thresholds (4.65V and 4.40V, respectively), V_{BATT} may not exceed V_{CC} by more than 0.6V. Thus, with a 5% tolerance on V_{CC} , V_{BATT} should not exceed $V_{CC}(\text{min}) + 0.6V = 5.35V$. Similarly, with a 10% tolerance on V_{CC} , V_{BATT} should not exceed 5.1V.

TM SuperCap is a registered trademark of Baknor Industries.

Figure 4's SuperCap circuit uses the MAX703 with a \pm 5% tolerance voltage supply. In this circuit, the SuperCap rapidly charges to within a diode drop of V_{CC} . However, the diode leakage current will trickle-charge the SuperCap voltage to V_{CC} . If $V_{BATT} = 5.25V$ and the power is suddenly removed and then reapplied with $V_{CC} = 4.75V$, $V_{BATT} - V_{CC}$ does not exceed the allowable 0.6V difference voltage.

Figure 5's circuit uses the MAX704 with a \pm 10% tolerance voltage supply. Note that if $V_{CC} = 5.5V$ and $V_{BATT} \leq 5.1V$, the power can be suddenly removed and reapplied with $V_{CC} = 4.95V$, and $(V_{BATT} - V_{CC})$ will not exceed the allowable 0.6V voltage difference.

Batteries and Power Supplies as Backup Power Sources

Lithium batteries work well as backup batteries because they have very low self-discharge rates and high-energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal for use with the MAX703/MAX704. Batteries with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be directly connected to the MAX703/MAX704 V_{BATT} input with no additional circuitry (see Typical Operating Circuit).

However, batteries with open-circuit voltages greater than the reset threshold plus 0.3V CANNOT be used as backup batteries, since they source current into the substrate through diode D1 (Figure 3) when V_{CC} is close to the reset threshold.

Table 2. Allowable Backup-Battery Voltages

PART NO.	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX703	4.80
MAX704	4.55

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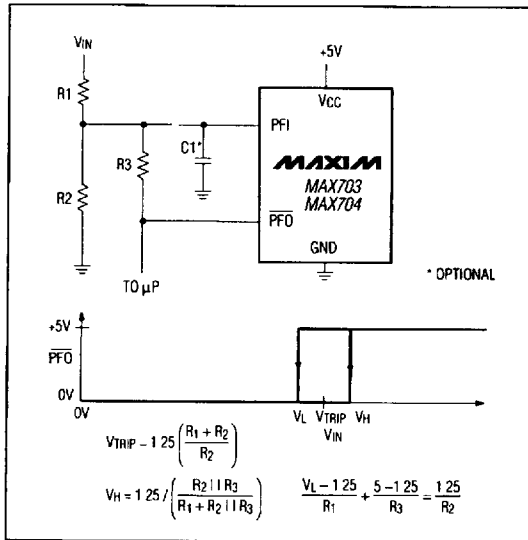


Figure 7. Adding Hysteresis to the Power-Fail Comparator

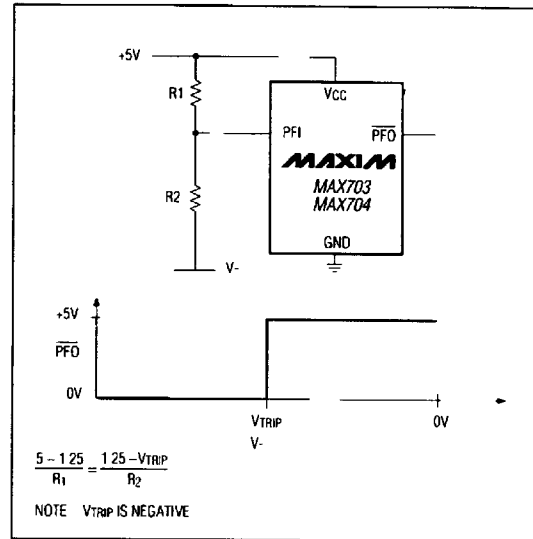


Figure 8. Monitoring a Negative Voltage

Using the MAX703/MAX704 Without a Backup Power Source

If a backup power source is not used, ground VBATT and connect VCC to VOUT. A direct connection to VCC eliminates any voltage drop across the internal switch, which would otherwise appear at VOUT. Alternatively, use the MAX705-MAX708, which do not have battery-backup capabilities.

Ensuring a Valid RESET Output Down to VCC = 0V

When VCC falls below 1V, the MAX703/MAX704 RESET output no longer sinks current; it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pull-down resistor is added to the RESET pin as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding RESET low. Resistor value R1 is not critical. It should be about 100k Ω , which is large enough not to load RESET and small enough to pull RESET to ground.

Replacing the Backup Battery

The backup battery can be removed while VCC remains valid without triggering a reset. As long as VCC stays above the reset threshold, battery-backup mode cannot be entered. This is an improvement on switchover ICs that initiate a reset when VCC and VBATT are at or near the same voltage level (regardless of the reset-threshold

voltage). If the voltage on the unconnected VBATT pin floats up toward VCC, this condition alone cannot initiate a reset when using the MAX703/MAX704.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when VIN is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1 μ A to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10k Ω to prevent it from loading down the PFO pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 8's circuit. When the negative supply is valid, PFO is low. When the negative supply voltage droops, PFO goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the VCC voltage, and resistors R1 and R2.

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Using the Power-Fail Comparator to Assert Reset

In addition to asserting reset at the VCC reset threshold voltage, reset can also be asserted at the PFI input threshold voltage. Connect PFO to MR to initiate a reset pulse when the monitored supply drops below a user-

specified threshold or when VCC falls below the reset threshold. For additional noise rejection, place a capacitor between PFI and GND.

Table 3. Maxim μ P Supervisory Products

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	CE Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt On Output
MAX690A	4.65	140	1.6	yes	no	yes	no	no	no	no	no
MAX691A	4.65	140/adj	1.6/adj	yes	yes	yes	no	yes	yes	yes	yes
MAX692A	4.40	140	1.6	yes	no	yes	no	no	no	no	no
MAX693A	4.40	140/adj	1.6/adj	yes	yes	yes	no	yes	yes	yes	yes
MAX696	adj.	35/adj.	1.6/adj.	yes	no	yes	no	yes	yes	yes	yes
MAX697	adj.	35/adj.	1.6/adj.	no	yes	yes	no	yes	yes	yes	no
MAX700	4.65/adj.	200	NA	no	no	no	yes	no	no	yes	no
MAX703	4.65	140	NA	yes	no	yes	yes	no	no	no	no
MAX704	4.40	140	NA	yes	no	yes	yes	no	no	no	no
MAX705	4.65	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706	4.40	140	1.6	no	no	yes	yes	yes	no	no	no
MAX707	4.65	140	NA	no	no	yes	yes	no	no	yes	no
MAX708	4.40	140	NA	no	no	yes	yes	no	no	yes	no
MAX791	4.65	140	1	yes	yes	yes	yes	yes	yes	yes	yes
MAX1232	4.50/4.75	250	0.15/0.60/1.2	no	no	no	yes	no	no	yes	no
MAX1259	NA	NA	NA	yes	no	yes	no	no	no	no	no

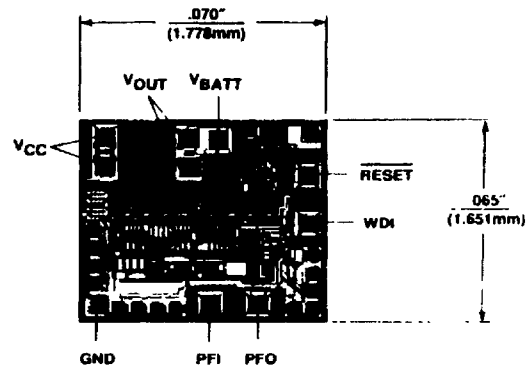
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX704CPA	0°C to +70°C	8 Plastic DIP
MAX704CSA	0°C to +70°C	8 SO
MAX704C/D	0°C to +70°C	Dice*
MAX704EPA	-40°C to +85°C	8 Plastic DIP
MAX704ESA	-40°C to +85°C	8 SO
MAX704MJA	-55°C to +125°C	8 CERDIP**

* Dice are tested at T_A = +25°C only

** Contact factory for availability and processing to MIL-STD-883

Chip Topography



SUBSTRATE MUST BE LEFT UNCONNECTED
TRANSISTOR COUNT 573

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