PM5343

STXC

SONET/SDH TRANSPORT OVERHEAD TRANSCEIVER TELECOM STANDARD PRODUCT

DATA SHEET

ISSUE 6: SEPTEMBER 1998

REVISION HISTORY

Issue No.	Issue Date	Details of Change
Issue 6	September, 1998	1. Name of PECL input parameter changed from VPIA to VPSWG. Spec. revised to 550 mV to reflect characterization results 2. Clarified usage of MBEB and CSB signals in test feature description section. 3. Clarified conditions required for test mode 0 access to RIN and SCPI/SCPO signals 4. Improved description of register 1AH. 5. Pin descriptions for GRICLK/RICLK and GTICLK/TICLK in bit-serial mode was improved. 6. Bit error rate tables added to meet ITU specs. 7. IDDOP2 spec improved 8. TIFP pin description corrected. 9. Changed lead temperature max rating to 230 deg 10. Changed all references from PQFP to more technically correct MQFP. 11. Changed PECL pin types from Input and Output to PECL Input and PECL output.
Issue 5	September, 1997	Re-formatted to fit new template.

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1 FEATURES

- Monolithic SONET/SDH Transport Overhead Terminating Transceiver for use in STS-1, STS-3 or STM-1 interface applications, operating at serial interface speeds of up to 155.52 Mbit/s.
- Provides termination for SONET Section and Line, and SDH Regenerator Section and Multiplexer Section transport overhead.
- Companion to the PM5344 SPTX SONET/SDH Path Terminating Transceiver.
- Operates in STS-1 and STS-3 bit-serial (PECL/TTL I/O) and byte-serial (TTL I/O) modes. Provides independent control of the transmit and receive operating modes for asymmetrical bandwidth applications.
- Frames to the STS-1 or STS-3 (STM-1) receive stream and inserts the framing bytes (A1, A2) and the STS identification bytes (J0) into the transmit stream; Descrambles the receive stream and scrambles the transmit stream.
- Calculates and compares the bit interleaved parity error detection codes (B1, B2) for the receive stream and calculates and inserts B1 and B2 in the transmit stream.
- Accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the Z2 growth byte based on received B2 errors.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.
- Optionally inserts the line BIP-8 error detection code into each of the constituent STS-1s (B2 bytes) of the transmit STS-1/3 stream.
- Extracts and serializes the order wire channels (E1, E2), the data communication channels (D1-D3, D4-D12) and the section user channel (F1) from the receive stream, and inserts the corresponding signals into the transmit stream.
- Extracts and serializes the automatic protection switch (APS) channel (K1, K2) bytes, filtering and extracting them into internal registers. Inserts the APS channel into the transmit stream.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI), line alarm indication signal (AIS), and protection switching byte failure alarms.

- Inserts and extracts a 64 byte or 16 byte section trace (J0) message using an internal register bank. Detects an unstable section trace message or mismatch with an expected message, and inserts Line AIS upon either of these conditions.

- Inserts RDI and AIS in the transmit stream.

- Provides loss of signal insertion, framing pattern error insertion, and coding violation insertion (B1 and B2) for diagnostic purposes. B1 and B2 errors can also be generated "on-the-fly" using an error insertion mask.

- Provides a transmit and receive ring control port, allowing alarm and maintenance signal control and status to be passed between mate STXCs for ring-based add drop multiplexer applications.

- Low power +5 Volt 0.8 micron CMOS. Device has PECL and TTL compatible inputs and outputs.

- 160 pin copper leadframe MQFP package. Supports Industrial Temperature Range (-40°C to 85°C) operation.

2 APPLICATIONS

- OC-N Regenerators
- OC-N to OC-M multiplexers
- SONET/SDH add drop multiplexers
- SONET/SDH terminal multiplexers
- Broadband ISDN user network interfaces
- SONET/SDH test equipment

3 REFERENCES

1. American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1991.

2. Committee T1 Contribution, "Draft of T1.105 - SONET Rates and Formats", T1X1.5/94-033R2-1994.

3. ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.

4. American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification - Supplement, ANSI T1.105a-1991.

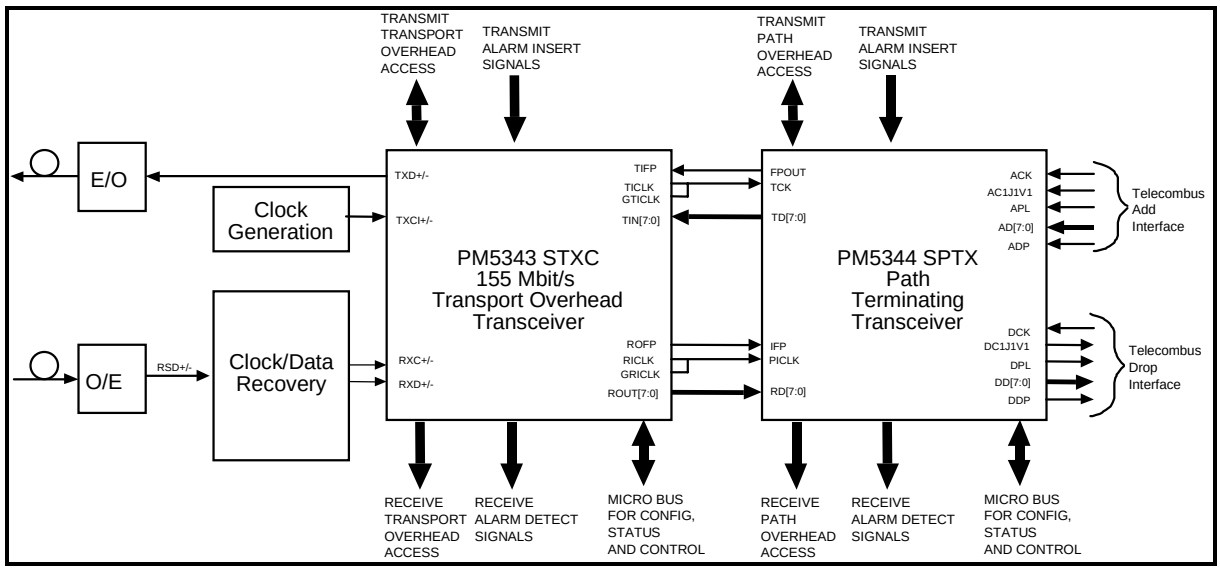
5. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE Issue 2, December, 1995.

10. ETSI DE/TM1015, "Generic Functional Requirement for SDH Transmission Equipment", Version 0.4, February 1993.

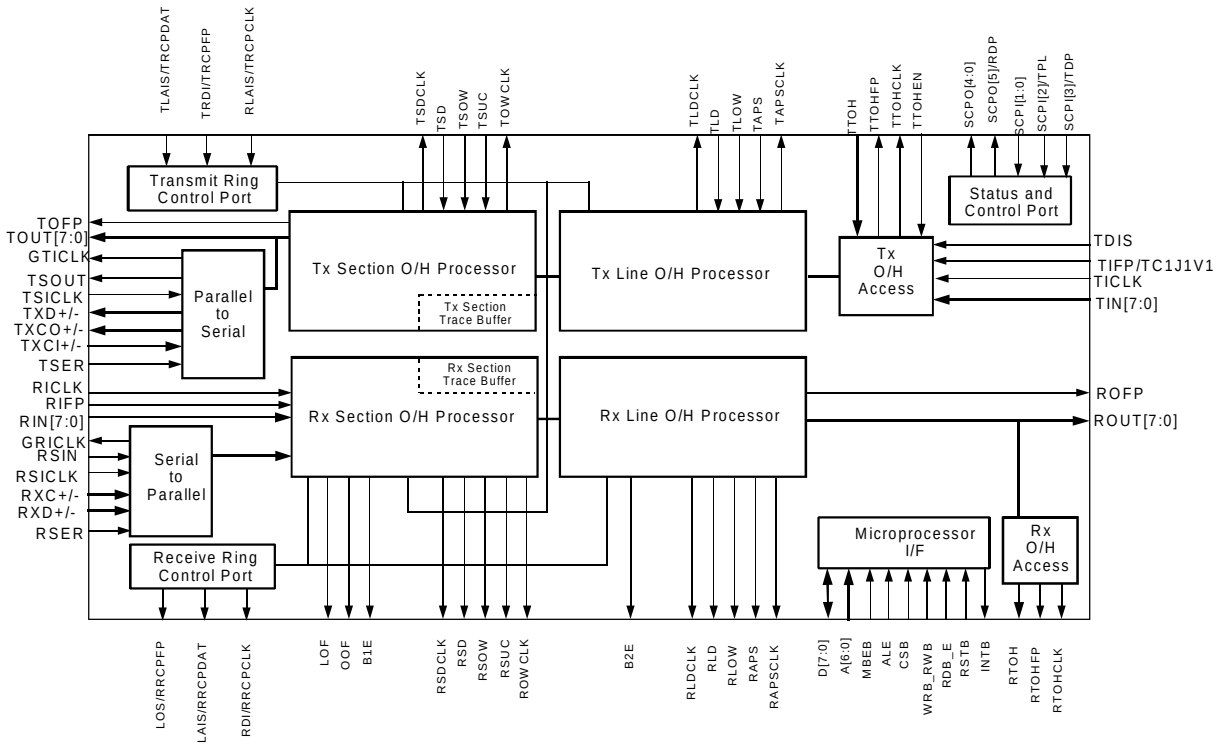
4 APPLICATION EXAMPLE

The STXC is typically used to implement a portion of an STS-3/STM-1 line Interface. The STXC may find application in many different types of SONET/SDH network elements including switches, terminal multiplexers, and add-drop multiplexers. In such applications, the STXC typically interfaces on its line side with a clock and data recovery device (for the receiver) and a physical media device such as a laser (for the transmitter). The system side interfaces directly to the PM5344 SONET/SDH Path Terminating Transceiver (SPTX) where pointer processing and path overhead termination are performed for an STS-3/STM-1 stream. The initial configuration and ongoing control and monitoring of the STXC are normally provided via a generic microprocessor interface.

Figure 1 - STS-3/STM-1 Line Interface



5 BLOCK DIAGRAM



6 DESCRIPTION

The PM5343 SONET/SDH 155 Mbit/s Transport Overhead Terminating Transceiver (STXC) processes the transport overhead (section overhead) of STS-1, and STS-3 (STM-1) streams at 51.84 Mbit/s and 155.52 Mbit/s. The STXC implements significant functions for a SONET/SDH compliant line interface.

The STXC receives SONET/SDH frames via a bit serial or byte serial interface and processes section (regenerator section) and line (multiplexer section) overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section and line path bit interleaved parity (B1, B2), accumulating error counts at each level for performance monitoring purposes. B2 errors are also monitored to detect signal fail and signal degrade threshold crossing alarms. Line remote error indications (M1) are also accumulated. A 16 or 64 byte section trace (J0) message may be buffered and compared against an expected message.

The STXC also provides convenient access to all transport overhead bytes, which are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead.

The STXC transmits SONET/SDH frames, via a bit serial or a byte serial interface, and formats section and line overhead appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section and line bit interleaved parity (B1, B2) as required to allow performance monitoring at the far end. Line remote error indications (M1) are optionally inserted. A 16 or 64 byte section trace (J0) message may be inserted.

The STXC also provides convenient access to all transport overhead bytes, which are optionally inserted from lower rate serial interfaces, allowing external sourcing of overhead. The STXC also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors and bit interleaved parity errors, which are useful for system diagnostics and tester applications.

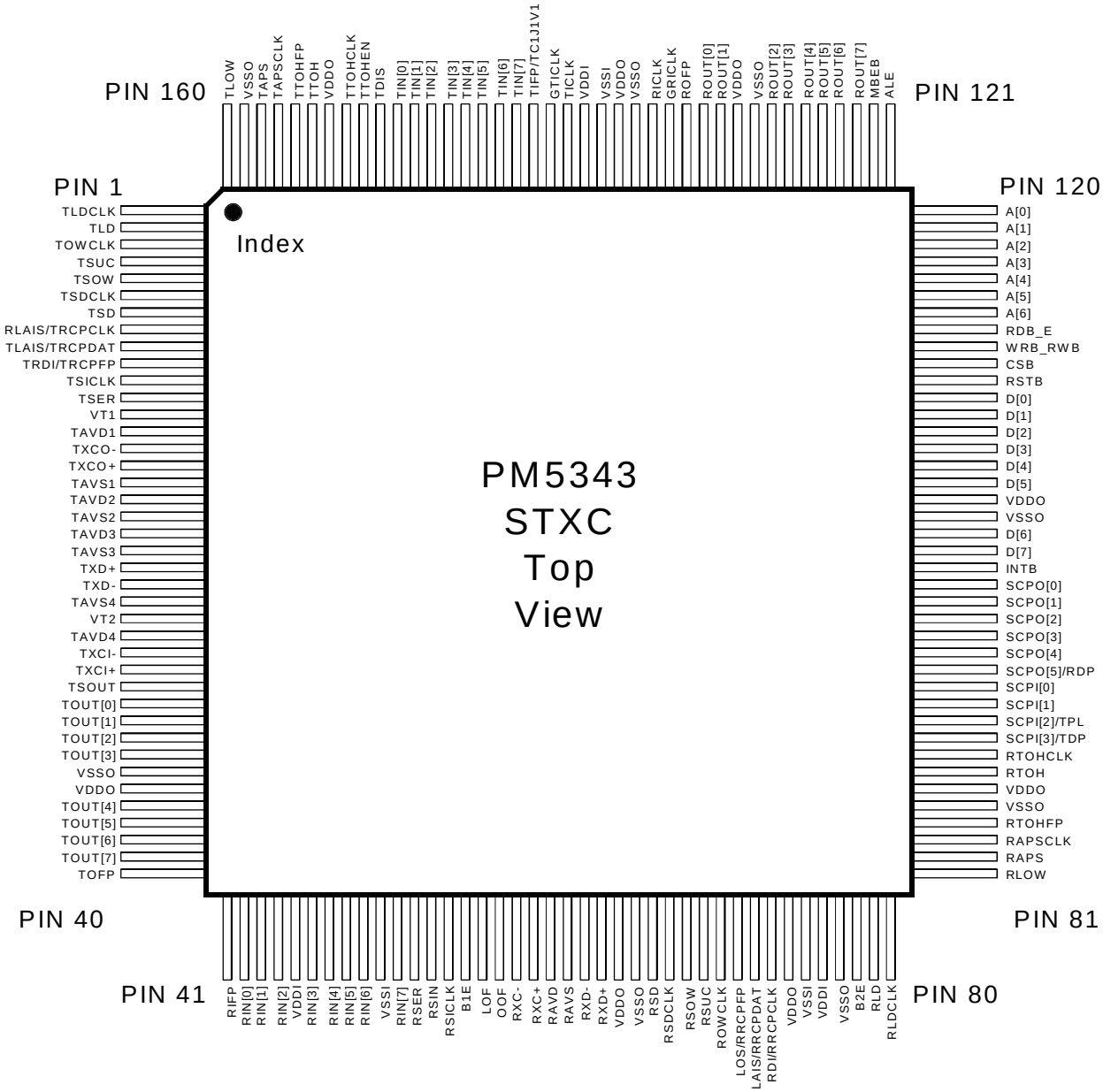
Ring control ports provide the ability to pass control and status information between mate transceivers.

The transmitter and receiver are independently configurable to allow for asymmetric interfaces. The STXC is configured, controlled and monitored via a generic 8-bit microprocessor bus interface.

The STXC is implemented in low power, +5 Volt, CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 160 pin MQFP package.

7 PIN DIAGRAM

The STXC is available in a 160 pin MQFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.65 mm.



8 PIN DESCRIPTION

Pin Name	Pin Type	Pin No.	Function
RSER	Input	52	The receive serial input (RSER) selects the receive line interface. RSER is tied high to select the bit serial interface on PECL pins RXC+, RXC-, RXD+, and RXD-. A TTL interface is also supported in STS-1 mode on pins RSIN and RSICLK. RSER is tied low to select the byte serial interface (on pins RICLK, RIN[7:0], and RIFP).
RICLK/	Input	135	The receive incoming clock (RICLK) provides timing for processing the byte serial receive stream, RIN[7:0]. RICLK is nominally a 6.48 MHz (STS-1), or 19.44 MHz (STS-3/STM-1) 50% duty cycle clock, depending on the selected operating mode. RIN[7:0], and RIFP are sampled on the rising edge of RICLK. RICLK must be externally shorted directly to GRICLK when processing a bit serial receive stream.
RVCLK			The receive vector clock (RVCLK) is used during STXC production test to verify internal functionality.
RIN[7]	Input	51	The receive incoming stream (RIN[7:0]) carries the scrambled STS-1 or STS-3/STM-1 stream in byte serial format. RIN[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). RIN[0] is the least significant bit (corresponding to bit 8 of each serial PCM word, the last bit transmitted). RIN[7:0] is sampled on the rising edge of RICLK.
RIN[6]	Input	49	
RIN[5]	Input	48	
RIN[4]	Input	47	
RIN[3]	Input	46	
RIN[2]	Input	44	
RIN[1]	Input	43	
RIN[0]	Input	42	

Pin Name	Pin Type	Pin No.	Function
RIFP	Input	41	The active high receive incoming framing position (RIFP) signal indicates when the first byte of the synchronous payload envelope is available on the RIN[7:0] inputs. RIFP is sampled on the rising edge of RICLK.
RSIN	Input	53	The receive incoming serial stream (RSIN) contains the TTL compatible 51.84 Mbit/s receive STS-1 stream. RSIN is sampled on the rising edge of RSICLK. The RSIN input has an integral pull down resistor. The RXD+/- inputs may also carry the receive STS-1 stream.
RSICLK	Input	54	The receive serial incoming clock (RSICLK) provides timing for processing the bit serial receive stream, RSIN when the TTL bit serial STS-1 mode is selected. RSICLK is nominally a 51.84 MHz, 50% duty cycle clock. RSIN is sampled on the rising edge of RSICLK. RSICLK is divided by eight to produce GRICLK when the TTL bit serial STS-1 mode is selected. The RSICLK input has an integral pull down resistor.
RXD+ RXD-	PECL Input	63 62	The receive differential data inputs (RXD+, RXD-) contain the 155.52 Mbit/s receive STS-3/STM-1 or 51.84 Mbit/s receive STS-1 stream. RXD+/- is sampled on the rising edge of RXC+/- (the falling edge may be used by reversing RXC+/-).
RXC+ RXC-	PECL Input	59 58	The receive differential clock inputs (RXC+, RXC-) provides timing for processing the bit serial receive stream, RXD+/- when the PECL bit serial mode is selected. RXC+/- is nominally a 155.52 MHz or 51.84 MHz, 50% duty cycle clock. RXD+/- is sampled on the rising edge of RXC+/-. RXC+/- is divided by eight to produce GRICLK when the PECL bit serial mode is selected.

Pin Name	Pin Type	Pin No.	Function
RLAIS/	Input	8	The receive line AIS insertion (RLAIS) signal controls the insertion of line AIS in the receive outgoing stream, ROUT[7:0], when the ring control port is disabled. When RLAIS is high, line AIS is inserted in the outgoing stream. Line AIS is also optionally inserted automatically upon detection of loss of signal, loss of frame, section trace alarms or line AIS in the incoming stream. RLAIS is sampled on the rising edge of RICLK.
TRCPCLK			The transmit ring control port clock (TRCPCLK) signal provides timing for the transmit ring control port when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the Master Control Register). TRCPCLK is nominally a 3.24 MHz, 50% duty cycle clock and is normally connected to the RRCPCLK output of a mate STXC in ring-based add-drop multiplexer applications. TRCPFP and TRCPDAT are sampled on the rising edge of TRCPCLK.
OOF	Output	57	The out of frame (OOF) signal is set high while the STXC is unable to find a valid framing pattern (A1, A2) in the incoming stream. OOF is set low when a valid framing pattern is detected. OOF is updated on the rising edge of RICLK.
LOF	Output	56	The loss of frame (LOF) signal is set high when an out of frame state persists for 3 ms. LOF is set low when an in frame state persists for 3 ms. LOF is updated on the rising edge of RICLK.

Pin Name	Pin Type	Pin No.	Function
LOS/	Output	71	Loss of signal (LOS) is active when the ring control port is disabled. Loss of signal (LOS) is set high when a violating period (20 ± 2.5 µs) of consecutive all zeros patterns is detected in the incoming stream. LOS is set low when two valid framing words (A1, A2) are detected, and during the intervening time (125 µs), no violating period of all zeros patterns is observed. LOS is updated on the rising edge of RICLK.
RRCPFP			The receive ring control port frame position (RRCPFP) signal identifies bit positions in the receive ring control port data (RRCPDAT) when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the Master Control Register). RRCPFP is high during the filtered K1, K2 bit positions, the change of APS value bit position, the protection switch byte failure bit position, and the send AIS and send RDI bit positions in the RRCPDAT stream. RRCPFP is normally connected to the TRCPFP input of a mate STXC in ring-based add-drop multiplexer applications. RRCPFP is updated on the falling edge of RRCPCLK.
B1E	Output	55	The B1 error clock (B1E) is a return to zero signal that pulses high for 154 ns with a minimum low time of 154 ns for every section bit interleaved parity error (B1) detected in the incoming stream. Up to eight pulses may occur on B1E per frame.

Pin Name	Pin Type	Pin No.	Function
RDI/	Output	73	The far end receive failure (RDI) signal is active when the ring control port is disabled. RDI is set high when line RDI is detected in the incoming stream. RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. RDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. This alarm indication is also available through register access. RDI is updated on the rising edge of RICLK.
RRCPCLK			The receive ring control port clock (RRCPCLK) signal provides timing for the receive ring control port when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the Master Control Register). RRCPCLK is nominally a 3.24 MHz, 50% duty cycle clock and is normally connected to the TRCPCLK input of a mate STXC in ring-based add-drop multiplexer applications. RRCPFP and RRCPDAT are updated on the falling edge of RRCPCLK.

Pin Name	Pin Type	Pin No.	Function
LAIS/	Output	72	The line alarm indication (LAIS) signal is active when the ring control port is disabled. LAIS is set high when line AIS is detected in the incoming stream. LAIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. This alarm indication is also available through register access. LAIS is updated on the rising edge of RICLK.
RRCPDAT			The receive ring control port data (RRCPDAT) signal contains the receive ring control port data stream when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the Master Control Register). The receive ring control port data consists of the filtered K1, K2 byte values, the change of APS value bit position, the protection switch byte failure status bit position, the send AIS and send RDI bit positions, and the line REI bit positions. RRCPDAT is normally connected to the TRCPDAT input of a mate STXC in ring-based add-drop multiplexer applications. RRCPDAT is updated on the falling edge of RRCPCLK.
B2E	Output	78	The B2 error clock (B2E) is a return to zero signal that pulses 154 ns with a minimum low time of 154 ns for every line bit interleaved parity error (B2) detected in the incoming stream. Up to 8 (STS-1), or 24 (STS-3/STM-1) pulses may occur on B2E, per frame.
RSDCLK	Output	67	The receive section DCC clock (RSDCLK) is a 192 kHz clock used to update the RSD output. RSDCLK is generated by gapping a 216 kHz clock.

Pin Name	Pin Type	Pin No.	Function
RSD	Output	66	The receive section DCC (RSD) signal contains the section data communications channel (D1, D2, D3) extracted from the incoming stream. RSD is updated on the falling edge of RSDCLK.
ROWCLK	Output	70	The receive order wire clock (ROWCLK) is a 64 kHz clock used to update the RSOW, RSUC, and RLOW outputs. ROWCLK is generated by gapping a 72 kHz clock.
RSOW	Output	68	The receive section order wire (RSOW) signal contains the section order wire channel (E1) extracted from the incoming stream. RSOW is updated on the falling edge of ROWCLK.
RSUC	Output	69	The receive section user channel (RSUC) signal contains the section user channel (F1) extracted from the incoming stream. RSUC is updated on the falling edge of ROWCLK.
RLOW	Output	81	The receive line order wire (RLOW) signal contains the line order wire channel (E2) extracted from the incoming stream. RLOW is updated on the falling edge of ROWCLK.
RLDCLK	Output	80	The receive line DCC clock (RLDCLK) is a 576 kHz clock used to update the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock.
RLD	Output	79	The receive line DCC (RLD) signal contains the line data communications channel (D4 - D12) extracted from the incoming stream. RLD is updated on the falling edge of RLDCLK.
RAPSCLK	Output	83	The receive automatic protection switch channel clock (RAPSCLK) is a 128 kHz clock used to update the RAPS output. RAPSCLK is generated by gapping a 144 kHz clock.

Pin Name	Pin Type	Pin No.	Function
RAPS	Output	82	The receive automatic protection switch channel (RAPS) signal carries the automatic protection switch channel (K1, K2) extracted from the incoming stream. RAPS is updated on the falling edge of RAPSCLK.
RTOH	Output	87	The receive transport overhead (RTOH) signal contains the receive transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1, Z2, and E2) extracted from the incoming stream. RTOH is updated on the falling edge of RTOHCLK.
RTOHCLK	Output	88	The receive transport overhead clock (RTOHCLK) is nominally a 5.184 MHz or 1.728 MHz clock that provides timing to process the extracted receive transport overhead, RTOH. RTOHCLK is a gapped 6.48 MHz clock when accessing the transport overhead of an STS-3/STM-1 stream. RTOHCLK is a gapped 2.16 MHz clock when accessing the transport overhead of an STS-1 stream.
RTOHFP	Output	84	The receive transport overhead frame position (RTOHFP) signal is used to locate the individual receive transport overhead bits in the receive transport overhead, RTOH. RTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is present in the RTOH stream. RTOHFP is updated on the falling edge of RTOHCLK.

Pin Name	Pin Type	Pin No.	Function
GRICLK	Output	134	When either of the bit serial receive interfaces are enabled, GRICLK is the generated byte serial clock. When the bit serial STS-1 mode is enabled, GRICLK is a 6.48 MHz clock that is generated by dividing the receive serial incoming clock (RSICLK) by eight. When the bit serial STS-3 mode is enabled, GRICLK is a 19.44 MHz clock that is generated by dividing the receive serial incoming clock (RSC+/-) by eight. GRICLK must be externally shorted directly to the receive incoming clock (RICLK) when processing a bit serial stream.
ROUT[7] ROUT[6] ROUT[5] ROUT[4] ROUT[3] ROUT[2] ROUT[1] ROUT[0]	Output Output Output Output Output Output Output Output	123 124 125 126 127 128 131 132	ROUT[7:0] contains the descrambled outgoing stream in byte serial format. ROUT[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit received). ROUT[0] is the least significant bit (corresponding to bit 8 of each serial PCM word). ROUT[7:0] is updated on the rising edge of RICLK.
ROFP	Output	133	The active high receive outgoing frame position (ROFP) signal is set high once per frame in the byte position immediately following the Z0 bytes in the ROUT[7:0] stream. ROFP is also used to mark the alignment of the RSOW, RSUC, RLOW and RAPS bit streams. ROFP is updated on the rising edge of RICLK.
TSER	Input	12	The transmit serial input (TSER) selects the transmit line interface. TSER is tied high to select the bit serial interface on PECL pins TXCI+, TXCI-, TXCO+, TXCO-, TXD+, and TXD-. A TTL interface is also supported in STS-1 mode on pins TSICLK and TSOUT. TSER is tied low to select the byte serial interface on pins TICLK, TOFP, and TOUT[7:0].

Pin Name	Pin Type	Pin No.	Function
TICLK/	Input	140	The transmit incoming clock (TICLK) provides timing for processing the transmit stream, TIN[7:0]. TICLK is nominally a 6.48 MHz (STS-1), or 19.44 MHz (STS-3/STM-1) 50% duty cycle clock, depending on the selected operating mode. TIN[7:0], and TIFP are sampled on the rising edge of TICLK. TICLK must be externally shorted directly to GTICLK when processing bit serial transmit streams.
TVCLK			The transmit vector clock (TVCLK) is used during STXC production test to verify internal functionality.
GTICLK	Output	141	When either of the bit serial transmit interfaces are enabled, GTICLK is the generated byte serial clock. GTICLK is a 6.48 MHz or 19.44 MHz clock that is generated by dividing the transmit serial incoming clock (TSICLK or TXCI+/-) by eight. GTICLK must be externally shorted directly to the transmit incoming clock (TICLK) when processing a bit serial stream. In line loopback mode operation (LLE bit set high), GTICLK is generated by dividing the RXC+/- inputs by eight.
TSICLK	Input	11	The transmit serial incoming clock (TSICLK) provides timing for updating the bit serial outgoing stream when STS-1 mode is selected. TSICLK is nominally a 51.84 MHz, 50% duty cycle clock. TSOUT is updated on the rising edge of TSICLK. The TSICLK input has an integral pull down resistor. The device may be configured to use the TXCI+/- inputs as the serial clock.
TXCI+ TXCI-	PECL Input	28 27	The transmit differential clock inputs (TXCI+, TXCI-) provide timing for updating the bit serial outgoing stream. TXCI+/- is nominally a 155.52 MHz or 51.84 MHz, 50% duty cycle clock. The TSICLK is the default clock for the 51.84 Mbit/s data rate.

Pin Name	Pin Type	Pin No.	Function
TIN[7] TIN[6] TIN[5] TIN[4] TIN[3] TIN[2] TIN[1] TIN[0]	Input	143 144 145 146 147 148 149 150	The transmit incoming bus, (TIN[7:0]), carries an STS-1 or STS-3/STM-1 stream in byte serial format. TIN[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). TIN[0] is the least significant bit (corresponding to bit 8 of each serial PCM word). TIN[7:0] is sampled on the rising edge of TICLK.
TIFP/ TC1J1V1	Input	142	The active high transmit incoming framing position (TIFP/TC1J1V1) signal indicates the frame alignment for incoming streams. When Register Mode Select bit C1EN is logic 0, a high level on TIFP marks the byte immediately following the Z0 bytes in the transmit STS-1 or STS-3 (STM-1) stream, TIN[7:0]. When Register Mode Select bit C1EN is logic 1, a high level on TIFP marks the first J0 byte in the transmit STS-1 or STS-3 (STM-1) stream, TIN[7:0]. TIFP/TC1J1V1 is sampled on the rising edge of TICLK.

Pin Name	Pin Type	Pin No.	Function
TDIS	Input	151	The active high transmit disable (TDIS) signal selectively disables overwriting the STS-1 or STS-3 (STM-1) byte serial stream with the corresponding overhead byte. TDIS is sampled on the rising edge of TICLK. TDIS takes precedence over the TTOHEN and TTOH inputs. In general, the value on TIN[7:0] passes through transparently if TDIS is high. Three exceptions exist: 1.) Bits 6 to 8 of the K2 byte may be overwritten by a active RDI indication ("110") regardless of the state of TDIS. 2.) If TDIS is high during the section BIP byte (B1), the TIN[7:0] value becomes an error mask for the generated section BIP. 3.) If TDIS is high during the line BIP bytes (B2), and the DB2 bit in the TLOP Control register is logic 0, the TIN[7:0] value becomes an error mask for the generated line BIP.
TTOH	Input	155	The transmit transport overhead bus (TTOH) contains the transport overhead bytes (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1, Z2, and E2) and error masks (H1, H2, B1, and B2) which may be inserted, or used to insert bit interleaved parity errors or payload pointer bit errors into the overhead byte positions in the outgoing stream. Insertion is controlled by the TTOHEN input. TTOH is sampled on the rising edge of TTOHCLK.

Pin Name	Pin Type	Pin No.	Function
TTOHFP	Output	156	The transmit transport overhead frame position (TTOHFP) signal is used to locate the individual transport overhead bits in the transport overhead bus, TTOH. TTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is expected in the incoming stream. TTOHFP is updated on the falling edge of TTOHCLK.
TTOHCLK	Output	153	The transmit transport overhead clock (TTOHCLK) is nominally a 5.184 MHz (1.728 MHz for STS-1) clock that provides timing for upstream circuitry that sources the transport overhead, TTOH. TTOHCLK is a gapped 6.48 MHz clock when accessing the transport overhead of STS-3/STM-1 streams. TTOHCLK is a gapped 2.16 MHz clock when accessing the transport overhead of an STS-1 stream.

Pin Name	Pin Type	Pin No.	Function
TTOHEN	Input	152	The transmit transport overhead insert enable (TTOHEN) signal controls the source of the transport overhead data which is inserted in the transmit stream. While TTOHEN is high during the most significant bit of a TTOH byte (and TDIS is low), values sampled on the TTOH input are inserted into the corresponding transport overhead bit positions (for the A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1, Z2, and E2 bytes). While TTOHEN is low during the most significant bit of a TTOH byte, the default values are inserted into these transport overhead byte positions. A high level on TTOHEN during most significant bit of TTOH for the H1, H2, B1, or B2 bytes enables an error mask. While the error mask is enabled, a high level on TTOH causes the corresponding H1, H2, B1 or B2 bit positions to be inverted. When the section trace enable (STEN) bit is a logic 1, the J0 byte contents are sourced from the section trace buffer, regardless of the state of TTOHEN. A low level on TTOH allows the corresponding bit positions to pass through the STXC uncorrupted. TTOHEN is sampled on the rising edge of TTOHCLK.

Pin Name	Pin Type	Pin No.	Function
TRDI/	Input	10	The active high transmit far end receive failure (TRDI) signal controls the insertion of a far end receive failure indication in the outgoing stream when the ring control port is disabled. When TRDI is set high, bits 6, 7, and 8 of the K2 byte are set to the pattern 110. Line RDI may also be inserted using the RDI bit in the TLOP Control Register, or upon detection of loss of signal, loss of frame, or line AIS in the receive stream, using the AUTORDI bit in the Master Control/Enable Register. The TRDI input takes precedence over the TTOH and TTOHEN inputs. TRDI is sampled on the rising edge of TICLK.
TRCPFP			The transmit ring control port frame position (TRCPFP) signal identifies bit positions in the transmit ring control port data (TRCPDAT) when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the Master Control Register). TRCPFP is high during the filtered K1, K2 bit positions, the change of APS value bit position, the protection switch byte failure bit position, and the send AIS and send RDI bit positions in the TRCPDAT stream. TRCPFP is normally connected to the RRCPFP output of a mate STXC in ring-based add-drop multiplexer applications. TRCPFP is sampled on the rising edge of TRCPCLK.

Pin Name	Pin Type	Pin No.	Function
TLAIS/	Input	9	The active high transmit line alarm indication signal (TLAIS) controls the insertion of line AIS in the outgoing stream when the ring control port is disabled. When TLAIS is set high, the complete frame (except the section overhead or regenerator section) is overwritten with the all ones pattern (before scrambling). The TLAIS input takes precedence over the TTOH and TTOHEN inputs. TLAIS is sampled on the rising edge of TICLK.
TRCPDAT			The transmit ring control port data (TRCPDAT) signal contains the transmit ring control port data stream when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the Master Control Register). The transmit ring control port data consists of the filtered K1, K2 byte values, the change of APS value bit position, the protection switch byte failure status bit position, the send AIS and send RDI bit positions, and the line REI bit positions. TRCPDAT is normally connected to the RRCPDAT output of a mate STXC in ring-based add-drop multiplexer applications. TRCPDAT is sampled on the rising edge of TRCPCLK.
TSDCLK	Output	6	The transmit section DCC clock (TSDCLK) is a 192 kHz clock used to sample the TSD input. TSDCLK is generated by gapping a 216 kHz clock.
TSD	Input	7	The transmit section DCC (TSD) signal contains the section data communications channel (D1, D2, D3) inserted into the outgoing stream. The TTOHEN input takes precedence over TSD. TSD is sampled on the rising edge of TSDCLK.

Pin Name	Pin Type	Pin No.	Function
TOWCLK	Output	3	The transmit order wire clock (TOWCLK) is a 64 kHz clock used to sample the TSOW, TSUC, and TLOW inputs. TOWCLK is generated by gapping a 72 kHz clock.
TSOW	Input	5	The transmit section order wire (TSOW) signal contains the section order wire channel (E1) inserted into the outgoing stream. The TTOHEN input takes precedence over TSOW. TSOW is sampled on the rising edge of TOWCLK.
TSUC	Input	4	The transmit section user channel (TSUC) signal contains the section user channel (F1) inserted into the outgoing stream. The TTOHEN input takes precedence over TSUC. TSUC is sampled on the rising edge of TOWCLK.
TLOW	Input	160	The transmit line order wire (TLOW) signal contains the line order wire channel (E2) inserted into the outgoing stream. The TTOHEN input takes precedence over TLOW. TLOW is updated on the rising edge of TOWCLK.
TLDCLK	Output	1	The transmit line DCC clock (TLDCLK) is a 576 kHz clock used to sample the TLD input. TLDCLK is generated by gapping a 2.16 MHz clock.
TLD	Input	2	The transmit line DCC (TLD) signal contains the line data communications channel (D4 - D12) inserted into the outgoing stream. The TTOHEN input takes precedence over TLD. TLD is sampled on the rising edge of TLDCLK.
TAPSCLK	Output	157	The transmit automatic protection switch channel clock (TAPSCLK) is a 128 kHz clock used to sample the TAPS input. TAPSCLK is generated by gapping a 144 kHz clock.

Pin Name	Pin Type	Pin No.	Function
TAPS	Input	158	The transmit automatic protection switch channel (TAPS) signal carries the automatic protection switch channel (K1, K2) inserted into the outgoing stream. The TTOHEN input takes precedence over TAPS. TAPS is sampled on the rising edge of TAPSCLK.
TOUT[7] TOUT[6] TOUT[5] TOUT[4] TOUT[3] TOUT[2] TOUT[1] TOUT[0]	Output Output Output Output Output Output Output Output	39 38 37 36 33 32 31 30	The transmit outgoing stream, (TOUT[7:0]), carries the scrambled STS-1, or STS-3/STM-1 stream. TOUT[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). TOUT[0] is the least significant bit (corresponding to bit 8 of each serial PCM word). TOUT[7:0] is updated on the rising edge of TICLK.
TSOUT	Output	29	The transmit serial outgoing stream, (TSOUT), contains the scrambled stream in bit serial format when serial STS-1 mode is selected. TSOUT is updated on the rising edge of TSICLK or TXCI+/-.
TXD+ TXD-	PECL Output	22 23	The transmit differential data/positive pulse outputs (TXD+, TXD-) contain the scrambled stream in bit serial format when serial mode is selected. TXD+/- is updated on the falling edge of TXCO+/-.
TXCO+ TXCO-	PECL Output	16 15	The transmit differential clock/negative pulse outputs (TXCO+, and TXCO-) contain transmit output clock. TXCO+/- is a buffered version of TXCI+/-. TXD+/- is updated on the falling edge of TXCO+/-.

Pin Name	Pin Type	Pin No.	Function
TOFP	Output	40	The active high transmit outgoing frame position (TOFP) signal is asserted once per frame in the byte position immediately following the Z0 bytes in the TOUT[7:0] stream. TOFP is also used to mark the alignment of the TSUC, TSOW, TLOW, and TAPS bit streams. TOFP is updated on the rising edge of TICLK.
SCPO[5] RDP	Output	93	The control output (SCPO[5]) is used to control an auxiliary device when the RDPEN bit in the Mode Select register is set to logic 0. The signal level on this output corresponds to the bit value contained in the Output Port register. The receive parity (RDP) signal indicates the parity of the receive bus when the RDPEN bit in the Mode Select register is set to logic 1. The receive data bus (ROUT[7:0]]) is always included in the parity calculation. Internal register bits in the Mode Select register control the inclusion of ROFP in the parity calculation, and the sense (even/odd) of the parity. RDP is updated on the rising edge of RICLK.
SCPO[4] SCPO[3] SCPO[2] SCPO[1] SCPO[0]	Output Output Output Output Output	94 95 96 97 98	The control port (SCPO[4:0]) together with SCPO[5] provides six drive points for controlling auxiliary devices. The signal levels on this output port correspond to the bit values contained in the Output Port register.

Pin Name	Pin Type	Pin No.	Function
SCPI[3]/	Input	89	The status input (SCPI[3]) is used to monitor the operation of an auxiliary device when the ENH bit in the Mode Select register is set to logic 0. An interrupt may be generated when state changes are detected in SCPI[3]. State changes and the real-time signal levels on this signal are available in the Input Port Status/Value register.
TDP			The transmit parity (TDP) signal indicates the parity of the transmit bus when the ENH bit in the Mode Select register is set to logic 1. The transmit data bus (TIN[7:0]) is always included in the parity calculation. Internal register bits in the Mode Select register control the inclusion of frame pulse (TIFP/TC1J1) and payload active signal (TPL) in the parity calculation, and the sense (even/odd) of the parity. TDP is sampled on the rising edge of TICLK. SCPI[3]/TDP contains an internal pull-down resistor.

Pin Name	Pin Type	Pin No.	Function
SCPI[2]/ TPL	Input	90	The status input (SCPI[2]) is used to monitor the operation of an auxiliary device when either the C1EN or the ENH bits in the Mode Select register are set to logic 0. An interrupt may be generated when state changes are detected in SCPI[2]. State changes and the real-time signal levels on this signal are available in the Input Port Status/Value register. The transmit payload (TPL) marks when TIN[7:0] is carrying a payload byte when both the C1EN and ENH bits in the Mode Select register are set to logic 1. It is set high during path overhead and payload bytes and low during transport overhead bytes. TPL is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The TPL signal is optionally used in the parity calculation of the transmit bus. The transmit data bus (TIN[7:0]) is always included in the parity calculation. Internal register bits in the Mode Select register control the inclusion of frame pulse (TIFP) and payload active signal (TPL) in the parity calculation, and the sense (even/odd) of the parity. SCPI[2]/TPL is sampled on the rising edge of TICLK. SCPI[2]/TPL contains an internal pull-down resistor.
SCPI[1] SCPI[0]	Input Input	91 92	The status port (SCPI[1:0]) together with SCPI[3:2] is used to monitor the operation of auxiliary devices. An interrupt may be generated when state changes are detected in the monitored signals. State changes and the real-time signal levels on this port are available in the Input Port Status/Value register. Each of the inputs contains an internal pull-down resistor.

Pin Name	Pin Type	Pin No.	Function
INTB	Output	99	The active low, open drain interrupt (INTB) signal is set when an event is detected on one of the STXC maskable interrupt sources.
A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	114 115 116 117 118 119 120	The address bus (A[6:0]) selects specific registers during accesses.
ALE	Input	121	The address latch enable (ALE) signal latches the address bus (A[6:0]) when low. This allows the STXC to be interfaced to a multiplexed address/data bus. The address latches are transparent when ALE is high. The ALE input has an integral pull up resistor.
MBEB	Input	122	The active low Motorola bus enable (MBEB) signal configures the STXC for Motorola bus mode where the RDB/E signal functions as E, and the WRB/RWB signal functions as RWB. When MBEB is high, the STXC is configured for Intel bus mode where the RDB/E signal functions as RDB. The MBEB input has an integral pull up resistor.
CSB	Input	111	The active low chip select (CSB) signal is asserted during all register accesses.

Pin Name	Pin Type	Pin No.	Function
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	100 101 104 105 106 107 108 109	The bidirectional data bus, D[7:0], is used during STXC read and write accesses.
RDB/ E	Input	113	The active low read enable (RDB) signal is low during a STXC read access. The STXC drives the D[7:0] bus with the addressed register's contents while RDB and CSB are low. The active high external access signal (E) is set high during STXC register access while in Motorola bus mode.
WRB/ RWB	Input	112	The active low write strobe (WRB) signal is low during a STXC write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. The read/write select signal (RWB) selects between STXC register read and write accesses while in Motorola bus mode. The STXC drives the data bus D[7:0] with the contents of the addressed register while CSB is low and RWB and E are high. The contents of D[7:0] are clocked into the addressed register on the falling E edge while CSB and RWB are low.
RSTB	Input	110	The active low reset (RSTB) signal is low to provide an asynchronous reset to the STXC. This schmitt triggered pin contains an internal pull up resistor.

Pin Name	Pin Type	Pin No.	Function
VDDI[0]	Power	45	Core power pins (VDDI[2:0]). These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDO[4:0] pins.
VDDI[1]	Power	76	
VDDI[2]	Power	139	
VSSI[0]	Gnd	50	Core ground pins (VSSI[2:0]). These pins must be connected to a common ground together with the VSSO[6:0] pins.
VSSI[1]	Gnd	75	
VSSI[2]	Gnd	138	
VDDO[0]	Power	35	Pad ring power pins (VDDO[4:0]). These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDI[2:0] pins. Care must be taken to avoid coupling noise induced on the VDDO pins into the VDDI pins.
VDDO[1]	Power	64	
VDDO[2]	Power	74	
VDDO[3]	Power	86	
VDDO[4]	Power	103	
VDDO[5]	Power	130	
VDDO[6]	Power	137	
VDDO[7]	Power	154	
VSSO[0]	Gnd	34	Pad ring ground pins (VSSO[6:0]). These pins must be connected to a common ground together with the VSSI[2:0] pins.
VSSO[1]	Gnd	65	
VSSO[2]	Gnd	77	
VSSO[3]	Gnd	85	
VSSO[4]	Gnd	102	
VSSO[5]	Gnd	129	
VSSO[6]	Gnd	136	
VSSO[7]	Gnd	159	
VT1	Input	13	The transmit PECL logic high reference (VT1) pin must be connected to GND.

Pin Name	Pin Type	Pin No.	Function
VT2	Input	25	The transmit PECL logic low reference (VT2) pin is used to control the logic low voltage level of the output PECL pins, TXCO+/- and TXD+/-. VT2 is engineered to sit at TAVD4 - 2.0 volts. VT2 should be connected to TAVD4 through a reference resistor. The PECL outputs have been designed for optimum performance in a 50Ω transmission line environment. Under these conditions, the reference resistor value is recommended to be 630Ω, ±1%. Additional details are provided in the Application Examples section.
TAVD1 TAVD2 TAVD3	Power	14 18 20	The power (TAVD1, TAVD2, TAVD3) pins for the transmit PECL driver pads. These pins should be connected to the PECL Driver Supply (nominally VDD).
TAVD4	Reference	26	The reference (TAVD4) pin for the transmit PECL circuitry. TAVD4 should be connected to the Transmit Analog Reference Supply.
TAVS1 TAVS2 TAVS3 TAVS4	Ground	17 19 21 24	The ground (TAVS1, TAVS2, TAVS3, TAVS4) pins for the transmit PECL pads. These pins should be connected to GND.
RAVD	Reference	60	The reference pin for the receive PECL circuitry. RAVD should be connected to the Receive Analog Reference Supply.
RAVS	Ground	61	The ground (RAVS) pin for the receive PECL pads. RAVS should be connected to GND.

Notes on Pin Description:

1. VDDI and VSSI are the +5 V and ground connections, respectively, for the core circuitry of the device. VDDO and VSSO are the +5 V and ground connections, respectively, for the pad ring circuitry of the device. These

power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the STXC between the core and pad ring supply rails. Failure to properly make these connections may result in improper operation or damage to the device.

2. Inputs RSTB, MBEB and ALE have internal pull-up resistors.

3. Inputs RSICLK, RSIN, TSICLK and SCPI[3:0] have internal pull-down resistors.

4. All STXC inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except for the TXCI+, TXCI-, RXC+, RXC-, RXD+, and RXD- differential inputs which operate at pseudo ECL (PECL) logic levels.

5. Most STXC digital outputs and bidirectionals have 4 mA drive capability, except the GRICLK and GTICLK outputs which have 8 mA drive capability. All 4 mA and 8 mA outputs are slew rate limited, except TSOUT. Differential outputs TXCO+, TXCO-, TXD+, TXD- operate at pseudo ECL (PECL) logic levels.

6. When receive bit serial mode is enabled (RSER = 1), GRICLK must be shorted to RICLK. The external capacitance must not exceed 30 pF.

7. When transmit bit serial mode is enabled (TSER = 1), GTICLK must be shorted to TICLK. The external capacitance must not exceed 30 pF.

9 FUNCTIONAL DESCRIPTION

9.1 Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) block provides the first stage of digital processing of the receive incoming STS-1 or STS-3 bit serial data stream. The byte alignment in the incoming stream is determined by searching for the 16 bit frame alignment signal (A1, A2) for STS-1 mode, or the 48 bit frame alignment signal (A1, A1, A1, A2, A2, A2) for STS-3 mode. The bit serial stream (RSIN, or RXD+/-) is converted from serial to parallel format in accordance with the determined byte alignment. The bit serial input clock (RSICLK, or RXC+/-) is divided by eight to produce the GRICLK output. GRICLK must be connected externally to RICLK when processing a bit serial stream.

Both TTL and PECL levels may be used at 51.84 Mbit/s, but only the PECL inputs are available at 155.22 Mbit/s.

9.2 Receive Section Overhead Processor

The Receive Section Overhead Processor (RSOP) block processes the section overhead (regenerator section) of the receive incoming stream. It can be configured to process an STS-1, or STS-3/STM-1 data stream.

The RSOP block optionally descrambles the received data and extracts the data communication channel, order wire channel and user channel from the section overhead, and provides them as lower rate bit serial outputs (RSD, RSOW, RSUC) together with associated clock signals (RSDCLK, and ROWCLK). The complete descrambled SONET/SDH data stream is output by the STXC in byte serial format. Line alarm indication signal is inserted in the byte serial output data stream using input RLAIS or, optionally, automatically when loss-of-frame, section trace or loss-of-signal events occur. The automatic insertion of AIS is controlled by the AUTORAIS bit in the Ring Control Register.

Out-of-frame (OOF), loss-of-frame (LOF), and loss-of-signal (LOS) state outputs are provided and section level bit-interleaved parity errors are accumulated. A section BIP-8 error clock is also provided (B1E). A maskable interrupt is activated by state transitions on the OOF, LOF, or LOS outputs, or by a single B1 error event. Microprocessor readable registers are provided that allow accumulated B1 errors to be read out at intervals of up to one second duration.

The RSOP block frames to the data stream by operating with an upstream pattern detector (the Serial to Parallel Converter block; or an external serial to

parallel converter) that searches for occurrences of the framing pattern (A1, A2) in the bit serial data stream. Once the external serial to parallel converter has found byte-alignment, the RSOP block monitors for the next occurrence of the framing pattern 125µs later. The block declares frame alignment when either all A1 and A2 bytes are seen error-free or when only the first A1 byte and the first four bits of the A2 byte are seen error-free. Depending upon the operating mode, the first algorithm examines 2 bytes (A1,A2) in STS-1 mode, or 6 bytes (A1A1A1,A2A2A2) in STS-3/STM-1 mode. The second algorithm examines only the first occurrence of A1 and the first four bits of the first occurrence of A2 in the sequence, regardless of the operating mode. Once in frame, the RSOP block monitors the framing pattern sequence and declares OOF when one or more bit errors in each framing pattern are detected for four consecutive frames. Again, depending upon the operating mode selected the first algorithm examines all 2, or 6 framing bytes for bit errors each frame, while the second algorithm examines only the A1 byte and the first four bits of the A2 byte (i.e. 12 bits total) during each frame.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment the performance of each algorithm is dominated by the alignment algorithm used in the serial to parallel converter. Assuming that the SIPO block is used, the probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the STXC continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a mean time between OOF occurrences of 33 minutes in STS-1 mode and 26 seconds in STS-3/STM-1 mode. The second algorithm provides a mean time between OOF occurrences of 103 minutes, regardless of operating mode.

The RSOP block provides descrambled data and frame alignment indication signals for use by the Receive Line Overhead Processor.

9.3 Receive Line Overhead Processor

The Receive Line Overhead Processor block (RLOP) processes the line overhead (multiplexer section) of a received SONET/SDH data stream. It can be configured to process an STS-1, or an STS-3/STM-1 stream.

The SONET frame alignment is indicated by the Receive Section Overhead Processor. The RLOP extracts the line data communication channel, line order wire channel and automatic protection switch channel from the line overhead, and provides them as lower rate bit serial outputs (RLD, RLOW, RAPS) together with associated clock signals (RLDCLK, ROWCLK, RAPSCLK). Line alarm indication signal is declared (LAIS is set high) when the bit pattern 111 is

observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line far end receive failure is declared (RDI is set high) when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The automatic protection switch bytes (K1, K2) are also extracted into the Receive K1 Register and the Receive K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the Receive K1/K2 Registers

The line level bit-interleaved parity (B2) is computed, and compared to the received B2 bytes. Line BIP-8 errors are accumulated in an internal counter. Registers are provided that allow accumulated line BIP-8 errors to be read out at intervals of up to one second duration. A line BIP-8 error clock is also provided (B2E).

Signal fail (SF) and signal degrade (SD) threshold crossing alarms are detected and indicated using internal register bits. The bit error rates associated with the SF and SD alarms are programmable over a range of 10^{-3} to 10^{-9}. The Bit Error Rate Monitor (BERM) circuit block extracts the Automatic Protection Switch (APS) bytes (K1 and K2), extracts the Synchronization Status byte (Z1), and processes the Line BIP-8 (B2) error signal. A protection switching byte failure alarm is declared when twelve successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the APS K1 Register and the APS K2 Register.

The received line BIP-8/24 error detection code (B2) byte is based on the line overhead and synchronous payload envelope of the receive stream. The line BIP code is a bit interleaved parity calculation using even parity, and the calculated BIP code is compared with the BIP code extracted from the B2 bytes of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192000 (24 BIP/frame x 8000 frames/seconde) bit errors can be detected per second for STS-3 rate and 64000 (8 BIP/frame x 8000 frames/seconde) for STS-1 rate.

The line level far end block error byte (M1) is extracted and accumulated in an internal counter. Registers are provided that allow accumulated line REI events to be read out at intervals of up to one second duration. Bits 2 through 8 of the Z2 byte are used for the line REI function. For STS-1 streams, the line REI byte has 9 legal values (namely 00H - 08H) representing 0 to 8 REI events. For STS-3 streams, the line REI byte has 25 legal values (namely 00H - 18H) representing 0 to 24 REI events. Illegal Z2 values are interpreted as zero errors.

An interrupt output is provided that may be activated by declaration or removal of line AIS, line RDI, protection switching byte failure alarm, a change of APS code value, a single B2 error event, or a single line REI event. Each interrupt source is individually maskable.

9.4 Receive Transport Overhead Access

The Receive Transport Overhead Access block (RTOH) extracts the entire receive transport overhead on the RTOH, along with the 5.184 MHz or 1.728 MHz transport overhead clock, RTOHCLK, and the transport overhead frame position, RTOHFP, allowing identification of the bit positions in the transport overhead stream.

9.5 Ring Control Port

The Transmit and Receive Ring Control Ports provide bit serial access to section and line layer alarm and maintenance signal status and control. These ports are useful in ring-based add drop multiplexer applications where alarm status and maintenance signal insertion control must be passed between separate STXCs (possibly residing on separate cards). Each ring control port consists of three signals: clock, data and frame position. It is intended that the clock, data and frame position outputs of the receive ring control port are connected directly to the clock, data and frame position inputs of the transmit ring control port on the mate STXC. The alarm status and maintenance signal control information that is passed on the ring control ports consists of

- Filtered APS (K1 and K2) byte values
- Change of filtered APS byte value status
- Protection switch byte failure alarm status
- Change of protection switch byte failure alarm status
- Insert the line RDI maintenance signal in the mate STXC

- Insert the line AIS maintenance signal in the mate STXC
- Insert line REI information in the mate STXC.

The same APS byte values must be seen for three consecutive frames before being shifted out on the receive ring control port. The change of filtered APS byte value status is high for one frame when a new, filtered APS value is shifted out.

The protection switch byte failure alarm bit position is high when twelve consecutive frames, where no three consecutive frames contain identical K1 bytes have been received. The bit position is set low when three consecutive frames containing identical K1 bytes have been received. The change of protection switch byte failure alarm status bit position is set high for one frame when the alarm state changes.

The insert line RDI bit position is set high under register control, or when loss of signal, loss of frame, or line AIS alarms are declared. The insert line AIS bit position is set high under register control only.

The insert line REI bit positions are high for one bit position for each detected B2 bit error. Up to 24 REIs may be indicated per frame for an STS-3/STM-1 signal.

9.6 Transmit Transport Overhead Access

The Transmit Transport Overhead Access block (TTOH) allows the complete transport overhead to be inserted using the TTOH, along with the 5.184 MHz or 1.728 MHz transport overhead clock, TTOHCLK, and the transport overhead frame position, TTOHFP. The transport overhead enable signal, TTOHEN, controls the insertion of transport overhead from TTOH. The STXC also supports upstream insertion of the line overhead using the TDIS input. TDIS is used to disable the insertion of transport overhead either from the TTOH bus, or from the individual channels (TSD, TSOW, TSUC, TLD, TAPS, and TLOW).

9.7 Transmit Line Overhead Processor

The Transmit Line Overhead Processor block (TLOP) processes the line overhead of the transmit stream. It can be configured to process an STS-1, or STS-3 (STM-1) stream that is presented in byte serial format at the rate of 6.48 Mbyte/s, or 19.44 Mbyte/s respectively.

The TLOP optionally inserts the line data communication channel, the line order wire channel, and the automatic protection switch channel into the line overhead of the transmit stream. These line overhead channels are separately fed to the

TLOP as bit serial inputs (TLD, TLOW, and TAPS). The TLOP provides the bit serial clock for each line overhead channel (TLDCLK, TOWCLK, TAPSCLK).

Line RDI may be inserted in the transmit stream under the control of an external input (TRDI), or a writeable register. The AUTORDI bit in the Ring Control Register controls the immediate insertion of Line RDI upon detection of Line AIS in the received SONET/SDH stream.

Line REI may be inserted automatically in the SONET/SDH stream under the control of the AUTOREI bit in the Ring Control Register. Receive B2 errors are accumulated and optionally inserted automatically in bits 2 to 8 of the third Z2 byte of the transmit stream (for STS-3/STM-1 modes), or in bits 2 to 8 of the Z2 byte of the transmit stream for STS-1 mode. Up to 8 or 24 errors may be inserted per frame for STS-1 or STS-3/STM-1 modes, respectively.

The line BIP (B2) error detection code for the transmit stream is calculated by the TLOP and is inserted into the line overhead. Errors may be inserted in the B2 code for diagnostic purposes. A byte serial stream, along with a frame position indicator is passed to the Transmit Section Overhead Processor.

9.8 Transmit Section Overhead Processor

The Transmit Section Overhead Processor (TSOP) block processes the section overhead of the transmit stream. It can be configured to process an STS-1, or an STS-3/STM-1 stream that is presented in byte serial format at 6.48 Mbyte/s, or 19.44 Mbyte/s respectively.

The TSOP accepts an unscrambled stream in byte serial format from the Transmit Line Overhead Processor. It optionally inserts the section data communication channel, the order wire channel, and the user channel into the section overhead (regenerator section) of the stream. These section overhead channels are input to the STXC as bit serial signals (TSD, TSOW, and TSUC). The TSOP provides the bit serial clock for each section overhead channel (TSDCLK, and TOWCLK). The line alarm indication signal may optionally be inserted into the data stream under the control of an external input (TLAIS), or a microprocessor writeable register.

The section BIP-8 error detection code (B1) is calculated by the TSOP block and is inserted into the section overhead of the transmit stream. Errors may be inserted in the B1 code for diagnostic purposes. Framing (A1, A2) and identity bytes (J0) are also inserted. Finally, the complete transmit stream is scrambled and output by the TSOP in byte serial format on outputs TOUT[7:0].

The TSOP block is intended to operate with a downstream serializer (the Parallel to Serial Converter block; or an external parallel to serial converter) that accepts the transmit stream in byte serial format and serializes it at the appropriate line rate.

9.9 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) block provides the final stage of digital processing for the transmit data stream. The PISO block converts the data stream from parallel to serial format.

A generated transmit clock (GTICLK) is provided by dividing the incoming transmit line clock (TSICLK, or TXC+/-) by eight. GTICLK must be externally connected to TICLK when processing a bit serial stream.

9.10 Receive Section Trace Buffer

The receive portion of the SONET Section Trace Buffer captures the received section trace identifier message (J0 byte) into microprocessor readable registers. It contains two pages of trace message memory. One is designated the capture page and the other the expected page. Section trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is downloaded by the microprocessor into the expected page. On receipt of a trace identifier byte, it is written into next location in the capture page. The received byte is compared with the data from the previous message in the capture page. An identifier message is accepted if it is received unchanged three times, or optionally, five times. The accepted message is then compared with the expected message. If enabled, an interrupt is generated when the accepted message changes from matching to mismatching the expected message and vice versa. If the current message differs from the previous message for eight consecutive messages, the received message is declared unstable. The received message is declared stable when the received message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state. Optionally, AIS may be inserted in the ROUT[7:0] bus when the receive message is in the mismatched or unstable state.

The length of the section trace identifier message is selectable between 16 bytes and 64 bytes. When programmed for 16 byte messages, the section trace buffer synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64 byte messages, the section trace buffer synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the

head of the capture page. This enables the section trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case, the memory acts as a circular buffer.

9.11 Transmit Section Trace Buffer

The transmit portion of the SONET Section Trace Buffer sources the section trace identifier message (J0) for the Transmit Transport Overhead Access block. The length of the trace message is selectable between 16 bytes and 64 bytes. The section trace buffer contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and delivered serially to the Transport Overhead Access block for insertion in the transmit stream. When the microprocessor is updating the transmit page buffer, the buffer may be programmed to transmit null characters to prevent transmission of partial messages.

9.12 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the STXC to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the STXC while the test mode registers are used to enhance the testability of the STXC.

10 REGISTER DESCRIPTION

Table 1 - Normal Mode Register Memory Map

A[6:0]	Register (ENH* bit = logic 0)	Register (ENH* bit = logic 1)
00H	Master Configuration	Master Configuration
01H	Master Control/Enable	Master Control/Enable
02H	Master Interrupt Status	Master Interrupt Status
03H	Master Reset and Identity	Master Reset and Identity
04H	TLOP Control	TLOP Control
05H	TLOP Diagnostic	TLOP Diagnostic
06H	Transmit K1	Transmit K1
07H	Transmit K2	Transmit K2
08H	RLOP Control/Status	RLOP Control/Status
09H	RLOP Interrupt	RLOP Interrupt
0AH	B2 Error Count #1	B2 Error Count #1
0BH	B2 Error Count #2	B2 Error Count #2
0CH	B2 Error Count #3	B2 Error Count #3
0DH	REI Error Count #1	REI Error Count #1
0EH	REI Error Count #2	REI Error Count #2
0FH	REI Error Count #3	REI Error Count #3
10H	RSOP Control	RSOP Control
11H	RSOP Interrupt Status	RSOP Interrupt Status
12H	B1 Error Count #1	B1 Error Count #1
13H	B1 Error Count #2	B1 Error Count #2
14H	Output Port	Output Port
15H	Input Port Interrupt Enable	Input Port Interrupt Enable
16H	Mode Select	Mode Select
17H	Ring Control Port	Ring Control Port
18H	TSOP Control	TSOP Control

A[6:0]	Register (ENH* bit = logic 0)	Register (ENH* bit = logic 1)
19H	TSOP Diagnostic	TSOP Diagnostic
1AH	Transmit Z1	Transmit Z1
1BH	Receive Z1	Transmit Z0
1CH	Reserved	Reserved
1DH	Receive K1	AIS Control
1EH	Receive K2	RDI Control
1FH	Input Port Status/Value	Input Port Status/Value
20H	Section Trace Control	RASE Interrupt Enable
21H	Section Trace Status	RASE Interrupt Status
22H	Section Trace Indirect Address	RASE Configuration/Control
23H	Section Trace Indirect Data	SF Accumulation Period (LSB)
24H	Reserved	SF Accumulation Period
25H	Reserved	SF Accumulation Period (MSB)
26H	Reserved	SF Saturation Threshold (LSB)
27H	Reserved	SF Saturation Threshold (MSB)
28H	Section Trace AIS Insertion	SF Declaring Threshold (LSB)
29H	Reserved	SF Declaring Threshold (MSB)
2AH	Reserved	SF Clearing Threshold (LSB)
2BH	Reserved	SF Clearing Threshold (MSB)
2CH	Reserved	SD Accumulation Period (LSB)
2DH	Reserved	SD Accumulation Period
2EH	Reserved	SD Accumulation Period (MSB)
2FH	Reserved	SD Saturation Threshold (LSB)
30H	Reserved	SD Saturation Threshold (MSB)
31H	Reserved	SD Declaring Threshold (LSB)
32H	Reserved	SD Declaring Threshold (MSB)
33H	Reserved	SD Clearing Threshold (LSB)
34H	Reserved	SD Clearing Threshold (MSB)

A[6:0]	Register (ENH* bit = logic 0)	Register (ENH* bit = logic 1)
35H	Reserved	Receive K1
36H	Reserved	Receive K2
37H	Reserved	Receive Z1
38H	Reserved	Section Trace Control
39H	Reserved	Section Trace Status
3AH	Reserved	Section Trace Indirect Address
3BH	Reserved	Section Trace Indirect Data
3CH- 3FH	Reserved	Reserved
40H-7FH	Reserved for STXC test	Reserved for STXC test

* The ENH bit is contained in the Mode Select Register (addr 16H).

Notes on Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the STXC to determine the programming state of the device.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect STXC operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the STXC operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Address 00H: Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	STEN	0
Bit 6	R/W	TMODE	1
Bit 5	R/W	FPOS	0
Bit 4	R/W	LLE	0
Bit 3	R/W	DLE	0
Bit 2	R/W	RXSEL	0
Bit 1	R/W	LTE	0
Bit 0	R/W	RMODE	1

RMODE:

The RMODE bus selects the operating mode of the receive overhead processor, as follows:

RMODE	MODE
0	STS-1
1	STS-3 (STM-1)

LTE:

The LTE bit selects the source of timing for the transmit section of the STXC. Loop time operation can only be activated while the receive and transmit bit serial interfaces are selected. When LTE is a logic zero, the transmitter timing is derived from inputs TXCI+ and TXCI- or, optionally, from input TSICLK when STS-1 mode is selected.

When LTE is a logic one, and the bit serial interface is selected (TSER and RSER are both tied high), the transmitter timing is derived from the receiver inputs RXCI+ and RXCI- or, optionally, from input RSICLK when STS-1 bit serial mode is selected. Loop timed operation is not supported when the byte serial interface is selected (Either TSER or RSER is tied low).

RXSEL:

The RXSEL bit only has effect when the RSER input is high and the RMODE bit is a logic zero. If RXSEL is a logic zero in this situation, the 51.84 Mbit/s

serial stream and associated clock are expected as TTL compatible signals on the RSIN and RSICLK inputs, respectively. If RXSEL is a logic one, the 51.84 Mbit/s serial stream and associated clock are expected as PECL compatible signals on the RXD+/- and RXC+/- inputs, respectively.

DLE:

The DLE bit enables the STXC diagnostic loopback. Diagnostic loopback may only be activated while the bit serial interface is selected (TSER and RSER are both tied high). When DLE is a logic one, the transmit stream is connected to the receive stream.

LLE:

The LLE bit enables the STXC line loopback. Line loopback may only be activated while the bit serial interface is selected (TSER and RSER are both tied high). When LLE is a logic one, RXD+, RXD-, RXC+, RXC-, and RSIN are connected internally to TXD+, TXD-, TXCO+, TXCO-, and TSOUT respectively.

FPOS:

When the byte serial receive STS-3 mode is selected, the FPOS bit controls receive interface of the STXC. When FPOS is a logic zero, the receive incoming frame position (RIFP) is expected during the third A2 byte of the receive incoming stream (RIN[7:0]). When FPOS is a logic one, the receive incoming frame position is indicated during the byte position immediately following the last Z0 byte in the receive incoming stream. In the byte serial receive STS-1 mode, the incoming frame position is indicated during the byte position immediately following the Z0 byte in the receive incoming stream regardless of the state of FPOS.

TMODE:

The TMODE bus selects the operating mode of the transmit overhead processor as follows:

TMODE	MODE
0	STS-1
1	STS-3 (STM-1)

STEN:

The STEN bit controls whether the section trace message stored in the section trace buffer is inserted in the transmit stream. When STEN is a logic

one, the message in the section trace buffer is inserted in the transmit stream. When STEN is a logic zero, the Z0 byte contents are supplied by the TSOP block or via the TTOH input.

Address 01H: Master Control/Enable

Bit	Type	Function	Default
Bit 7	R/W	RCP	0
Bit 6	R/W	Z1E/Z0INS	0
Bit 5	R/W	PSBFE/TDPE	0
Bit 4	R/W	COAPSE/RASEE	0
Bit 3	R/W	TCLKSEL	0
Bit 2	R/W	RSOPE	0
Bit 1	R/W	STBE	0
Bit 0	R/W	RLOPE	0

RLOPE:

The RLOP interrupt enable is an interrupt mask for events detected by the receive line overhead processor. When RLOPE is a logic one, an interrupt is generated when line layer events are detected, provided the associated enable in the RLOP Interrupt Enable and Status register is set.

STBE:

The section trace buffer interrupt enable is an interrupt mask for events detected by the receive section trace buffer. When STBE is a logic one, an interrupt is generated when section trace events are detected by the section trace buffer.

RSOPE:

The RSOP interrupt enable is an interrupt mask for events detected by the receive section overhead processor. When RSOPE is a logic one, an interrupt is generated when section layer events are detected, provided the associated enable in the RSOP Control register is set.

TCLKSEL:

The TCLKSEL bit only has effect when the TSER input is high and the TMODE bit is a logic zero. If TCLKSEL is a logic zero in this situation, TTL compatible TSICLK input is the source of the 51.84 MHz transmit serial clock. If TCLKSEL is a logic one, the PECL compatible TXCI+/- inputs are the source of the 51.84 MHz transmit serial clock.

COAPSE/RASEE:

The change of APS byte interrupt enable (COAPSE) is an interrupt mask for events detected by the receive APS processor. When the ENH bit in the Mode Select register is a logic 0, COAPSE set to a logic one enables an interrupt to be generated when a new K1/K2 code value has been extracted into the Receive K1/K2 Registers.

The RASE interrupt enable (RASEE) is an interrupt mask for events detected by the receive APS and synchronization extractor. When the ENH bit in the Mode Select register is a logic 1, RASEE set to a logic one enables an interrupt to be generated when the APS status changes, APS alarm or a threshold crossing, provided the associated enable in the RASE Interrupt Enable register is set.

PSBFE/TDPE:

The change of protection switch byte failure alarm interrupt enable (PSBFE) is an interrupt mask for events detected by the receive APS processor. When PSBFE is a logic one, and the ENH bit in the Mode Select register is a logic 0, an interrupt is generated upon a change in the protection switch byte failure alarm state.

The transmit parity error interrupt enable (TDPE) is an interrupt mask for parity errors detected on the transmit bus. When TDPE is a logic one, and the ENH bit in the Mode Select register is logic 1, an interrupt is generated when parity errors are detected on the transmit bus.

Z1E/Z0INS:

The change of Z1 interrupt enable (Z1E) is an interrupt mask for changes in the receive Z1 byte value. When Z1E is a logic one, and the ENH bit in the Mode Select register is a logic 0, an interrupt is generated when the extracted Z1 byte is different from the Z1 byte extracted in the previous frame.

The Z0INS bit controls the values inserted in the transmit Z0 bytes when STS-3/STM-1 mode is selected. When Z0INS is logic 1, and the ENH bit in the Mode Select register is a logic 0, the value contained in the Transmit Z0 register is inserted in the two Z0 bytes. When Z0INS is logic 0, the values 02H and 03H are inserted in Z0 byte of 2nd and 3rd STS-1 respectively. Note that values inserted using the transmit transport overhead port or the TDIS input take priority over Z0INS. Note also that this bit must be set to logic 0 for the DC1 bit in the TSOP Control register to function correctly.

RCP:

The RCP bit controls the enabling of the receive and transmit ring control ports. When RCP is a logic zero, the ring control ports are disabled, and the LOS, LAIS and RDI outputs and the RLAIS, TLAIS, and TRDI inputs are used to monitor alarm status and control maintenance signal insertion. When RCP is a logic one, the ring control ports are enabled, and alarm status and maintenance signal insertion control is provided by the RRCPCLK, RRCPFP, and RRCPDAT outputs and the TRCPCLK, TRCPFP, and TRCPDAT inputs.

Address 02H: Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSBFV	X
Bit 6	R	Z1I	X
Bit 5	R	PSBFI/TDPI	X
Bit 4	R	COAPSI/RASEI	X
Bit 3		Unused	X
Bit 2	R	RSOPI	X
Bit 1	R	STBI	X
Bit 0	R	RLOPI	X

RLOPI:

The RLOPI bit is set high when one or more of the maskable interrupt sources in the receive line overhead processor has been activated. This register bit remains high until the interrupt is acknowledged by reading the RLOP Interrupt Enable and Status Register.

STBI:

The STBI bit is set high when one or more of the maskable interrupt sources in the section trace buffer has been activated. This register bit remains high until the interrupt is acknowledged by reading the Section Trace Interrupt Enable and Status Register.

RSOPI:

The RSOPI bit is set high when one or more of the maskable interrupt sources in the receive section overhead processor has been activated. This register bit remains high until the interrupt is acknowledged by reading the RSOP Interrupt Status Register.

COAPSI/RASEI:

The COAPSI bit is set high when a new APS code value has been extracted into the Receive K1/K2 Registers and the ENH bit in the Mode Select register is a logic 0. The registers are updated when the same new K1/K2 byte values are observed for three consecutive frames. This bit is cleared when the Master Interrupt Status Register is read.

The RASEI bit is set high when one or more of the maskable interrupt sources in the receive APS and synchronization extractor has been activated and the ENH bit in the Mode Select register is a logic 1. This register bit remains high until the interrupt is acknowledged by reading the RASE Interrupt Status Register.

PSBFI/TDPI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed and the ENH bit in the Mode Select register is a logic 0. This bit is cleared when the Master Interrupt Status Register is read.

The TDPI bit is set high when a parity error is detected on the transmit bus and both the ENH bit in the Mode Select register are logic 1. This bit is cleared when the Master Interrupt Status Register is read.

Z1I:

The Z1I bit is set high when a new Z1 byte value has been extracted into the Receive Z1 Register and the ENH bit in the Mode Select register is a logic 0. The register is updated when a Z1 byte value is extracted that is different than the Z1 byte value extracted in the previous frame. This bit is cleared when the Master Interrupt Status Register is read. This bit position is reserved when the ENH bit in the Mode Select register is a logic 1.

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state when the ENH bit in the Mode Select register is a logic 0. The alarm is declared (PSBFV is set high) when twelve successive frames, where no three consecutive frames contain identical K1 bytes, have been received. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received. This bit position is reserved when the ENH bit in the Mode Select register is a logic 1.

Address 03H: Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	RICLKA	0
Bit 5	R	TICLKA	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

A write to this register initiates a transfer of all performance monitor counter values (B1, B2, and line REI) into holding registers.

ID[4:0]:

The version identification bits ID[4:0], are set to the value 01H, representing the version number of the STXC.

TICLKA:

The transmit clock activity monitor is set to a logic one if one or more rising edges are detected on primary input TICLK since the last time this register was read. A logic zero in this bit position indicates TCLK is not toggling.

RICLKA:

The receive clock activity monitor is set to a logic one if one or more rising edges are detected on primary input RICLK since the last time this register was read. A logic zero in this bit position indicates RICLK is not toggling.

RESET:

The RESET bit allows the STXC to be asychronously reset. The software reset is equivalent to setting the RSTB input pin low. When RESET is a logic one, the STXC is reset. When RESET is a logic zero, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

Address 04H: TLOP Control

Bit	Type	Function	Default
Bit 7	R/W	DB2	0
Bit 6	R/W	UBT	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	DZ2	0
Bit 3	R/W	DAPS	0
Bit 2	R/W	DDL	0
Bit 1	R/W	DOW	0
Bit 0	R/W	RDI	0

RDI:

The RDI bit controls the insertion of transmit line remote defect indication (RDI). When RDI is a logic one, line RDI is inserted into the transmit stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte. Line RDI may also be inserted using the TRDI input (when the ring control ports are disabled) or using the transmit ring control port (when it is enabled). When RDI is logic zero, bit 6, 7, and 8 of the K2 byte are not modified by the transmit line overhead processor.

DOW:

The DOW bit controls the overwriting of the express orderwire byte (E2). When DOW is logic one, the value sampled on TIN[7:0] during the E2 byte position is passed through the transmit line overhead processor unaltered, as though the TDIS input had been sampled high during the E2 byte position in the incoming frame. The upstream insertion of the express orderwire is thus accomplished without the use of the TDIS input. Note that only the E2 byte position is passed unaltered, the remaining 2 (STS-3/STM-1) undefined byte positions are overwritten with all zeros. This overwriting may be defeated by using the TDIS input, or by using the UBT bit in this register. When DOW is logic zero, the express order wire source is nominally the TLOW input (while TDIS and TTOHEN are both low).

DDL:

The DDL bit controls the overwriting of the line data communications channel (D4 - D12). When DDL is logic one, the values sampled on TIN[7:0] during

the D4 - D12 byte positions are passed through the transmit line overhead processor unaltered, as though the TDIS input had been sampled high during the D4 - D12 byte positions in the incoming frame. The upstream insertion of the line DCC is thus accomplished without the use of the TDIS input. Note that only the D4 - D12 byte positions are passed unaltered, the remaining 18 (STS-3/STM-1) undefined byte positions are overwritten with all zeros. This overwriting may be defeated by using the TDIS input, or by using the UBT bit in this register. When DDL is logic zero, the line DCC source is nominally the TLD input (while TDIS and TTOHEN are both low).

DAPS:

The DAPS bit controls the overwriting of the automatic protection switch channel (K1, K2). When DAPS is logic one, the values sampled on TIN[7:0] during the K1 and K2 byte positions are passed through the transmit line overhead processor unaltered, as though the TDIS input had been sampled high during the K1 and K2 byte positions in the incoming frame. The upstream insertion of the APS channel is thus accomplished without the use of the TDIS input. Note that only the K1 and K2 byte positions are passed unaltered, the remaining 4 (STS-3/STM-1) undefined byte positions are overwritten with all zeros. This overwriting may be defeated by using the TDIS input, or by using the UBT bit in this register. When DAPS is logic zero, the APS source is nominally the TAPS input or the Transmit K1/K2 Registers (as selected by the APSREG bit in the TLOP Control Register while TDIS and TTOHEN are both low).

DZ2:

The DZ2 bit controls the overwriting of the Z2 growth byte. When DZ2 is logic one, the values sampled on TIN[7:0] during the Z2 byte position are passed through the transmit line overhead processor unaltered, as though the TDIS input had been sampled high during the Z2 byte position in the incoming frame. The upstream insertion of the growth bytes is thus accomplished without the use of the TDIS input. Note that all 3 (STS-3/STM-1) or 1 (STS-1) Z2 bytes are passed through unaltered. When DZ2 is logic zero, the Z2 byte positions are nominally overwritten with the line REI value and all zeros (while TDIS and TTOHEN are both low).

APSREG:

The APSREG bit selects the source for the transmit APS channel. When APSREG is a logic zero, the transmit APS channel is inserted from the bit serial input TAPS which is shifted in on the rising edge of TAPSCLK. When APSREG is a logic one, the transmit APS channel is inserted from the Transmit K1 Register and the Transmit K2 Register. The APS bytes may also

be inserted upstream of the TLOP using the TDIS or TTOHEN inputs, or the DAPS bit in the TLOP Control Register. Values inserted using TDIS take precedence over the source selected by the APSREG bit.

UBT:

The UBT bit controls the overwriting of the unused byte positions in the transmit STS-3/STM-1 stream. The unused bytes are contained in the K1, K2, D4-D12, and E2 byte positions of STS-1 #2 and STS-1 #3. When UBT is logic zero, the unused byte position are overwritten with all zeros. When UBT is logic one, the values sampled on TIN[7:0] during the unused byte positions are passed through the transmit line overhead processor unaltered, as though the TDIS input had been sampled high during the unused byte positions in the incoming frame.

DB2:

The DB2 bit controls the insertion of the B2 bytes. When DB2 is logic one, the values sampled on TIN[7:0] during the B2 byte positions are passed through the transmit line overhead processor unaltered. When DB2 is logic zero, the internally calculated bit interleaved parity bytes are inserted in the B2 byte positions.

Address 05H: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DB2	0

DB2:

The DB2 bit controls the insertion of bit errors continuously in each of the line BIP-8 bytes (B2 bytes). When DB2 is set high, each bit of every B2 byte is inverted.

Address 06H: Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is logic one. K1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the Transmit K2 Register are inserted in the SONET/SDH stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Address 07H: Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is logic one. K2[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K2[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the Transmit K1 Register.

Address 08H: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	AISDET	0
Bit 4	R/W	RDIDET	0
Bit 3	R/W	BIPWORDO	0
Bit 2		Unused	X
Bit 1	R	LAISV	X
Bit 0	R	RDIV	X

RDIV:

The RDIV bit is set high when line RDI is detected. Line RDI is detected when a 110 binary pattern is detected in bits 6, 7, and 8, of the K2 byte for three or five consecutive frames (as selected by the RDIDET bit in this register). Line RDI is removed when any pattern other than 110 is detected for three or five consecutive frames. This alarm indication is also available on output RDI.

LAISV:

The LAISV bit is set high when line AIS is detected. Line AIS is detected when a 111 binary pattern is detected in bits 6, 7, and 8, of the K2 byte for three or five consecutive frames (as selected by the AISDET bit in this register). Line AIS is removed when any pattern other than 111 is detected for three or five consecutive frames. This alarm indication is also available on output LAIS.

BIPWORDO:

The BIPWORDO bit controls the indication of B2 errors on the B2E output. When BIPWORDO is logic one, the B2E output is asserted for once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORDO is logic zero, the B2E output is asserted once for every B2 bit error that occurs during that frame (the BIPE output can be asserted up to 8xN BIPECLK periods, for N=1, or 3). The accumulation of B2 error events functions independently from the B2E output indication, and is controlled by the BIPWORD register bit.

If the AUTOREI register bit is a logic one and the RINGEN register bit is a logic zero, the number of block errors sent to the far end in the line REI bits equals the number of B2E assertions. If BIPWORDO is a logic one, bits 2 through 8 of the transmitted Z2 byte may only contain 00H and 01H.

RDIDET:

The RDIDET bit determines the line RDI alarm detection algorithm. When RDIDET is set to logic one, line RDI is declared when a 110 binary pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames and is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When RDIDET is set to logic zero, line RDI is declared when a 110 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames and is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

AISDET:

The AISDET bit determines the line AIS alarm detection algorithm. When AISDET is set to logic one, line AIS is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames and is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When AISDET is set to logic zero, line AIS is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames and is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

ALLONES:

The ALLONES bit controls automatically forcing the ROUT[7:0] outputs to logical all-ones whenever line AIS is detected. When ALLONES is set to logic one, the output bus is forced to logic one immediately when the line AIS alarm is declared. When line AIS is removed, the outputs are immediately returned to carrying the receive stream. When ALLONES is set to logic zero, the outputs carry the receive stream regardless of the state of the line AIS alarm.

BIPWORD:

The BIPWORD bit controls the accumulation of B2 errors. When BIPWORD is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORD is logic zero, the B2 error event counter is incremented for each B2 bit error that occurs during that frame (the counter can be incremented up to 8xN times per frame, for N=1 or 3).

Address 09H: RLOP Interrupt Enable and Status

Bit	Type	Function	Default
Bit 7	R/W	REIE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	RDIE	0
Bit 3	R	REII	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	RDII	X

RDII:

The RDII bit is set high when line RDI is declared or removed. This bit is cleared when the RLOP Interrupt Enable and Status Register is read.

LAISI:

The LAISI bit is set high when line LAIS is declared or removed. This bit is cleared when the RLOP Interrupt Enable and Status Register is read.

BIPEI:

The BIPEI bit is set high when a line BIP error is detected. This bit is cleared when the RLOP Interrupt Enable and Status Register is read.

RDIE:

The RDI interrupt enable is an interrupt mask for line RDI. When RDIE is a logic one, a line interrupt is generated when line RDI is declared or removed.

LAISE:

The LAIS interrupt enable is an interrupt mask for line AIS. When LAISE is a logic one, a line interrupt is generated when line AIS is declared or removed.

BIPEE:

The line BIP error interrupt enable is an interrupt mask for line BIP error events. When BIPEE is a logic one, a line interrupt is generated when a line BIP error (B2) is detected.

REIE:

The line remote error indication interrupt enable is an interrupt mask for line REI events. When REIE is a logic one, a line interrupt is generated when a line REI indication is detected.

Address 0AH: B2 Error Count #1

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

Address 0BH: B2 Error Count #2

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

Address 0CH: B2 Error Count #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	BE[19]	X
Bit 2	R	BE[18]	X
Bit 1	R	BE[17]	X
Bit 0	R	BE[16]	X

BE[19:0]:

Bits BE[19] through BE[0] represent the number of line bit-interleaved parity errors that have been detected since the last accumulation interval. The error counters are polled by writing to any of the B2 Error Count Register addresses (0AH, 0BH, or 0CH), or by writing to the Master Reset and Identity Register (03H). Such a write transfers the internally accumulated error count to the registers within 1µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 1µs period has elapsed, the B2 Error Count Registers may be read.

Address 0DH: REI Error Count #1

Bit	Type	Function	Default
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Address 0EH: REI Error Count #2

Bit	Type	Function	Default
Bit 7	R	FE[15]	X
Bit 6	R	FE[14]	X
Bit 5	R	FE[13]	X
Bit 4	R	FE[12]	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

Address 0FH: REI Error Count #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	FE[19]	X
Bit 2	R	FE[18]	X
Bit 1	R	FE[17]	X
Bit 0	R	FE[16]	X

FE[19:0]:

Bits FE[19] through FE[0] represent the number of line remote error indications that have been detected since the last accumulation interval. The error counters are polled by writing to any of the REI Error Count Register addresses (0DH, 0EH, or 0FH), or by writing to the Master Reset and Identity Register (03H). Such a write transfers the internally accumulated error count to the registers within 1µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 1µs period has elapsed, the REI Error Count Registers may be read.

Address 10H: RSOP Control

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOF interrupt enable is an interrupt mask for out of frame. When OOFE is a logic one, a section interrupt is generated when OOF is declared or removed.

LOFE:

The LOF interrupt enable is an interrupt mask for loss of frame. When LOFE is a logic one, a section interrupt is generated when LOF is declared or removed.

LOSE:

The LOS interrupt enable is an interrupt mask for loss of signal. When LOSE is a logic one, a section interrupt is generated when LOS is declared or removed.

BIPEE:

The section BIP interrupt enable is an interrupt mask for section BIP (B1) error events. When BIPE is a logic one, a section interrupt is generated when a section BIP error is detected.

ALGO2:

The ALGO2 bit position selects the framing algorithm used to confirm and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the first A2 framing

byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern regardless of the STS mode; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined. This algorithm examines all 16 bits of the framing pattern in STS-1 mode, and all 48 bits of the framing pattern in STS-3 mode.

FOOF:

When a logic one is written to the force out-of-frame (FOOF) bit location, the STXC is forced out-of-frame at the next frame boundary, regardless of the framing byte values. The out-of-frame event results in the assertion of the OOF output and the OOFV register bit. When operating in a byte serial mode, the OOF output instructs an upstream framing pattern detector to attempt to find a new byte alignment. When operating in a bit serial mode, the reframe procedure is performed internally. The FOOF bit is a write only bit; an RSOP Control register read may yield a logic one or a logic zero in this bit position.

DDS:

The disable descrambling (DDS) bit controls the descrambling of the receive stream. When a logic one is written to the DDS bit position, the descrambler is disabled. When a logic zero is written to the DDS bit position, the descrambler is enabled.

BIPWORD:

The BIPWORD bit position enables the reporting and accumulating of section BIP word errors. When a logic one is written to the BIPWORD bit position, one or more errors in the BIP-8 byte result in a single error indicated per frame on the B1E output and a single error accumulated in the B1 error counter. When a logic zero is written to the BIPWORD bit position, all errors in the B1 byte are indicated per frame on the B1E output and are accumulated in the B1 error counter.

Address 11H: RSOP Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is set high when out of frame is declared. OOF is declared (OOFV is high) while the STXC is unable to find a valid framing pattern (A1, A2) in the incoming stream. OOF is removed when a valid framing pattern is detected. This alarm indication is also available on output OOF.

LOFV:

The LOFV bit is set high when loss of frame is declared. LOF is declared (LOFV is high) when an out of frame state persists for 3 ms. LOF is removed when an in frame state persists for 3 ms. This alarm indication is also available on output LOF.

LOSV:

The LOSV bit is set high when loss of signal is declared. LOS is declared (LOSV is high) when 20 ± 2.5 µs of consecutive all zeros patterns is detected in the incoming stream. LOS is removed when two valid framing words (A1, A2) are detected, and during the intervening time (125 µs), no violating period of all zeros patterns is observed. This alarm indication is also available on output LOS.

OOFI:

The OOFI bit is set high when out of frame is declared or removed. This bit is cleared when the RSOP Interrupt Status Register is read.

LOFI:

The LOFI bit is set high when loss of frame is declared or removed. This bit is cleared when the RSOP Interrupt Status Register is read.

LOSI:

The LOSI bit is set high when loss of signal is declared or removed. This bit is cleared when the RSOP Interrupt Status Register is read.

BIPEI:

The BIPEI bit is set high when a section BIP error is detected. This bit is cleared when the RSOP Interrupt Status Register is read.

Address 12H: B1 Error Count #1

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

Address 13H: B1 Error Count #2

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

BE[15:0]:

Bits BE[15] through BE[0] represent the number of section bit-interleaved parity errors that have been detected since the last accumulation interval. The error counters are polled by writing to any of the B1 Error Count Register addresses (12H, or 13H), or by writing to the Master Reset and Identity Register (03H). Such a write transfers the internally accumulated error count to the registers within 1µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 1µs period has elapsed, the B1 Error Count Registers may be read.

Address 14H: Output Port

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	SCPO[5]	1
Bit 4	R/W	SCPO[4]	1
Bit 3	R/W	SCPO[3]	0
Bit 2	R/W	SCPO[2]	0
Bit 1	R/W	SCPO[1]	1
Bit 0	R/W	SCPO[0]	0

SCPO[4:0]:

The values written to the SCPO[4:0] bit in the output port register directly correspond to the states set on the SCPO[4:0] output pins. This provides a generic port useful for controlling up to 5 signals.

SCPO[5]:

The value written to the SCPO[5] bit in the output port register directly corresponds to the state set on the SCPO[5] output pin when either the ENH bit or the RDPEN bit in the Mode Select register is logic 0. This register bit is reserved when both the ENH bit and the RDPEN bit in the Mode Select register are logic 1.

Address 15H: Input Port Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SCPIE[3]	0
Bit 2	R/W	SCPIE[2]	0
Bit 1	R/W	SCPIE[1]	0
Bit 0	R/W	SCPIE[0]	0

SCPIE[1:0]

The SCPIE[1:0] bits are interrupt enables. When a logic one is written to these locations, the occurrence of an event on the corresponding SCPI[1:0] input activates the interrupt (INTB). The interrupt is cleared by reading the Configuration Input Port Status/Value Register. When a logic zero is written to these locations, the occurrence of an event on the corresponding SCPI[1:0] input is inhibited from activating the interrupt.

SCPIE[3:2]

The SCPIE[3] bits are interrupt enables. When a logic one is written to these locations, the occurrence of an event on the SCPI[3:2] input activates the interrupt (INTB) when the ENH bit in the Mode Select register is logic 0. The interrupt is cleared by reading the Configuration Input Port Status/Value Register. When a logic zero is written to these locations, the occurrence of an event on the corresponding SCPI[3:2] inputs are inhibited from activating the interrupt. These register bits are reserved when the ENH bit in the Mode Select register are logic 1.

Address 16H: Mode Select

Bit	Type	Function	Default
Bit 7	R/W	ODDPG	0
Bit 6	R/W	ODDPC	0
Bit 5	R/W	INCPL	0
Bit 4	R/W	INCFP	0
Bit 3	R/W	C1EN	0
Bit 2	R/W	RDPEN	0
Bit 1	R/W	TSOUTDIS	0
Bit 0	R/W	ENH	0

ENH:

The ENH bit enables an enhanced STXC feature set. When ENH is a logic 0, the enhanced feature set is disabled, and this version of the STXC is backwards compatible with previous versions. When ENH is a logic 1, the enhanced feature set is enabled. The major features of this enhanced feature set include signal fail and signal degrade alarm threshold detection, and optional parity on the receive and transmit busses. Note that certain register addresses are relocated when the enhanced feature set is enabled, and that the STXC register memory map and certain bit positions are not backwards compatible with earlier versions of the device.

TSOUTDIS:

The TSOUTDIS bit disables the transmit serial outgoing stream, TSOUT. When TSOUTDIS is 0 TSOUT contains the scrambled outgoing stream in bit serial format when serial STS-1 mode is selected. When TSTOUTDIS is 1, or when STS-1 mode is not selected, TSOUT outputs logic 0. When ENH is logic 0, TSOUTDIS is reserved.

RDPEN:

The RDPEN input configures the multifunction output SCPO[5]/RDP, and enables parity generation on the receive bus. When RDPEN is logic 1, SCPO[5]/RDP reports the generated receive parity bit. When RDPEN is a logic 0, or when ENH is logic 0, the multifunction output SCPO[5]/RDP is part of the generic control port.

C1EN:

The C1EN bit configures the multifunction input SCPI[2]/TPL, as well as configures the frame pulse boundaries reported by TIFP/TC1J1V1. When C1EN is logic 0, or when ENH is logic 0, the input SCPI[2]/TPL is sampled as SCPI[2]. Also, TIFP pulses high at the first SPE byte following the Z0 byte(s) to mark frame boundaries. When C1EN is logic 1, SCPI[2]/TPL sampled as TPL. Also, SCPI[2]/TPL is set low while TC1J1V1 pulses high at the J0 byte to mark farme boundaries.

INCFP:

The INCFP bit determines whether the frame pulse signal is included in the receive and transmit parity calculations. When INCFP is logic 1, and when ENH is logic 1, ROFP is included in the receive parity generation when RDPEN is logic 1, and TIFP/TC1J1V1 is included in the trasmit parity calculation. When INCFP is logic 0, ROFP and TIFP/TC1J1V1 are excluded from parity calculations. When ENH is logic 0, INCFP is reserved, and there are no parity calculations.

INCPL:

The INCPL bit determines whether the active payload signal is included in the trasmit parity calculation. When INCPL is a logic 1, and C1EN is logic 1, SCPI[2]/TPL is included in the calculation. When INCPL is a logic 0, or when C1EN is logic 0, SCPI[2]/TPL is excluded from the calculation. When ENH is logic 0, INCPL is reserved, and there are no parity calculations.

ODDPC:

The ODDPC bit controls the parity expected on the transmit bus. When ODDPC is a logic 1, the bus parity including the TDP signal is odd. When ODDPC is a logic 0, the bus parity including the TDP signal is even.

ODDPG:

When parity generation is enabled, ODDPG controls the parity expected on the receive bus. When ODDPG is a logic 1, the bus parity including the RDP signal is odd. When ODDPG is a logic 0, the bus parity including the RDP signal is even.

Address 17H: Ring Control

Bit	Type	Function	Default
Bit 7	R/W	RINGEN	0
Bit 6	R	INSRDI	X
Bit 5	R	INSAIS	X
Bit 4	R/W	AUTOREI	0
Bit 3	R/W	AUTORDI	0
Bit 2	R/W	AUTORAIS	0
Bit 1	R/W	SRDI	0
Bit 0	R/W	SAIS	0

SAIS:

The SAIS bit controls the value of the SENDAIS bit position in the receive ring control port stream. The SAIS bit is used to cause a mate STXC to send the line AIS maintenance signal under software control.

SRDI:

The SRDI bit controls the value of the SENDRDI bit position in the receive ring control port stream. The SENDRDI bit value is determined by the logical OR of this register bit, along with the loss of signal, loss of frame, and line AIS alarm states when the ENH bit in the Mode Select register is a logic 0. When the ENH bit is a logic 1, the SENDRDI bit value is determined by the logical OR of this register bit along with the RDI insertion events programmed in he RDI Control register. The SRDI bit is used to cause a mate STXC to send the line RDI maintenance signal under software control.

AUTORAIS:

The AUTORAIS bit enables the automatic insertion of line AIS in the receive direction. When AUTOAIS is logic one and the ENH bit in the Mode Select register is logic zero, line AIS is automatically inserted in ROUT[7:0] when LOS or LOF is declared. AIS is also conditionally inserted based on the contents of the Section Trace AIS Insertion register. When AUTOAIS is logic zero, automatic AIS insertion is disabled. When ENH is logic one, the AUTOAIS bit is reserved, and line AIS is conditionally inserted in ROUT[7:0] based on the contents of the AIS Control register. Note that the insertion of line AIS is also controlled by the RLAIS input.

AUTORDI:

The AUTORDI bit enables the automatic insertion of line RDI in the transmit direction. When AUTORDI is logic one and the ENH bit in the Mode Select register is logic zero, line RDI is automatically inserted in the transmit stream when LOS, LOF, or line AIS is declared and when the ring control ports are disabled. When AUTORDI is logic zero, automatic RDI insertion is disabled. When ENH is logic one, the AUTORDI bit is reserved, and line RDI is conditionally inserted in the transmit stream based on the contents of the RDI Control register when the ring control ports are disabled. Line RDI is automatically inserted in the transmit stream when the SENDRDI bit position in the transmit ring control port is a logic 1 and when the ring control ports are enabled.

Note that the insertion of line RDI is also controlled by the TRDI input (when the ring control ports are disabled) and the RDI bit in the TLOP Control Register.

AUTOREI:

The AUTOREI bit enables the automatic insertion of line REI events in the transmit direction. When AUTOREI is a logic one, receive B2 errors detected by the STXC (when the ring control ports are disabled), or from the transmit ring control port, (when the ring control ports are enabled) are automatically inserted in the Z2 byte of the transmit stream. When AUTOREI is a logic zero, line REI events are not automatically inserted in the transmit stream. A Z2 byte inserted upstream of the STXC (using the TDIS input) or inserted from the transmit transport overhead port (using the TTOHEN input) take precedence over the automatic insertion of REI events.

INSAIS:

The INSAIS bit reports the value of the SENDAIS bit position in the transmit ring control port. When the ring control ports are enabled, a logic one in this bit position indicates that the STXC is inserting the line AIS maintenance signal.

INSRDI:

The INSRDI bit reports the value of the SENDRDI bit position in the transmit ring control port. When the ring control ports are enabled, a logic one in this bit position indicates that the STXC is inserting the line RDI maintenance signal.

RINGEN:

The RINGEN bit controls the operation of the transmit ring control port when the ring control ports are enabled by the RCP bit in the Master Control/Enable Register. When RINGEN is a logic one, the automatic insertion of line RDI, line AIS, and line REI is controlled by bit positions in the transmit ring control port input stream.

When RINGEN is a logic zero, the insertion of line RDI is done automatically based on alarms detected by the receive portion of the STXC. Also, line REI is inserted based on B2 errors detected by the receive portion of the STXC.

Register 18H: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	UBT	0
Bit 4	R/W	DC1	0
Bit 3	R/W	DUC	0
Bit 2	R/W	DDL	0
Bit 1	R/W	DOW	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set high, the TSOP inserts line AIS into the transmit stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

DOW:

The DOW bit controls the overwriting of the local orderwire byte (E1). When DOW is logic one, the value sampled on TIN[7:0] during the E1 byte position is passed through the transmit section overhead processor unaltered, as though the TDIS input had been sampled high during the E1 byte position in the incoming frame. The upstream insertion of the express orderwire is thus accomplished without the use of the TDIS input. Note that only the E1 byte position is passed unaltered, the remaining 2 (STS-3/STM-1) byte positions are overwritten with all zeros. This overwriting may be defeated by using the TDIS input, or by using the UBT bit in this register. When DOW is logic zero, the section order wire source is nominally the TSOW input (while TDIS and TTOHEN are both low).

DDL:

The DDL bit controls the overwriting of the section data communications channel (D1 - D3). When DDL is logic one, the values sampled on TIN[7:0] during the D1 - D3 byte positions are passed through the transmit section overhead processor unaltered, as though the TDIS input had been sampled high during the D1 - D3 byte positions in the incoming frame. The upstream

insertion of the section DCC is thus accomplished without the use of the TDIS input. Note that only the D1 -D3 byte positions are passed unaltered, the remaining 6 (STS-3/STM-1) undefined byte positions are overwritten with all zeros. This overwriting may only be defeated by using the TDIS input, or by using the UBT bit in this register. When DDL is logic zero, the section DCC source is nominally the TSD input (while TDIS and TTOHEN are both low).

DUC:

The DUC bit controls the overwriting of the section user channel byte (F1). When DUC is logic one, the value sampled on TIN[7:0] during the F1 byte position is passed through the transmit section overhead processor unaltered, as though the TDIS input had been sampled high during the F1 byte position in the incoming frame. The upstream insertion of the user channel is thus accomplished without the use of the TDIS input. Note that only the F1 byte position is passed unaltered, the remaining 2 (STS-3/STM-1) undefined byte positions are overwritten with all zeros. This overwriting may only be defeated by using the TDIS input, or by using the UBT bit in this register. When DUC is logic zero, the section user channel source is nominally the TSUC input (while TDIS and TTOHEN are both low).

DC1:

The DC1 bit controls the overwriting of the identity bytes (J0/Z0). When DC1 is logic one, the values sampled on TIN[7:0] during the J0/Z0 byte positions are passed through the transmit section overhead processor unaltered, as though the TDIS input had been sampled high during the J0/Z0 byte positions in the incoming frame. The upstream insertion of the identity is thus accomplished without the use of the TDIS input. Note that all 1 (STS-1) or 3 (STS-3/STM-1) identification bytes are passed through unaltered. When DC1 is logic zero, the identity bytes are programmed as specified in the North American references: STS-1 #1 J0 = 01H, STS-1 #2 Z0 = 02H, and STS-1 #3 Z0 = 03H. The DC1 bit has no effect on STS-1 #1 when the STEN bit of the Master Configuration register is a logic one.

UBT:

The UBT bit controls the overwriting of the unused byte positions in the transmit STS-3/STM-1 stream. The unused bytes are contained in the B1, E1, F1, D1, D2, and D3 byte positions of STS-1 #2 and STS-1 #3. When UBT is logic zero, the unused byte positions are overwritten with all zeros. When UBT is logic one, the values sampled on TIN[7:0] during the unused byte positions are passed through the transmit section overhead processor unaltered, as though the TDIS input had been sampled high during the unused byte positions in the incoming frame.

DS:

The disable scrambling (DS) bit controls the scrambling of the transmit stream. When a logic one is written to the DS bit position, the scrambler is disabled. When a logic zero is written to the DS bit position, the scrambler is enabled.

Register 19H: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. If DFP is set high the A1 bytes are set to 76H instead of F6H.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the B1 section overhead byte. When DBIP8 is set high the B1 byte value is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the transmit outgoing stream. When DLOS is set high the TOUT[7:0] data bus is forced to 00H and the transmit serial stream (TSOUT or TXD+/-) is forced low.

Register 1AH: Transmit Z1

Bit	Type	Function	Default
Bit 7	R/W	Z1[7]	0
Bit 6	R/W	Z1[6]	0
Bit 5	R/W	Z1[5]	0
Bit 4	R/W	Z1[4]	0
Bit 3	R/W	Z1[3]	0
Bit 2	R/W	Z1[2]	0
Bit 1	R/W	Z1[1]	0
Bit 0	R/W	Z1[0]	0

In STS-3/STM-1 operation, the value 00h is inserted into the the Z1 byte for STS-1#2 and STS-1#3, irrespective of the value of register 1Ah. The TTOHEN and TDIS inputs take precedence over this insertion value.

Z1[7:0]:

The value written to these bit positions is inserted in the first Z1 byte position of the transmit stream. The Z1 byte is used to carry synchronization status messages between line terminating network elements. Z1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. Z1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The TTOHEN and TDIS inputs take precedence over the contents of this register.

Register 1BH: Receive Z1 (ENH=0)

Bit	Type	Function	Default
Bit 7	R	Z1[7]	X
Bit 6	R	Z1[6]	X
Bit 5	R	Z1[5]	X
Bit 4	R	Z1[4]	X
Bit 3	R	Z1[3]	X
Bit 2	R	Z1[2]	X
Bit 1	R	Z1[1]	X
Bit 0	R	Z1[0]	X

Z1[7:0]:

The first Z1 byte contained in the receive stream is extracted into this register when the ENH bit in the Mode Select register is a logic 0. The Z1 byte is used to carry synchronization status messages between line terminating network elements. Z1[7] is the most significant bit corresponding to bit 1, the first bit received. Z1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame (using the Z1E bit in the Master Control/Enable Register).

Register 1BH: Transmit Z0 (ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	Z0[7]	1
Bit 6	R/W	Z0[6]	1
Bit 5	R/W	Z0[5]	0
Bit 4	R/W	Z0[4]	0
Bit 3	R/W	Z0[3]	1
Bit 2	R/W	Z0[2]	1
Bit 1	R/W	Z0[1]	0
Bit 0	R/W	Z0[0]	0

Z0[7:0]:

Z0[7:0] contains the value inserted in Z0 bytes for STS-1 #2 and #3 in the transmit STS-3/STM-1 stream when the ENH bit in the Mode Select register and the Z0INS bit in the Master Control/Enable register are both logic 1. Z0[7] is the most significant bit corresponding to bit 1, the first bit transmitted. Z0[0] is the least significant bit, corresponding to bit 8, the last bit transmitted.

Address 1DH: Receive K1 (ENH=0)

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value when the ENH bit in the Mode Select register is a logic 0. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the Master Control/Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Address 1DH: AIS Control (ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SDINS	0
Bit 6	R/W	SFINS	0
Bit 5	R/W	LOFINS	1
Bit 4	R/W	LOSINS	1
Bit 3	R/W	RTIMINS	0
Bit 2	R/W	RTIUINS	0
Bit 1		Unused	X
Bit 0	R/W	DCCAIS	0

DCCAIS:

The DCCAIS bit enables the insertion of all ones in the section DCC (RSD) and the line DCC (RLD) when loss of frame (LOF) or LOS is declared. When DCCAIS is a logic 1, all ones is inserted in RSD and RLD when LOF or LOS is declared.

RTIUINS:

The RTIUINS bit enables the insertion of line AIS in the receive direction upon the declaration of section trace unstable when the ENH bit in the Mode Select register is a logic 1. If RTIUINS is a logic 1, line AIS is inserted into ROUT[7:0] when the current received section trace identifier message has not matched the previous message for eight consecutive messages. Line AIS is terminated when the current message becomes the accepted message.

RTIMINS:

The RTIMINS bit enables the insertion of line AIS in the receive direction upon the declaration of section trace mismatch when the ENH bit in the Mode Select register is a logic 1. If RTIMINS is a logic 1, line AIS is inserted into ROUT[7:0] when the accepted identifier message differs from the expected message. Line AIS is terminated when the accepted message matches the expected message.

LOSINS:

The LOSINS bit enables the insertion of line AIS in the receive direction upon the declaration of loss of signal (LOS) when the ENH bit in the Mode Select

register is a logic 1. If LOSINS is a logic 1, line AIS is inserted into ROUT[7:0] when LOS is declared. Line AIS is terminated when LOS is removed.

LOFINS:

The LOFINS bit enables the insertion of line AIS in the receive direction upon the declaration of loss of frame (LOF) when the ENH bit in the Mode Select register is a logic 1. If LOSINS is a logic 1, line AIS is inserted into ROUT[7:0] when LOS is declared. Line AIS is terminated when LOS is removed.

SFINS:

The SFINS bit enables the insertion of line AIS in the receive direction upon the declaration of signal fail (SF) when the ENH bit in the Mode Select register is a logic 1. If SFINS is a logic 1, line AIS is inserted into ROUT[7:0] when SF is declared. Line AIS is terminated when SF is removed.

SDINS:

The SDINS bit enables the insertion of line AIS in the receive direction upon the declaration of signal degrade (SD) when the ENH bit in the Mode Select register is a logic 1. If SDINS is a logic 1, line AIS is inserted into ROUT[7:0] when SD is declared. Line AIS is terminated when SD is removed.

Address 1EH: Receive K2 (ENH=0)

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value when the ENH bit in the Mode Select register is a logic 0. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the Master Control/Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Address 1EH: RDI Control (ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SDINS	0
Bit 6	R/W	SFINS	0
Bit 5	R/W	LOFINS	1
Bit 4	R/W	LOSINS	1
Bit 3	R/W	RTIMINS	0
Bit 2	R/W	RTIUINS	0
Bit 1	R/W	AISINS	1
Bit 0		Unused	X

AISINS:

The AISINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of line AIS. When AISINS is a logic 1, the detection of line AIS results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDRDI bit position in the receive ring control port (when the ring control ports are enabled).

RTIUINS:

The RTIUINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of section trace unstable. When RTIUINS is a logic 1, the detection of section trace unstable results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDRDI bit position in the receive ring control port (when the ring control ports are enabled).

RTIMINS:

The RTIMINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of section trace mismatch. When RTIMINS is a logic 1, the detection of section trace mismatch results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDRDI bit position in the receive ring control port (when the ring control ports are enabled).

LOSINS:

The AISINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of loss of signal. When LOSINS is a logic 1, the detection of LOS results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDRDI bit position in the receive ring control port (when the ring control ports are enabled).

LOFINS:

The LOFINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of loss of frame. When LOFINS is a logic 1, the detection of LOF results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDRDI bit position in the receive ring control port (when the ring control ports are enabled).

SFINS:

The SFINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of signal failure. When SFINS is a logic 1, the detection of SF results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDRDI bit position in the receive ring control port (when the ring control ports are enabled).

SDINS:

The SDINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of signal degrade. When SDINS is a logic 1, the detection of SD results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDRDI bit position in the receive ring control port (when the ring control ports are enabled).

Address 1FH: Configuration Input Port Status/Value

Bit	Type	Function	Default
Bit 7	R	SCPIV[3]	X
Bit 6	R	SCPIV[2]	X
Bit 5	R	SCPIV[1]	X
Bit 4	R	SCPIV[0]	X
Bit 3	R	SCPII[3]	X
Bit 2	R	SCPII[2]	X
Bit 1	R	SCPII[1]	X
Bit 0	R	SCPII[0]	X

SCPII[2:0]:

The SCPII[2:0] bits are interrupt indications. A logic one in any bit location indicates that an event has occurred on the corresponding SCPI[2:0] input. More specifically, a logic one in the SCPII[2] bit location indicates that the signal on SCPI[2] input has transitioned from logic zero to logic one (i.e. upon detection of a rising edge); a logic one in any of the SCPII[1:0] bit locations indicates that the signal on the corresponding SCPI[1:0] input has transitioned either from logic zero to logic one or from logic one to logic zero (i.e. upon a change of state). The SCPII[2:0] bits are cleared by reading this register. These register bits function independently from the Configuration input Port Enable register bits; the SCPII[2:0] bits will indicate events occurring on the SCPI[2:0] inputs regardless of whether or not these events are enabled to generate an interrupt. The SCPII[2] bit is reserved when the ENH bit in the Mode Select register are logic 1.

SCPII[3]:

The SCPII[3] bit is an interrupt indication. A logic one indicates that an event has occurred on the SCPI[3] input. More specifically, a logic one in the SCPII[3] bit location indicates that the signal on SCPI[3] input has transitioned from logic zero to logic one (i.e. upon detection of a rising edge). The SCPII[3] bit is cleared by reading this register. This register bit functions independently from the Configuration input Port Enable register bits; the SCPII[3] bit indicates events occurring on the SCPI[3] input regardless of whether or not this event is enabled to generate an interrupt. This register bit is reserved when the ENH bit in the Mode Select register are logic 1.

SCPIV[3:0]:

The SCPIV[3:0] bits are real-time input port state indications. A logic one in any bit location indicates that the signal on the corresponding SCPI[3:0] input is a logic one. A logic zero in any bit location indicates that the signal on the corresponding SCPI[3:0] input is a logic zero. The state of the SCPI[3:0] inputs are latched and held during a microprocessor read of this register.

Register 20H: Section Trace Control (ENH=0)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

LEN16:

The section trace message length bit (LEN16) selects the length of the section trace message to be 16 bytes or 64 bytes.

NOSYNC:

The section trace message synchronization disable bit (NOSYNC) disables the writing of the section trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the section trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zero section trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer are ignored and all-zeros bytes are provided to the TPOP block. When TNULL is set low the contents of the transmit section trace buffer is sent to TPOP. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The receive section trace identifier message mismatch interrupt enable bit (RTIMIE) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state activates the interrupt (INTB) output. When RTIMIE is set low, section trace identifier message state changes will not affect INTB.

RTIUIE:

The receive section trace identifier message unstable interrupt enable bit (RTIUIE) controls the activation of the interrupt output when the receive identifier message state changes from stable to unstable and vice versa. The unstable state is entered when the current identifier message differs from the previous message for eightconsecutive messages. The stable state is entered when the same identifier message is received for three or five consecutive messages as controlled by the PER5 bit. When RTIUIE is set high, changes in the received section trace identifier message stable/unstable state will activate the interrupt (INTB) output. When RTIUIE is set low, section trace identifier state changes will not affect INTB.

RRAMACC:

The receive RAM access control bit (RRAMACC) directs read and writes access to between the receive and transmit portion of the section trace buffers. When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

Register 20H: RASE Interrupt Enable (ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	Z1E	0
Bit 4	R/W	SFBERE	0
Bit 3	R/W	SDBERE	0
Bit 2	R/W	Unused	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

SDBERE:

The SDBERE bit is the interrupt enable for the signal degrade threshold alarm. When SDBERE is a logic one, an interrupt is generated when the SD alarm is declared or removed.

SFBERE:

The SFBERE bit is the interrupt enable for the signal fail threshold alarm. When SFBERE is a logic one, an interrupt is generated when the SF alarm is declared or removed.

Z1E:

The Z1 interrupt enable is an interrupt mask for changes in the received synchronization status. When Z1E is a logic one, an interrupt is generated when a new synchronization status message is extracted into the Receive Z1 register.

COAPSE:

The COAPS interrupt enable is an interrupt mask for changes in the received APS code. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value is extracted into the Receive K1 and Receive K2 registers.

PSBFE:

The PSBF interrupt enable is an interrupt mask for protection switch byte failure alarms. When PSBFE is a logic one, an interrupt is generated when PSBF is declared or removed.

Register 21H: Section Trace Status (ENH=0):

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the section trace status.

RTIMV:

The receive section trace identifier message mismatch status bit (RTIMV) reports the match/mismatch status of the identifier message framer. RTIMV is set high when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is set low when the accepted message matches the expected message.

RTIMI:

The receive section trace identifier mismatch interrupt status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

RTIUV:

The receive section trace identifier message unstable status bit (RTIUV) reports the stable/unstable status of the identifier message framer. RTIUV is set high when the current received section trace identifier message has not matched the previous message for eight consecutive messages. RTIUV is set low when the current message becomes the accepted message.

RTIUI:

The receive section trace identifier message unstable interrupt status bit (RTIUI) is set high when stable/unstable status of the trace identifier framer

changes state. This bit (and the interrupt) are cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the Section Trace Indirect Address register, and stays high until the initiated access has completed. At which point, BUSY is set low. This register should be polled to determine when new data is available in the Section Trace Indirect Data register.

Register 21H: RASE Interrupt Status (ENH=1)

Bit	Type	Function	Default
Bit 7	R	PSBFI	X
Bit 6	R	COAPSI	X
Bit 5	R	Z1I	X
Bit 4	R	SFBERI	X
Bit 3	R	SDBERI	X
Bit 2	R	SFBERV	X
Bit 1	R	SDBERV	X
Bit 0	R	PSBFV	X

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is set high) when twelve successive frames, where no three consecutive frames contain identical K1 bytes, have been received. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received. This bit position is reserved when the ENH bit in the Mode Select register is a logic 1.

SDBERV:

The SDBERV bit indicates the signal degrade threshold crossing alarm state. The alarm is declared (SDBERV is set high) when the bit error rate exceeds the threshold programmed in the SD Declaring Threshold registers. The alarm is removed (SDBERV is set low) when the bit error rate is below the threshold programmed in the SD Clearing Threshold registers.

SFBERV:

The SFBERV bit indicates the signal failure threshold crossing alarm state. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the SF Declaring Threshold registers. The alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the SF Clearing Threshold registers.

SDBERI:

The SDBERI bit is set high when the signal degrade threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

SFBERI:

The SFBERI bit is set high when the signal failure threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Z1I:

The Z1I bit is set high when a new synchronization status message has been extracted into the Receive Z1 register. This bit is cleared when the RASE Interrupt Status register is read.

COAPSI:

The COAPSI bit is set high when a new APS code value has been extracted into the Receive K1 and Receive K2 registers. This bit is cleared when the RASE Interrupt Status register is read.

PSBFI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Register 22H: Section Trace Indirect Address Register (ENH=0):

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the section trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set low, addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted into the J0 byte of the transmit stream. Addresses 64 to 127 are unused and must not be accessed.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the Section Trace Indirect Data register. When RWB is set low, a write access is initiated. The data in the Section Trace Indirect Data register will be written to the addressed location in the static page.

Register 22H: RASE Configuration/Control Register (ENH=1):

Bit	Type	Function	Default
Bit 7	R/W	Z1_CAP3	0
Bit 6	R/W	SFBERTEN	0
Bit 5	R/W	SFSMODE	0
Bit 4	R/W	SFCMODE	0
Bit 3	R/W	SDBERTEN	0
Bit 2	R/W	SDSMODE	0
Bit 1	R/W	SDCMODE	0
Bit 0	R/W	Unused	X

SDCMODE:

The SDCMODE alarm bit selects the SD BERM window size to use for clearing the SD alarm. When SDCMODE is a logic 0 the SD BERM clears the SD alarm using the same window size used for declaration. When SDCMODE is a logic 1 the SD BERM clears the SD alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the SD BERM Accumulation Period registers.

SDSMODE:

The SDSMODE bit selects the SD BERM saturation mode. When SDSMODE is a logic 0 the SD BERM limits the number of B2 errors accumulated in one frame period to the SD Saturation Threshold register value. When SDSMODE is a logic 1 the SD BERM limits the number of B2 errors accumulated in one window subtotal accumulation period to the SD Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the SD Accumulation Period register value.

SDBERTEN:

The SDBERTEN bit selects automatic monitoring of line bit error rate threshold events by the Signal Degrade Bit Error Rate Monitor (SD BERM). When SDBERTEN is a logic one, the SD BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SDBERTEN is a logic zero, the SD BERM BIP accumulation logic is disabled, and the BERM logic is reset to the declaration monitoring state.

All SD BERM accumulation period and threshold registers should be set up before SDBERTEN is written.

SFCMODE:

The SFCMODE alarm bit selects the SF BERM window size to use for clearing the SF alarm. When SFCMODE is a logic 0 the SF BERM clears the SF alarm using the same window size used for declaration. When SFCMODE is a logic 1 the SF BERM clears the SF alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the SF BERM Accumulation Period registers.

SFSMODE:

The SFSMODE bit selects the SF BERM saturation mode. When SFSMODE is a logic 0 the SF BERM limits the number of B2 errors accumulated in one frame period to the SF Saturation Threshold register value. When SFSMODE is a logic 1 the SF BERM limits the number of B2 errors accumulated in one window subtotal accumulation period to the SF Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the SF Accumulation Period register value.

SFBERTEN:

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure Bit Error Rate Monitor (SF BERM). When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to the declaration monitoring state.

All SF BERM accumulation period and threshold registers should be set up before SFBERTEN is written.

Z1_CAP3:

The Z1_CAP3 bit enables the Z1 Capture algorithm. When Z1_CAP3 is a logic one, the Z1 nibble must have the same value for three consecutive frames before writing the new value into the Receive Z1 register. When Z1_CAP3 is logic zero, the Z1 nibble value is written directly into the Receive Z1 register.

Register 23H: Section Trace Indirect Data Register (ENH=0)

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 23H: RASE SF Accumulation Period (LSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

Register 24H: RASE SF Accumulation Period (ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[15]	0
Bit 6	R/W	SFSAP[14]	0
Bit 5	R/W	SFSAP[13]	0
Bit 4	R/W	SFSAP[12]	0
Bit 3	R/W	SFSAP[11]	0
Bit 2	R/W	SFSAP[10]	0
Bit 1	R/W	SFSAP[9]	0
Bit 0	R/W	SFSAP[8]	0

Register 25H: RASE SF Accumulation Period (MSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

SFSAP[23:0]:

The SFSAP[23:0] bits represent the number of 8 kHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SF alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Register 26H: RASE SF Saturation Threshold (LSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SFSTH[7]	0
Bit 6	R/W	SFSTH[6]	0
Bit 5	R/W	SFSTH[5]	0
Bit 4	R/W	SFSTH[4]	0
Bit 3	R/W	SFSTH[3]	0
Bit 2	R/W	SFSTH[2]	0
Bit 1	R/W	SFSTH[1]	0
Bit 0	R/W	SFSTH[0]	0

Register 27H: RASE SF Saturation Threshold (MSB, ENH=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFSTH[11]	0
Bit 2	R/W	SFSTH[10]	0
Bit 1	R/W	SFSTH[9]	0
Bit 0	R/W	SFSTH[8]	0

SFSTH[11:0]:

The SFSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SF threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 28H: Section Trace AIS Insertion (ENH=0)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RTIU_AIS	0
Bit 0	R/W	RTIM_AIS	0

This register enables the insert of Line AIS into the ROUT[7:0] byte stream upon a section trace alarm condition.

RTIM_AIS:

The RTIM_AIS bit enables the insertion of Line AIS upon the declaration of a section trace mismatch. If RTIM_AIS is a logic one, Line AIS is inserted into ROUT[7:0] when the accepted identifier message differs from the expected message. Line AIS is terminated when the accepted message matches the expected message.

RTIU_AIS:

The RTIU_AIS bit enables the insertion of Line AIS upon the declaration of section trace unstable. If RTIU_AIS is a logic one, Line AIS is inserted into ROUT[7:0] when the current received section trace identifier message has not matched the previous message for eight consecutive messages. Line AIS is terminated when the current message becomes the accepted message.

Register 28H: RASE SF Declaring Threshold (LSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SFDTH[7]	0
Bit 6	R/W	SFDTH[6]	0
Bit 5	R/W	SFDTH[5]	0
Bit 4	R/W	SFDTH[4]	0
Bit 3	R/W	SFDTH[3]	0
Bit 2	R/W	SFDTH[2]	0
Bit 1	R/W	SFDTH[1]	0
Bit 0	R/W	SFDTH[0]	0

Register 29H: RASE SF Declaring Threshold (MSB, ENH=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFDTH[11]	0
Bit 2	R/W	SFDTH[10]	0
Bit 1	R/W	SFDTH[9]	0
Bit 0	R/W	SFDTH[8]	0

SFDTH[11:0]:

The SFDTH[11:0] value determines the threshold for the declaration of the SF alarm. The SF alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SFDTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 2AH: RASE SF Clearing Threshold (LSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SFCTH[7]	0
Bit 6	R/W	SFCTH[6]	0
Bit 5	R/W	SFCTH[5]	0
Bit 4	R/W	SFCTH[4]	0
Bit 3	R/W	SFCTH[3]	0
Bit 2	R/W	SFCTH[2]	0
Bit 1	R/W	SFCTH[1]	0
Bit 0	R/W	SFCTH[0]	0

Register 2BH: RASE SF Clearing Threshold (MSB, ENH=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFCTH[11]	0
Bit 2	R/W	SFCTH[10]	0
Bit 1	R/W	SFCTH[9]	0
Bit 0	R/W	SFCTH[8]	0

SFCTH[11:0]:

The SFCTH[11:0] value determines the threshold for the removal of the SF alarm. The SF alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SFCTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 2CH: RASE SD Accumulation Period (LSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[7]	0
Bit 6	R/W	SDSAP[6]	0
Bit 5	R/W	SDSAP[5]	0
Bit 4	R/W	SDSAP[4]	0
Bit 3	R/W	SDSAP[3]	0
Bit 2	R/W	SDSAP[2]	0
Bit 1	R/W	SDSAP[1]	0
Bit 0	R/W	SDSAP[0]	0

Register 2DH: RASE SD Accumulation Period (ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[15]	0
Bit 6	R/W	SDSAP[14]	0
Bit 5	R/W	SDSAP[13]	0
Bit 4	R/W	SDSAP[12]	0
Bit 3	R/W	SDSAP[11]	0
Bit 2	R/W	SDSAP[10]	0
Bit 1	R/W	SDSAP[9]	0
Bit 0	R/W	SDSAP[8]	0

Register 2EH: RASE SD Accumulation Period (MSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[23]	0
Bit 6	R/W	SDSAP[22]	0
Bit 5	R/W	SDSAP[21]	0
Bit 4	R/W	SDSAP[20]	0
Bit 3	R/W	SDSAP[19]	0
Bit 2	R/W	SDSAP[18]	0
Bit 1	R/W	SDSAP[17]	0
Bit 0	R/W	SDSAP[16]	0

SDSAP[23:0]:

The SDSAP[23:0] bits represent the number of 8 kHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SD alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Register 2FH: RASE SD Saturation Threshold (LSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SDSTH[7]	0
Bit 6	R/W	SDSTH[6]	0
Bit 5	R/W	SDSTH[5]	0
Bit 4	R/W	SDSTH[4]	0
Bit 3	R/W	SDSTH[3]	0
Bit 2	R/W	SDSTH[2]	0
Bit 1	R/W	SDSTH[1]	0
Bit 0	R/W	SDSTH[0]	0

Register 30H: RASE SD Saturation Threshold (MSB, ENH=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDSTH[11]	0
Bit 2	R/W	SDSTH[10]	0
Bit 1	R/W	SDSTH[9]	0
Bit 0	R/W	SDSTH[8]	0

SDSTH[11:0]:

The SDSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SD threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 31H: RASE SD Declaring Threshold (LSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SDDTH[7]	0
Bit 6	R/W	SDDTH[6]	0
Bit 5	R/W	SDDTH[5]	0
Bit 4	R/W	SDDTH[4]	0
Bit 3	R/W	SDDTH[3]	0
Bit 2	R/W	SDDTH[2]	0
Bit 1	R/W	SDDTH[1]	0
Bit 0	R/W	SDDTH[0]	0

Register 32H: RASE SD Declaring Threshold (MSB, ENH=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDDTH[11]	0
Bit 2	R/W	SDDTH[10]	0
Bit 1	R/W	SDDTH[9]	0
Bit 0	R/W	SDDTH[8]	0

SDDTH[11:0]:

The SDDTH[11:0] value determines the threshold for the declaration of the SD alarm. The SD alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SDDTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 33H: RASE SD Clearing Threshold (LSB, ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	SDCTH[7]	0
Bit 6	R/W	SDCTH[6]	0
Bit 5	R/W	SDCTH[5]	0
Bit 4	R/W	SDCTH[4]	0
Bit 3	R/W	SDCTH[3]	0
Bit 2	R/W	SDCTH[2]	0
Bit 1	R/W	SDCTH[1]	0
Bit 0	R/W	SDCTH[0]	0

Register 34H: RASE SD Clearing Threshold (MSB, ENH=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDCTH[11]	0
Bit 2	R/W	SDCTH[10]	0
Bit 1	R/W	SDCTH[9]	0
Bit 0	R/W	SDCTH[8]	0

SDCTH[11:0]:

The SDCTH[11:0] value determines the threshold for the removal of the SD alarm. The SD alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SDCTH[11:0] value. Refer to the Operations section for the recommended settings.

Address 35H: Receive K1 (ENH=1)

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value when the ENH bit in the Mode Select register is a logic 1. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Address 36H: Receive K2 (ENH=1)

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value when the ENH bit in the Mode Select register is a logic 1. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 37H: Receive Z1 (ENH=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	Z1[3]	X
Bit 2	R	Z1[2]	X
Bit 1	R	Z1[1]	X
Bit 0	R	Z1[0]	X

Z1[3:0]:

The lower nibble of the first Z1 byte contained in the receive stream is extracted into this register when the ENH bit in the Mode Select register is a logic 1. The Z1 byte is used to carry synchronization status messages between line terminating network elements. Z1[3] is the most significant bit corresponding to bit 5, the first bit received. Z1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame (using the Z1E bit in the RASE Interrupt Enable Register).

Register 38H: Section Trace Control (ENH=1):

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

LEN16:

The section trace message length bit (LEN16) selects the length of the section trace message to be 16 bytes or 64 bytes.

NOSYNC:

The section trace message synchronization disable bit (NOSYNC) disables the writing of the section trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the section trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zero section trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer are ignored and all-zeros bytes are provided to the TPOP block. When TNULL is set low the contents of the transmit section trace buffer is sent to TPOP. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The receive section trace identifier message mismatch interrupt enable bit (RTIMIE) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state activates the interrupt (INTB) output. When RTIMIE is set low, section trace identifier message state changes will not affect INTB.

RTIUIE:

The receive section trace identifier message unstable interrupt enable bit (RTIUIE) controls the activation of the interrupt output when the receive identifier message state changes from stable to unstable and vice versa. The unstable state is entered when the current identifier message differs from the previous message for six consecutive messages. The stable state is entered when the same identifier message is received for three or five consecutive messages as controlled by the PER5 bit. When RTIUIE is set high, changes in the received section trace identifier message stable/unstable state will activate the interrupt (INTB) output. When RTIUIE is set low, section trace identifier state changes will not affect INTB.

RRAMACC:

The receive RAM access control bit (RRAMACC) directs read and writes access to between the receive and transmit portion of the section trace buffers. When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

Register 39H: Section Trace Status (ENH=1):

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the section trace status.

RTIMV:

The receive section trace identifier message mismatch status bit (RTIMV) reports the match/mismatch status of the identifier message framer. RTIMV is set high when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is set low when the accepted message matches the expected message.

RTIMI:

The receive section trace identifier mismatch interrupt status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

RTIUV:

The receive section trace identifier message unstable status bit (RTIUV) reports the stable/unstable status of the identifier message framer. RTIUV is set high when the current received section trace identifier message has not matched the previous message for eight consecutive messages. RTIUV is set low when the current message becomes the accepted message.

RTIUI:

The receive section trace identifier message unstable interrupt status bit (RTIUI) is set high when stable/unstable status of the trace identifier framer

changes state. This bit (and the interrupt) are cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the Section Trace Indirect Address register, and stays high until the initiated access has completed. At which point, BUSY is set low. This register should be polled to determine when new data is available in the Section Trace Indirect Data register.

Register 3AH: Section Trace Indirect Address Register (ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the section trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set low, addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted into the J0 byte of the transmit stream. Addresses 64 to 127 are unused and must not be accessed.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the Section Trace Indirect Data register. When RWB is set low, a write access is initiated. The data in the Section Trace Indirect Data register will be written to the addressed location in the static page.

Register 3BH: Section Trace Indirect Data Register (ENH=1)

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs low causes all output pins and the data bus to be held in a high-impedance state, provided that the MBEB input is held high. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the STXC. Test mode registers (as opposed to normal mode registers) are selected when A[6] is high.

Test mode registers may also be used for board or module level testing. When all of the constituent TSBs within the STXC are placed in test mode 0, device inputs may be observed, and device outputs may be controlled via the microprocessor interface (refer to the "Test Mode 0" section below for details).

Table 2 - Test Mode Register Memory Map

A[6:0] Register	
00H-3FH	Reserved for normal registers
40H-42H	Reserved
43H	Master Test
44H-47H	TLOP Test Registers
48H-4CH	RLOP Test Registers
4DH-4FH	Reserved
50H-53H	RSOP Test Registers
54H-57H	Reserved
58H-5BH	TSOP Test Registers
5CH-5EH	Reserved
5FH	Reserved
60H-63H	RASE Test Registers
63H-77H	Reserved
78H-7CH	SPTB Test Registers
7DH-7FH	Reserved

Notes on Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2. Writeable register bits are not initialized upon reset unless otherwise noted.

Address 43H: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	W	FORCE_ENH	0
Bit 4	W	PMCTST	X
Bit 3	W	MOTOTST	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable STXC test features. All bits, except PMCTST, are reset to zero by a reset of the STXC.

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the STXC . While the HIZIO bit is a logic one, all output pins of the STXC except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the STXC for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

MOTOTST:

The MOTOTST bit is used to test the MOTOROLA interface. When MOTOTST is logic one and the MBEB input is logic zero the SCPI[2] and SCPI[3] inputs are used to replace the function of E and RWB, respectively. This is done because the fixed waveform shapes assigned to the RDB_E and WRB_RWB inputs can not be used to test MOTOROLA type microprocessor

interface logic. This mode is also used to test the D.C. drive capability of the D[7:0] device pins.

PMCTST:

The PMCTST bit is used to configure the STXC for PMC's manufacturing tests. When PMCTST is set to logic one, the STXC microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB to logic one or by writing a logic zero.

FORCE_ENH:

The FORCE_ENH bit is used to test the STXC enhanced mode. When FORCE_ENH is set to logic one, the ENH bit in the Mode Select register is forced to logic one. When FORCE_ENH is set to logic zero, the ENH bit is not forced to logic one.

Test Mode 0

In test mode 0, the STXC allows the logic levels on the device inputs to be observed through the microprocessor interface, and allows the device outputs to be controlled to either logic level through the microprocessor interface.

Test mode 0 is enabled by resetting the device (using the RSTB input, or the master reset and identity register), and then setting the IOTST bit in the Master Test register. The following addresses must then be written with the value 00H: 00H, 45H, 49H, 51H, 59H and 3DH. Write 05H to address 01H. With the exception of the SCPI[3:0] pins, applying a rising edge (logic zero to logic one transition) on the RICLK and TICLK inputs followed by a read from the following locations returns the value for the indicated pins. The current states of the SCPI[3:0] pins are reflected in the corresponding register locations.

Table 3 - Test Mode 0 Input Observation

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1AH	TSER	RSER					TTOH	TTOHEN
1FH	SCPI[3]	SCPI[2]	SCPI[1]	SCPI[0]				
40H							RSICLK	RSIN
44H	TDIS	TLOW	TLD	TRDI/	TAPS TRCPFP		TIFP	
46H	TIN[7]	TIN[6]	TIN[5]	TIN[4]	TIN[3]	TIN[2]	TIN[1]	TIN[0]
50H						RLAIS/ TRCPCLK	RIFP*	RICLK

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
52H*	RIN[7]	RIN[6]	RIN[5]	RIN[4]	RIN[3]	RIN[2]	RIN[1]	RIN[0]
58H	TSUC**	TSOW**	TSD			TLAIS/ TRCPDAT		

Notes:

* Two RICLK cycles are required before the read. RSER must be tied low in order to observe the RIN[7:0] inputs.

** To propagate TSUC and TSOW, 00H then 10H must be written to 44H followed by a rising edge on TICLK.

A write to one of the following locations forces each output to the value in the corresponding bit position. They need be followed by a rising edge (logic one to logic zero transition) on the RICLK and TICLK inputs, with the exception of these outputs: RSOW, RSD, RSDCLK, RSUC, GTICLK, TSDCLK, TOFP, TSOUT, SCPO[5:0].

Table 4 - Test Mode 0 Output Control

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14H			SCPO[5]	SCPO[4]	SCPO[3]	SCPO[2]	SCPO[1]	SCPO[0]
1AH		RTOHFP	RTOHCLK	RTOH	TTOHFP	TTOHCLK		
40H								GRICLK
44H			TAPSCLK	TOWCLK	TLDCLK			
48H	RAPS	B2E*	B2E*	RDI/ RRCPCLK	LAIS/ RRCPDAT	ROFP		
4AH			INTB**	RAPSCLK	RLD	RLDCLK	RLOW	ROWCLK
4BH	ROUT[7]	ROUT[6]	ROUT[5]	ROUT[4]	ROUT[3]	ROUT[2]	ROUT[1]	ROUT[0]
50H	B1E*	B1E*	LOF	OOF	LOS/ RRCPFP			
52H		INTB**	RSOW		RSD	RSDCLK	RSUC	
58H				GTICLK	TSDCLK	TOFP		
5AH	TOUT[7]	TOUT[6]	TOUT[5]	TOUT[4]	TOUT[3]	TOUT[2]	TOUT[1]	TOUT[0]/ FPOUT
5CH								TSOUT
60H					INTB**			

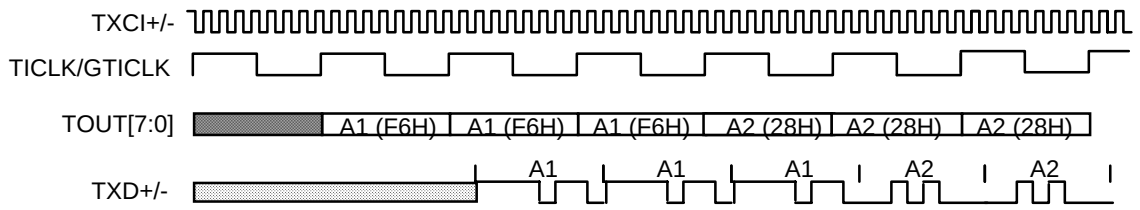
Notes:

* Both B1E bits must be a logic one before the B1E output is asserted high. Likewise, both B2E bits must be a logic one before the B2E output is asserted high.

** Writing a logic one to any of the INTB bits forces the INTB output low provided the enable bits are set in the Master Control/Enable register.

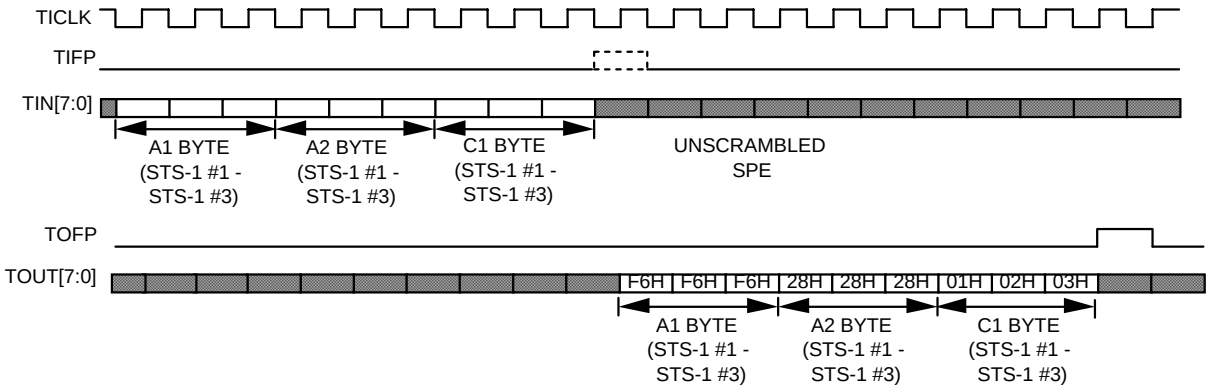
12 FUNCTIONAL TIMING

Figure 2 - STS-3 Bit Serial Transmit Frame Pattern and Data Alignment



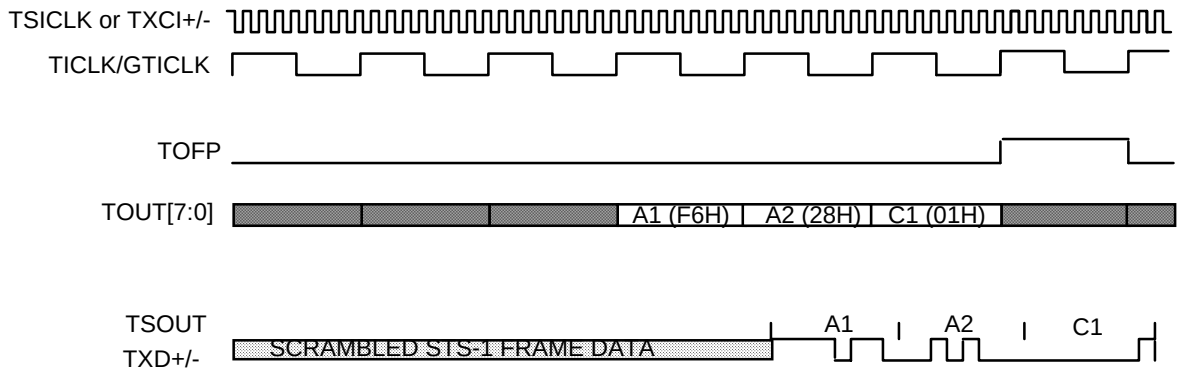
The STS-3 bit serial transmit frame pulse and data alignment timing diagram (Figure 2) illustrates bit serial operation for an STS-3 application (TSER=1). The STS-3 transmit clock, TXCI+/-, is divided by eight to produce the byte serial transmit clock, GTICLK. GTICLK must be externally connected to TICLK, and bytes are then "pulled" from an upstream path overhead insertion/payload mapping device.

Figure 3 - STS-3 Byte Serial Transmit Frame Pulse and Data Alignment



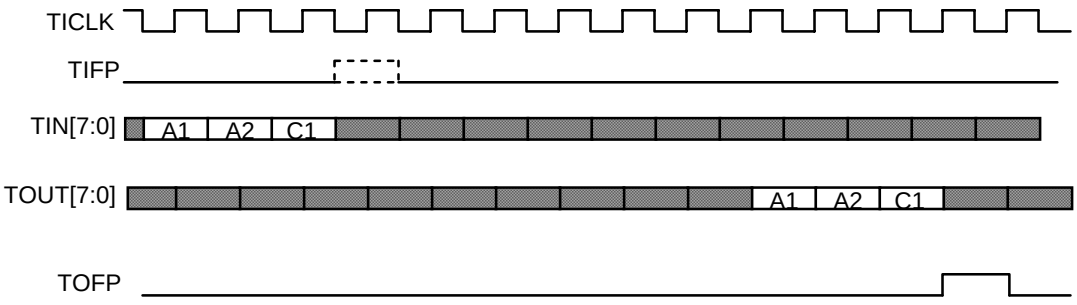
The STS-3 transmit frame pulse and data alignment timing diagram (Figure 3) illustrates the transmit frame pulse input/output alignment for an STS-3 (STM-1) frame when the byte serial interface is enabled (TSER=0). The input frame pulse is aligned to the byte immediately following the last Z0 byte, and it is not always necessary for this pulse to be present.

Figure 4 - STS-1 Bit Serial Transmit Frame Pulse and Data Alignment



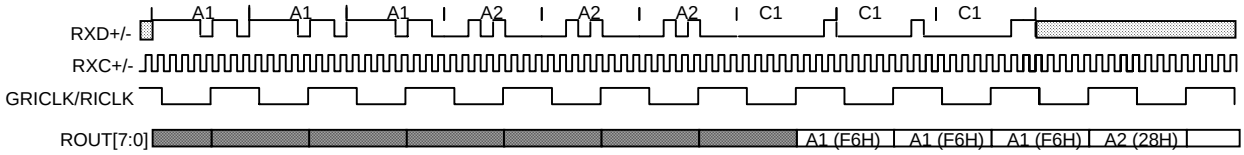
The STS-1 bit serial transmit frame pulse and data alignment timing diagram (Figure 4) illustrates bit serial operation for an STS-1 application (TSER=1). The STS-1 transmit clock, TSICLK or TXCI+/-, is divided by eight to produce the byte serial transmit clock, GTICLK. GTICLK must be connected externally to TCLK, and bytes are "pulled" from an upstream path overhead insertion/payload mapping device.

Figure 5 - STS-1 Byte Serial Transmit Frame Pulse and Data Alignment



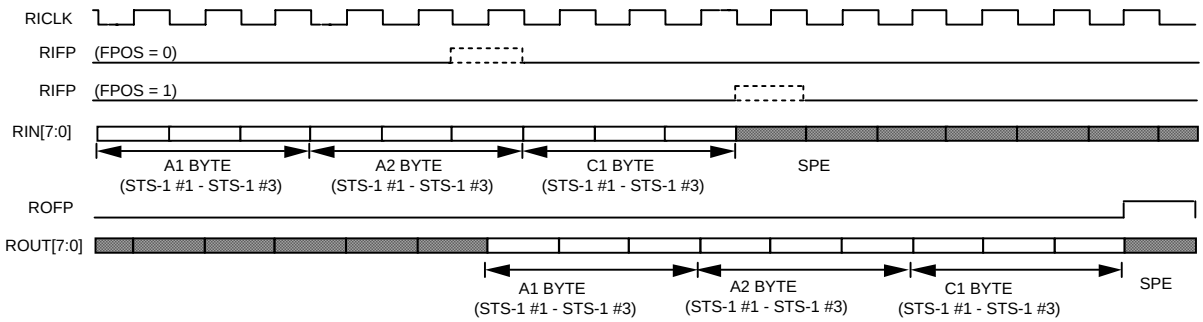
The STS-1 byte serial transmit frame pulse and data alignment timing diagram (Figure 5) illustrates the transmit frame pulse input/output alignment for an STS-1 frame when the byte serial interface is enabled (TSER=0). The input frame pulse is aligned to the byte immediately following the last Z0 byte, and it is not always necessary for this pulse to be present.

Figure 6 - STS-3 Bit Serial Receive Frame Pattern and Data Alignment



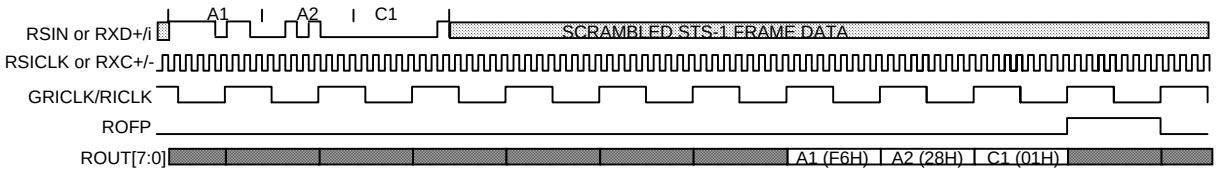
The STS-3 Bit Serial Receive Frame Pulse and Data Alignment timing diagram (Figure 6) illustrates the receive frame alignment for an STS-3 frame when the bit serial interface is enabled (RSER=1). The STXC converts the bit serial STS-3 stream, RXD+/-, to byte serial format. Output GRICLK is a divide by eight of the bit serial line clock, RSICLK, and must be externally connected to RICLK for proper operation. The ROFP output is set high during the first SPE byte of the first row of the SONET frame (immediately following the last Z0 byte), and may be used by downstream circuitry for frame alignment. While the STXC is out-of-frame, ROFP is updated based on the last frame alignment.

Figure 7 - STS-3 Byte Serial Receive Frame Pulse and Data Alignment



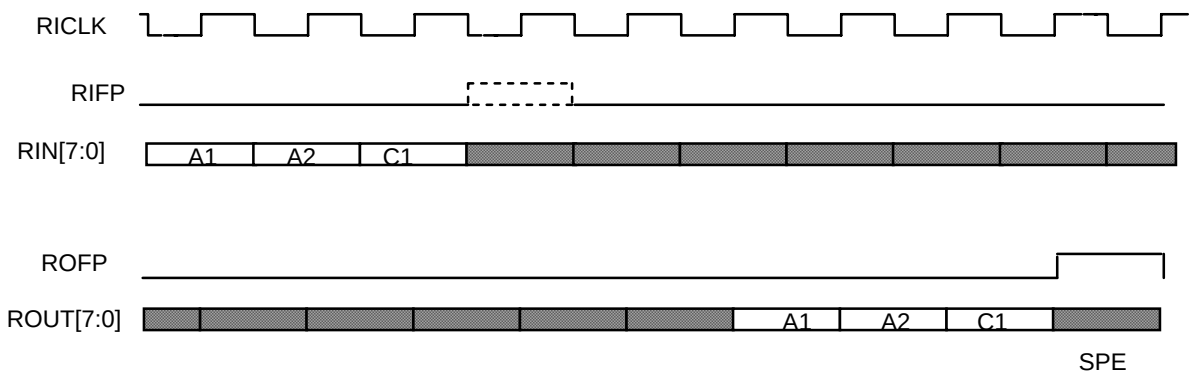
The STS-3 Byte Serial Receive Frame Pulse and Data Alignment timing diagram (Figure 7) illustrates the receive frame pulse input/output alignment for an STS-3/STM-1 frame when the byte serial interface is enabled (RSER=0). The FPOS bit in the Master Configuration Register controls the expected location of the externally applied frame indication input, RIFP as indicated in the diagram. The ROFP output is set high during the first SPE byte of the first row of the SONET frame (immediately following the last Z0 byte), and may be used by downstream circuitry for frame alignment. While the STXC is out-of-frame, ROFP is updated based on the last frame alignment.

Figure 8 - STS-1 Bit Serial Receive Frame Pulse and Data Alignment



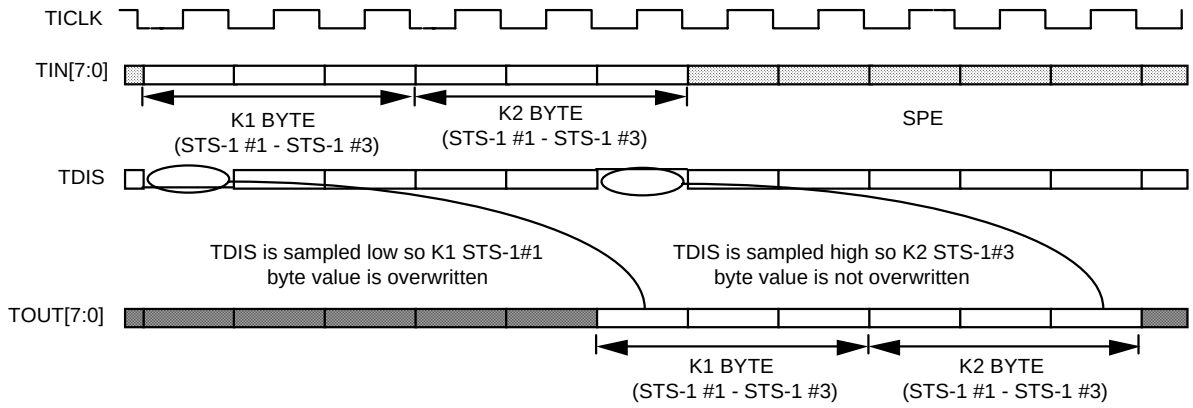
The STS-1 Bit Serial Receive Frame Pulse and Data Alignment timing diagram (Figure 8) illustrates the receive frame alignment for an STS-1 frame when the bit serial interface is enabled (RSER=1). The STXC converts the bit serial STS-1 stream, RSIN or RXD+/-, to byte serial format. Output GRICLK is a divide by eight of the bit serial line clock, RSICLK or RXC+/-, and must be externally connected to RICLK for proper operation. The ROFP output is set high during the first SPE byte of the first row of the SONET frame (immediately following the last Z0 byte), and may be used by downstream circuitry for frame alignment. While the STXC is out-of-frame, ROFP is updated based on the last frame alignment.

Figure 9 - STS-1 Byte Serial Receive Frame Pulse and Data Alignment



The STS-1 Byte Serial Receive Frame Pulse and Data Alignment timing diagram (Figure 9) illustrates the receive frame alignment for an STS-1 frame when the byte serial interface is enabled (RSER=0). The ROFP output is set high during the first SPE byte of the first row of the SONET frame (immediately following the last Z0 byte), and may be used by downstream circuitry for frame alignment. While the STXC is out-of-frame, ROFP is updated based on the last frame alignment.

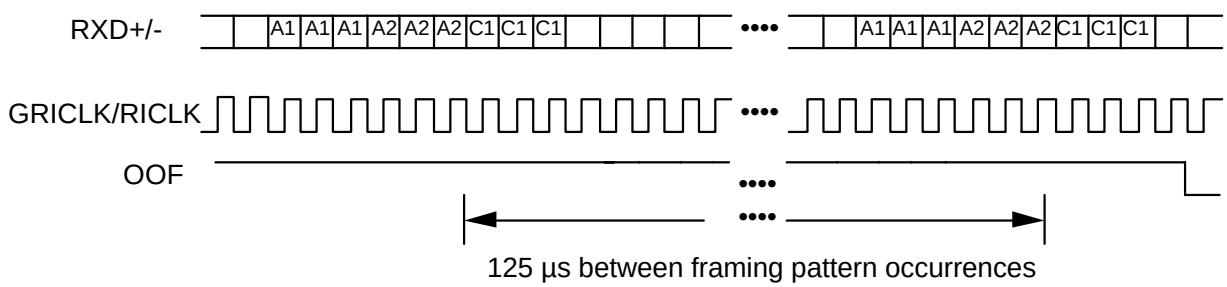
Figure 10 - Transport Overhead Overwrite Enable and Disable



The transport overhead overwrite enable and disable timing diagram (Figure 10) illustrates the operation of the TOH overwrite disable feature. It is assumed that the TTOHEN input is low. The diagram shows input TDIS sampled low during the K1 STS-1 #1 byte and then sampled high during the K2 STS-1 #3 byte. Since TDIS was low the byte value in the K1 STS-1 #1 byte position for the output data TOUT[7:0] is overwritten with the value shifted in on TAPS (or the value contained in the Transmit K1/K2 Registers depending on the level of the APSREG bit in the Master Control/Enable Register). However, the byte value in the K2 STS-1 #3 position for the output data TOUT[7:0] is not overwritten with an all zero byte because TDIS was sampled high during this byte position on the input data stream.

An error insertion feature is also provided for the B1 and B2 byte positions. When TDIS is held high during any or all of the B1 or B2 byte positions, the associated data sampled on TIN[7:0] is used as an error insertion mask. A logic one in a given bit position causes the inversion of the corresponding B1 or B2 bit position prior to transmission. A logic zero in a given bit position causes the corresponding B1 or B2 bit position to be transmitted uncorrupted.

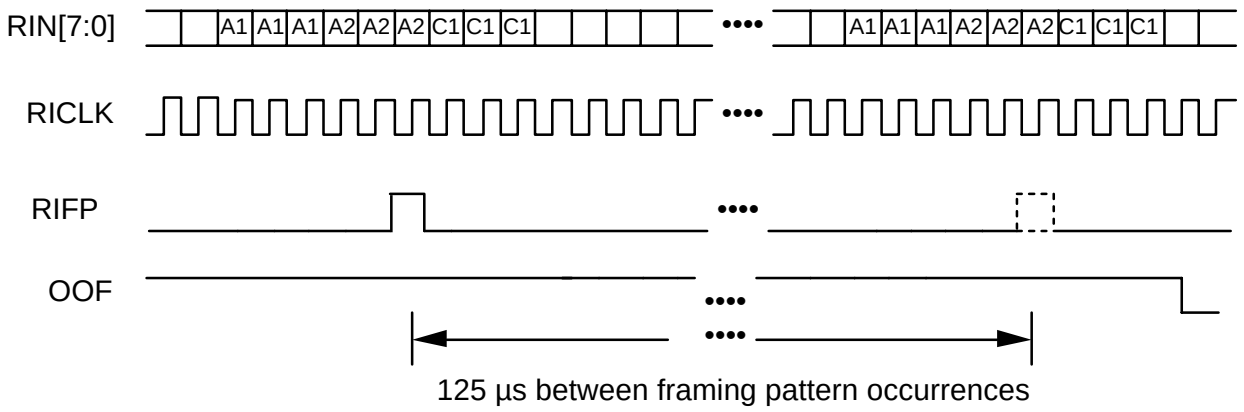
Figure 11 - In Frame Declaration (bit serial interface, RSER=1)



The In Frame Declaration (bit serial interface, RSER = 1) timing Figure 11) illustrates the declaration of in-frame by the STXC when processing a 155.52 Mbit/s stream on RXD+/RXD-. The STXC searches the incoming stream for an occurrence of the 48 bit framing pattern (three A1 bytes followed by three A2 bytes). In frame is declared when the framing pattern (or a 12 bit subset if the ALGO2 register bit is set) is observed for the second time, 125 µs after the first occurrence, and in the intervening period (125 µs), no occurrences of the 48 bit framing pattern were detected. This algorithm results in a maximum average reframe time of 250 µs in the absence of mimic framing patterns.

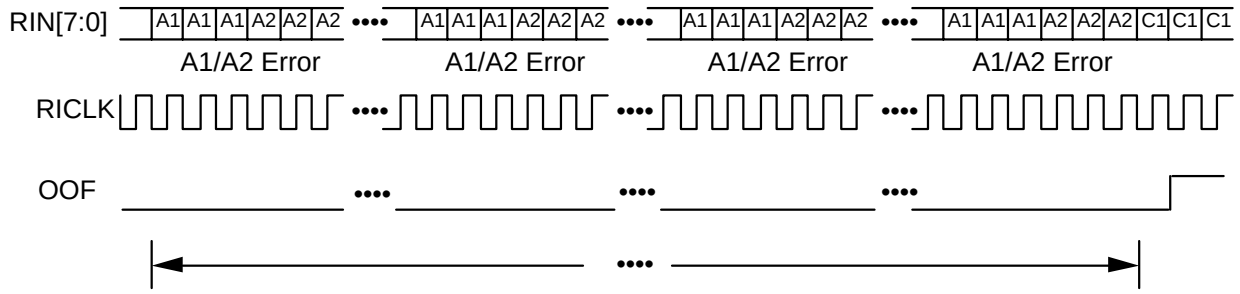
GRICLK is generated by dividing the bit serial clock (RXC+, RXC-) by eight and must be connected externally to the RICLK input. The falling edge of RICLK is used to update OOF.

Figure 12 - In Frame Declaration (byte serial interface, RSER=0)



The In Frame Declaration (byte serial interface, RSER=0) Timing Diagram (Figure 12) illustrates the declaration of in-frame by the STXC when processing a 19.44 Mbyte/s stream on RIN[7:0]. An upstream serial to parallel converter, or byte interleaved demultiplexer indicates the frame location using the RIFP input. The byte position marked by RIFP may be controlled using the FPOS bit in the Master Configuration Register. Figure 12 illustrates the RIFP alignment when FPOS is set to a logic zero. The frame verification is initialized by a pulse on RIFP while the STXC is out of frame. In frame is declared if the framing pattern is observed in the correct byte positions in the following frame, and in the intervening period (125 µs) no additional pulses were present on RIFP. The STXC ignores pulses on RIFP while in frame. This algorithm results in a maximum average reframe time of 250 µs in the absence of mimic framing patterns.

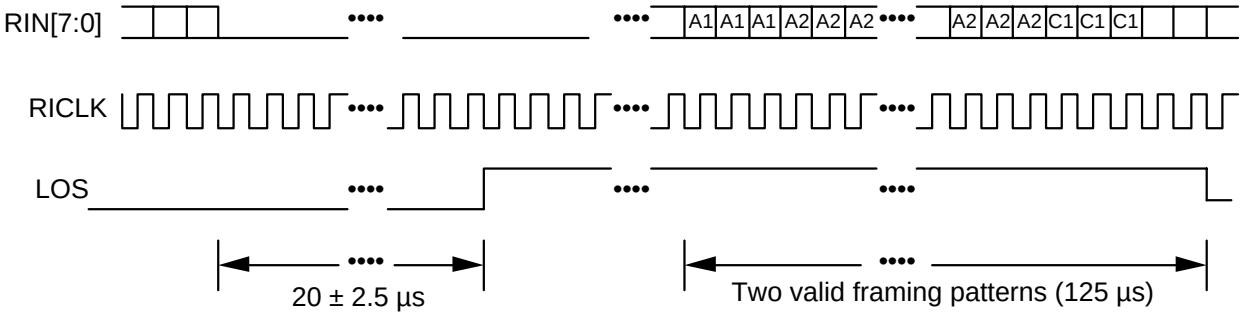
Figure 13 - Out of Frame Declaration



Four consecutive frames containing framing pattern errors

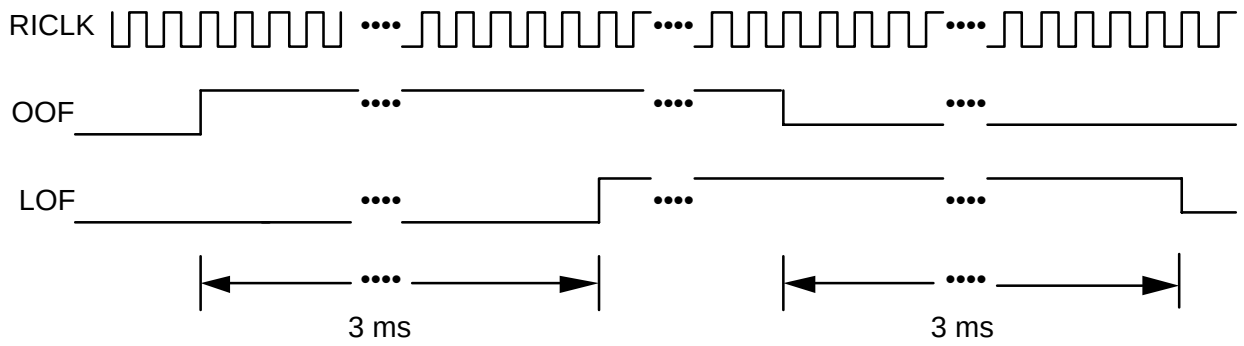
The out of frame declaration timing diagram (Figure 13) illustrates the declaration of out of frame. In an STS-3 (STM-1) stream, the framing pattern is a 48 bit sequence that repeats once per frame (for the purposes of OOF declaration, the framing pattern may be modified using the ALGO2 bit in the RSOP Control Register). Out of frame is declared when one or more errors are detected in this pattern for four consecutive frames as illustrated. In the presence of random data, out of frame will normally be declared within 500 µs.

Figure 14 - Loss of Signal Declaration/Removal



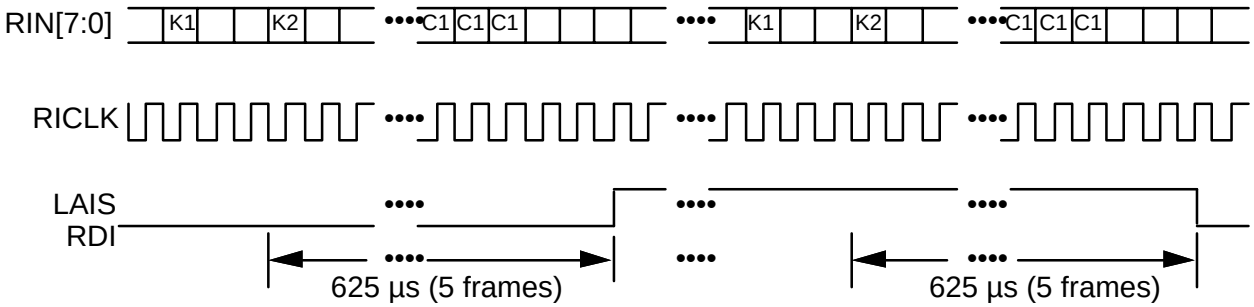
The loss of signal declaration/removal timing diagram (Figure 14) illustrates the operation of the LOS output. LOS is declared when a violating period of all zeros (20 ±2.5 µs) is observed on RIN[7:0] (note the same criteria applies to RXD+/- and RSIN when processing bit serial streams). LOS is removed when two valid framing patterns are observed, and in the intervening period (125 µs), no violating periods of all zeros is observed.

Figure 15 - Loss of Frame Declaration/Removal



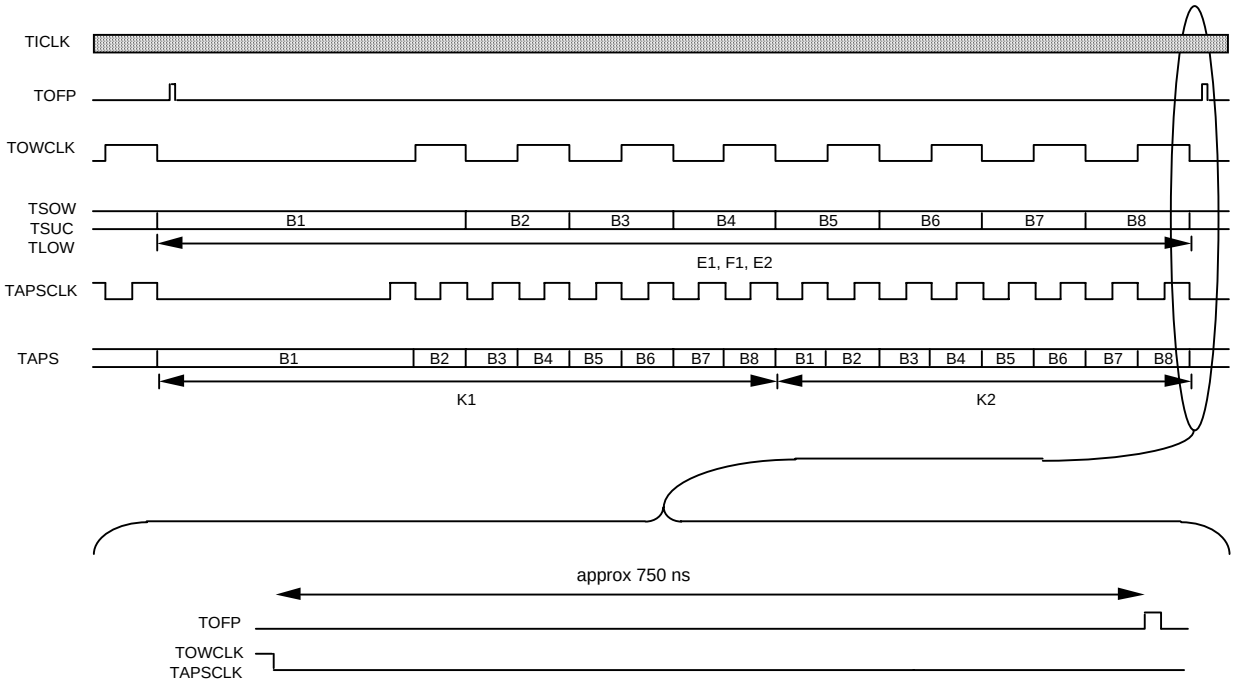
The loss of frame declaration/removal timing diagram (Figure 15) illustrates the operation of the LOF output. LOF is an integrated version of OOF. LOF is declared when an out of frame condition persists for 3 ms. LOF is removed when an in frame condition persists for 3 ms.

Figure 16 - Line AIS and Line RDI Declaration/Removal



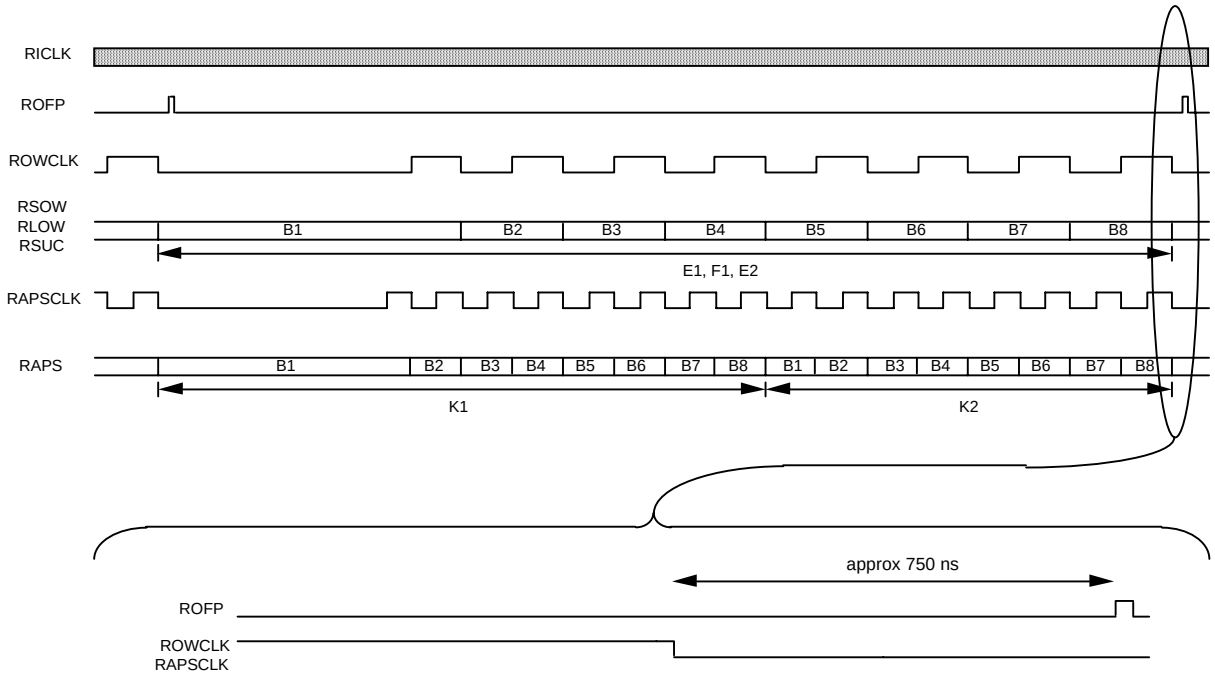
The line AIS and line RDI declaration/removal timing diagram (Figure 16) illustrates the operation of the LAIS and RDI outputs. A byte serial STS-3 (STM-1) stream is shown for illustrative purposes. LAIS (RDI) is declared when the binary pattern '111' ('110') is observed in bits 6,7, and 8 of the K2 byte for three or five consecutive frames. LAIS (RDI) is removed when any pattern other than the binary pattern '111' ('110') is observed in bits 6,7, and 8 of the K2 byte for three or five consecutive frames.

Figure 17 - Transmit Overhead Clock and Data Alignment



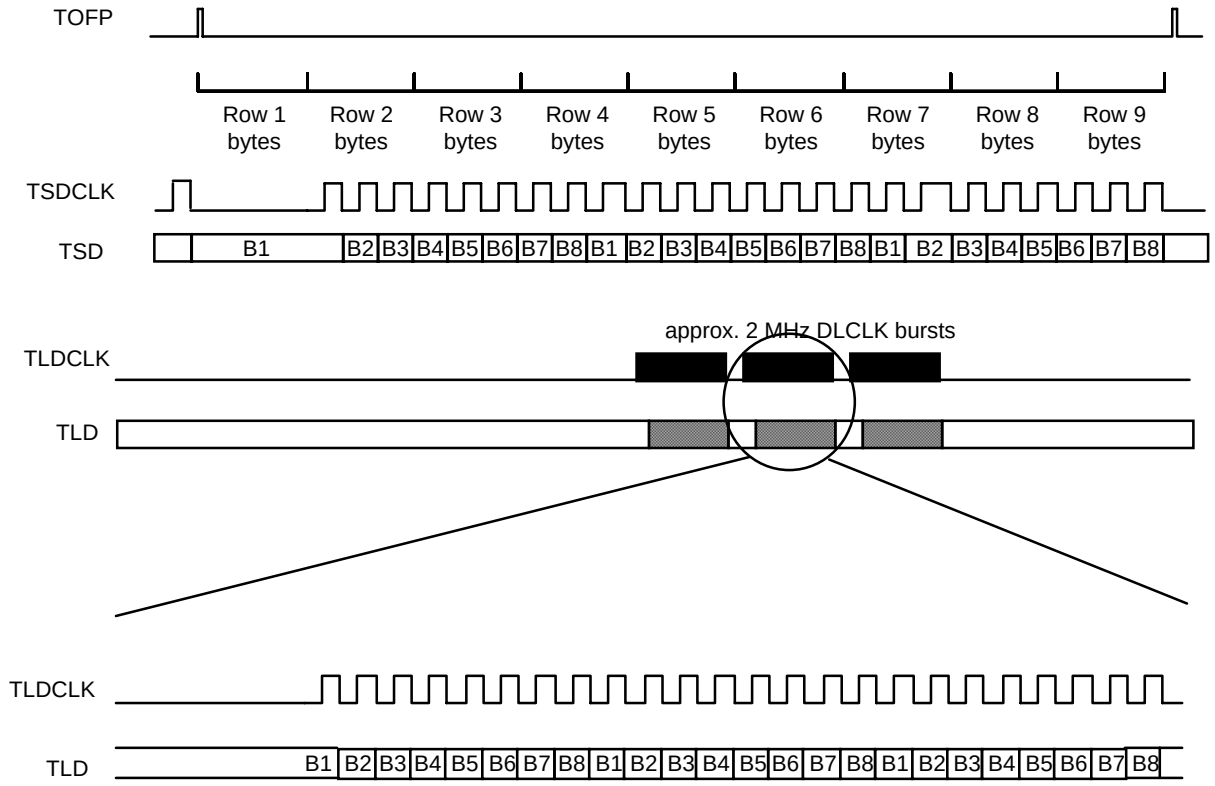
The transmit overhead clock and data alignment timing diagram (Figure 17) shows the relationship between the TSOW, TLOW, TSUC and TAPS serial data inputs and their associated clocks, TOWCLK and TAPSCLK. TOWCLK is a 72 kHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. TAPSCLK is a 144 kHz 50% duty cycle clock that is gapped to produce a 128 kHz nominal rate and is aligned as shown in the timing diagram. The E1, E2, F1, K1 and K2 bytes shifted into the STXC on TSOW, TLOW, TSUC, and TAPS in the frame shown are inserted in the corresponding transport overhead channels in the next frame.

Figure 18 - Receive Overhead Clock and Data Alignment



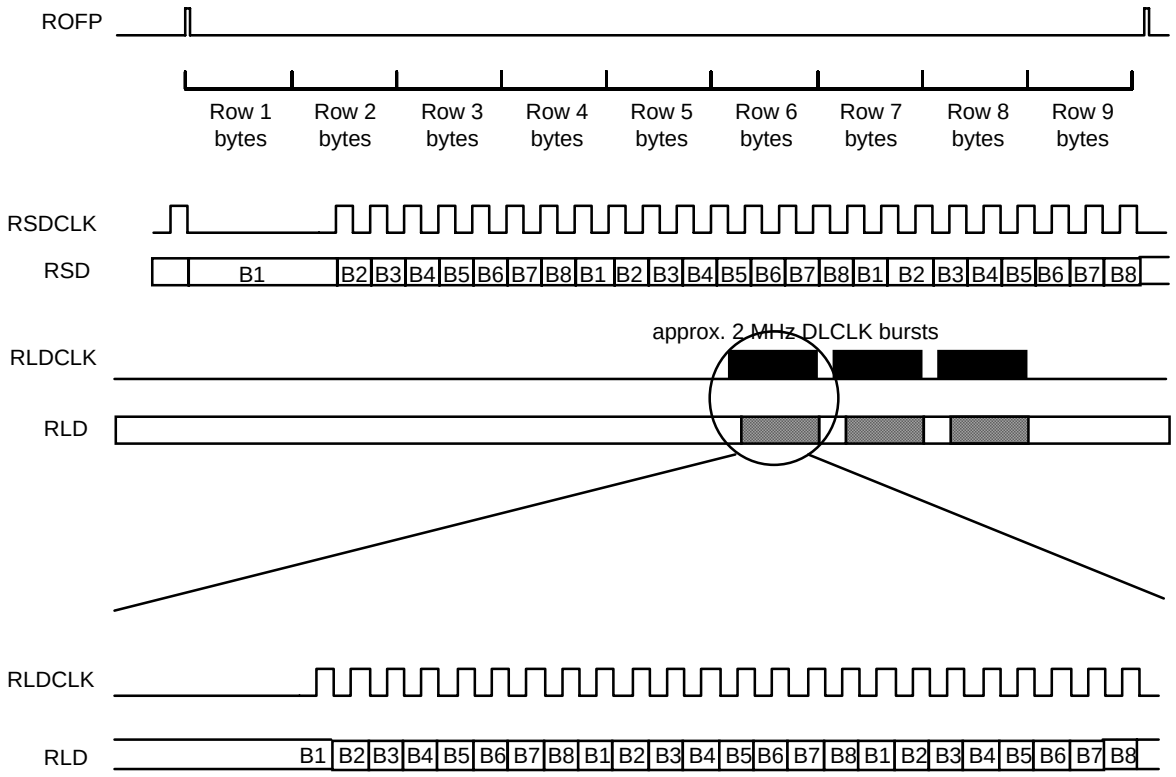
The receive overhead alignment timing diagram (Figure 18) shows the relationship between the RSOW, RSUC, RLOW, and RAPS serial data outputs and their associated clocks, ROWCLK and RAPSCLK. ROWCLK is a 72 kHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. RAPSCLK is a 144 kHz 50% duty cycle clock that is gapped to produce a 128 kHz nominal rate and is aligned as shown in the timing diagram. The E1, F1, E2, K1 and K2 bytes shifted out of the STXC on RSOW, RSUC, RLOW, and RAPS in the frame shown are extracted from the corresponding transport overhead channels in the previous frame.

Figure 19 - Transmit Data Link Clock and Data Alignment



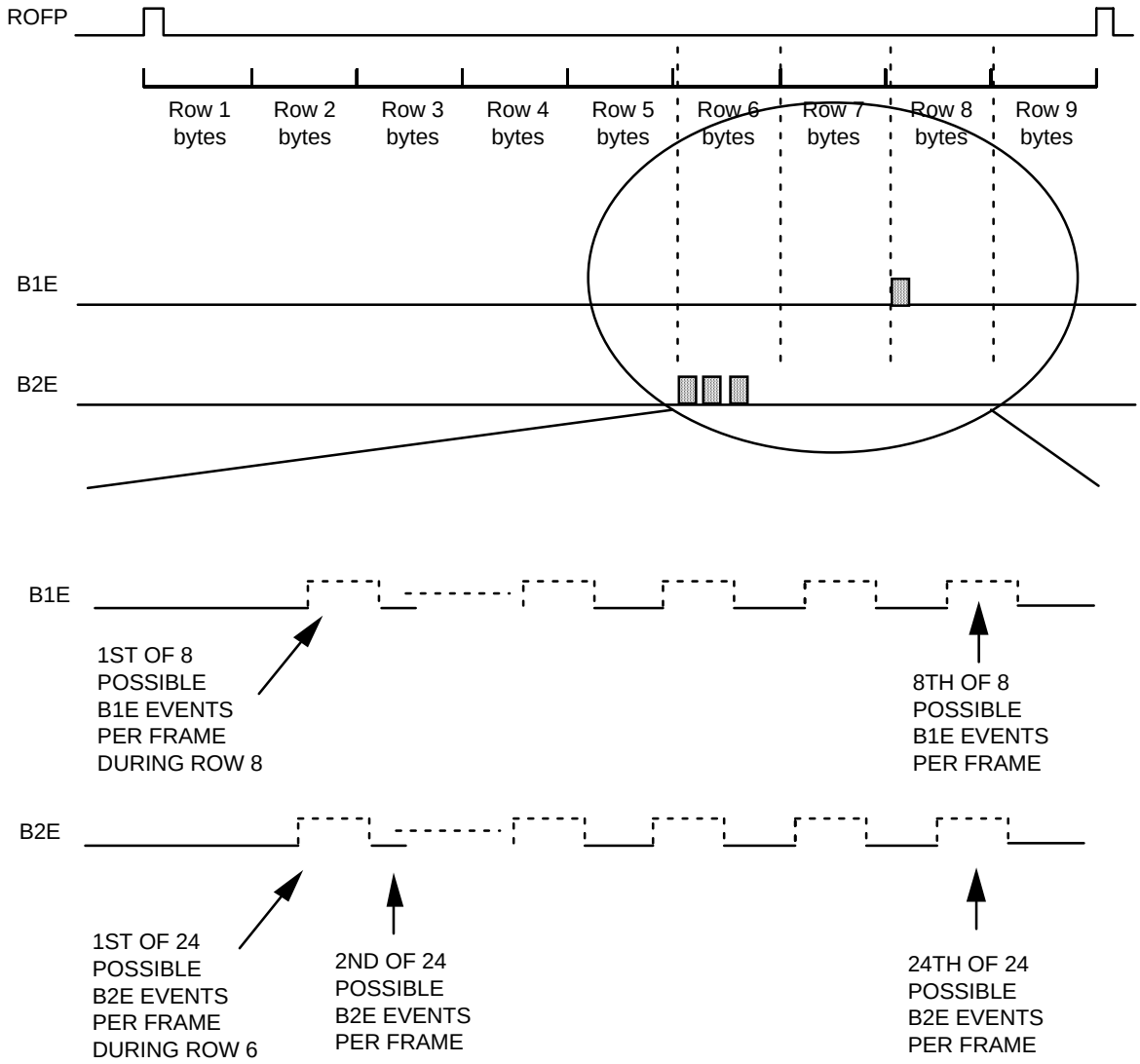
The transmit data link clock and data alignment timing diagram (Figure 19) shows the relationship between the TSD, and TLD serial data inputs, and their associated clocks, TSDCLK and TLDCLK respectively. TSDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate that is aligned with TOFP as shown in the timing diagram. TLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate that is aligned with TOFP as shown in the timing diagram. TSD (TLD) is sampled on the rising TSDCLK (TLDCLK) edge. The D1-D3, and D4-D12 bytes shifted into the STXC in the frame shown are inserted in the corresponding transport overhead channels in the following frame.

Figure 20 - Receive Data Link Clock and Data Alignment



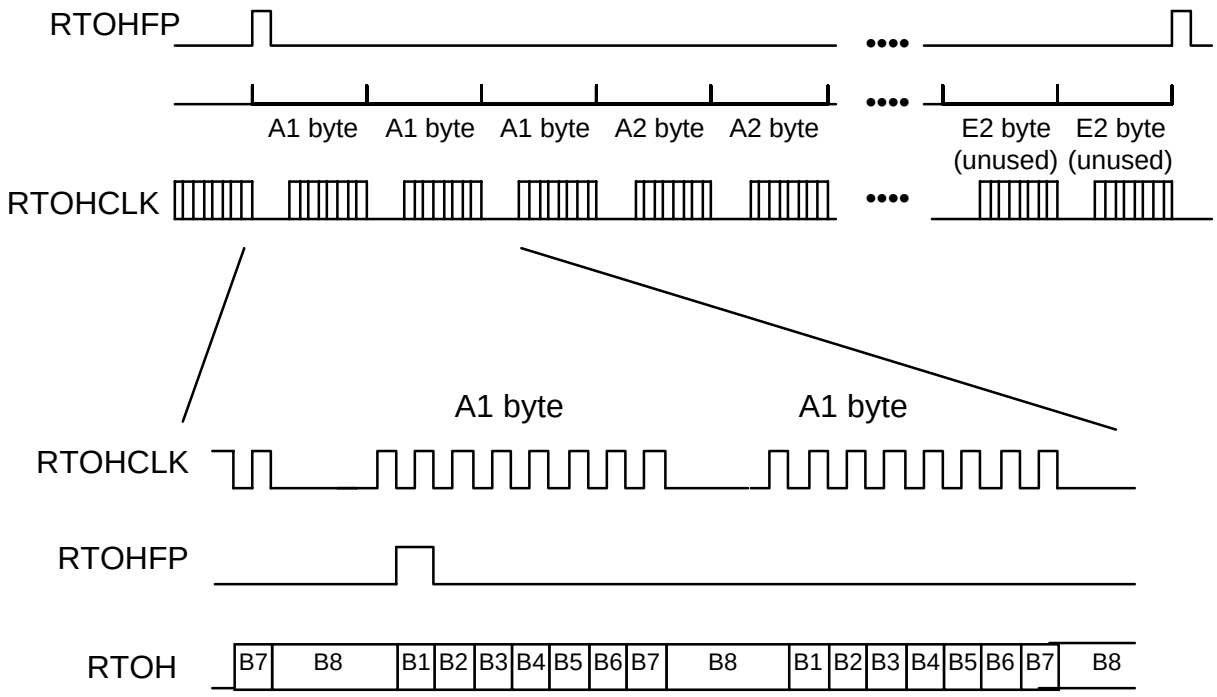
The receive data link clock and data alignment timing diagram (Figure 20) shows the relationship between the RSD, and RLD serial data outputs, and their associated clocks, RSDCLK and RLDCLK. RSDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate that is aligned with ROFP as shown in the timing diagram. RLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate that is aligned with ROFP as shown in the timing diagram. RSD (RLD) is updated on the falling RSDCLK (RLDCLK) edge. The D1-D3, and D4-D12 bytes shifted out of the STXC in the frame shown are extracted from the corresponding receive line overhead channels in the previous frame.

Figure 21 - B1 and B2 Error Event Occurrence



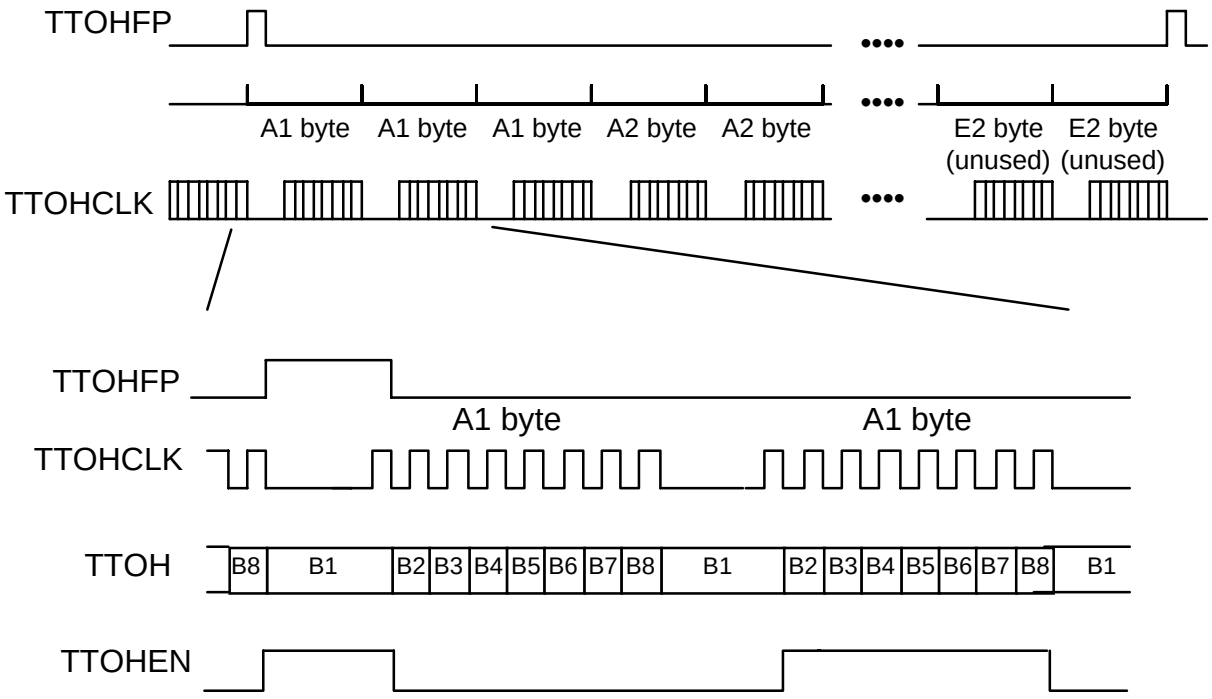
The B1 and B2 Error Event Occurrence timing diagram (Figure 21) shows the location of B1 and B2 error events in an STS-3 frame. Up to 8 B1 errors and 24 B2 errors may be detected per frame. The B1 and B2 error clocks, B1E and B2E, pulse once for every B1 and B2 error detected. These signals may be used to accumulate B1 and B2 errors externally.

Figure 22 - Transport Overhead Extraction



The transport overhead extraction timing diagram (Figure 22) illustrates the transport overhead extraction interface for STS-3. The transport overhead extraction clock, RTOHCLK is nominally a 5.184 MHz clock (1.728 MHz for an STS-1 stream), and is derived from the receive line clock, RICLK. The entire transport overhead (the complete 9 row by 9 column structure) is extracted for the STS-3 stream and is serialized on RTOH over a frame period (125 µs).

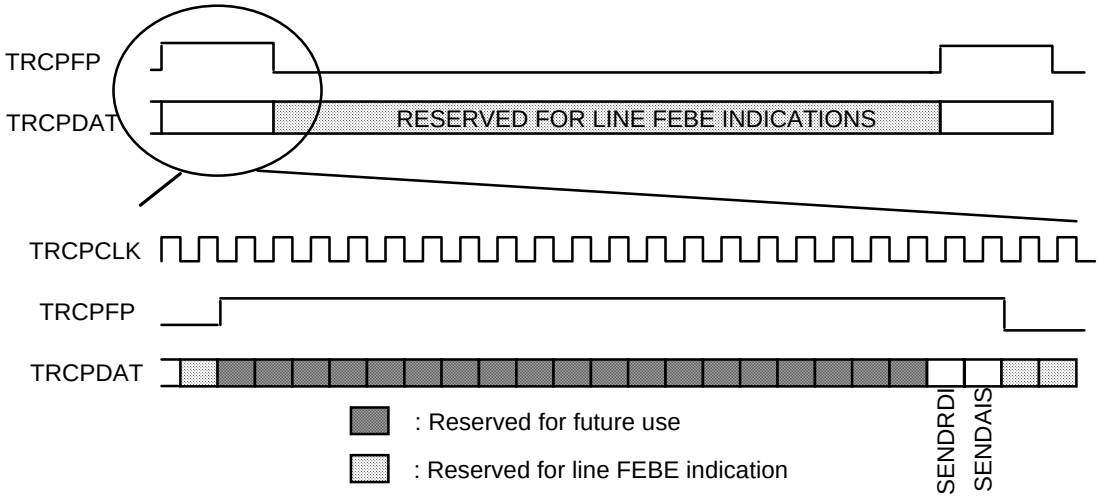
Figure 23 - Transport Overhead Insertion



The transport overhead insertion timing diagram (Figure 23) illustrates the transport overhead insertion interface. Output TTOHCLK is nominally a 5.184 MHz clock (1.728 MHz for an STS-1 stream), and is used to update output TTOHFP, and to sample input TTOH and TTOHEN. It is assumed that the TDIS input is held low. A high level on TDIS takes precedence over the transport overhead insertion interface. The value sampled on TTOHEN during the first overhead bit position of a given set of overhead bytes determines whether the value sampled on TTOH is inserted in the STS-3 stream. In figure 22, TTOHINS is held high during the bit 1 position of the A1 byte in the TTOH stream. The eight bit values sampled on input TTOH during the first A1 byte period are inserted in the first A1 byte position in the STS-3 (STM-1) stream. Similarly, TTOHINS is held low during the bit 1 position of the second A1 byte. The default value (F6H) is inserted in the second A1 byte position in the STS-3 (STM-1) stream.

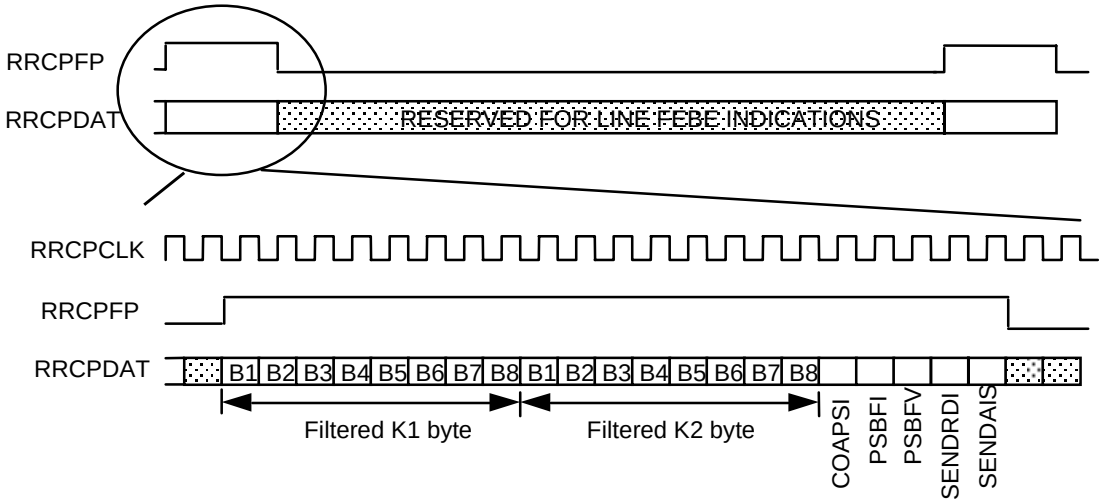
An error insertion feature is also provided for the B1, and B2 byte positions. When TTOH is held high during any of the bit positions corresponding to these bytes, the corresponding bit is inverted before being inserted in the STS-3 (STM-1) stream (TTOHEN must be sampled high during the first bit position to enable the error insertion mask).

Figure 24 - Transmit Ring Control Port



The Transmit Ring Control Port timing diagram (Figure 24) illustrates the operation of the transmit ring control port when the ring control ports are enabled (using the RCP bit in the STXC Control/Enable Register). The control port timing is provided by the TRCPCLK input. TRCPFP and TRCPDAT are sampled on the rising edge of TRCPCLK. TRCPFP is used to distinguish the bit positions carrying maintenance signal control information (TRCPFP is high) from the bit positions carrying line REI indications (TRCPFP is low). TRCPFP is high for 21 bit positions once per frame 125 µs). Currently, only the last two bit positions are used. These bit positions control the insertion of line RDI and line AIS maintenance signals as illustrated in Figure 24. The remaining 19 bit positions are reserved for future STXC feature enhancements.

Figure 25 - Receive Ring Control Port



The Receive Ring Control Port timing diagram (Figure 25) illustrates the operation of the receive ring control port when the ring control ports are enabled (using the RCP bit in the STXC Control/Enable Register). The control port timing is provided by the RRCPCLK input. RRCPFP and RRCPDAT are updated on the falling edge of RRCPCLK. RRCPFP is used to distinguish the bit positions carrying alarm status and maintenance signal control information (RRCPFP is high) from the bit positions carrying line REI indications (RRCPFP is low). RRCPFP is high for 21 bit positions once per 125 µs frame.

The first 16 bit positions contain the APS channel byte values after filtering (the K1 and K2 values have been identical for at least three consecutive frames). The 17th bit position, COAPSI, is high for one frame when a new APS channel byte value (after filtering) is received. The 18th and 19th bit positions contain the current protection switch byte failure alarm status. PSBFI is high for one frame when a change in the protection switch byte failure alarm state is detected. PSBFV contains the real-time active high state value of the protection switch byte failure alarm. The 20th and 21st bit positions control the insertion of the line AIS and line RDI maintenance signals in a mate STXC. The SENDRDI bit position is controlled by the logical OR of the loss of signal, loss of frame and line AIS alarms, or by the SRDI bit in the Ring Control Register. The SENDAIS bit position is controlled by the SAIS bit in the Ring Control Register.

While RRCPFP is low, RRCPDAT is high for one RRCPCLK cycle for each received REI indication.

13 OPERATION

13.1 Bit Error Rate Monitor

The Receive APS, Synchronization Extractor and Bit Error (RASE) block counts and monitors line BIP errors over programmable periods of time (window size). The RASE contains two Bit Error Rate Monitors (BERM), one monitors the signal fail threshold crossing alarm, and the other monitors the signal degrade threshold crossing alarm.

The tables below give calculated values that are appropriate for both the SF BERM and SD BERM. Typically, the SF threshold will be configured for a BER of 10^{-3} or 10^{-4} and the SD threshold will be configured between 10^{-5} and 10^{-9}. For all of the tables below, the saturation threshold should be disabled by setting SMODE=0.

All of the recommended values below meet the various requirements for detection/clearing and (where applicable) false detection/clearing. In the case of the SDH recommendations, the detection (clearing) thresholds were chosen between the minimum and maximum values established by the detection and false detection requirements. In the case of the Sonet recommendations, the detection thresholds were chosen at their maximum value, and the clearing thresholds at their minimum.

The CMODE column corresponds to the values that should be written to the SFCMODE and SDCMODE bits in the RASE Configuration/Control register. The Accumulation Period column represents the values that should be written to the RASE SF Accumulation Registers and the RASE SD Accumulation Period Registers. . The Detection Threshold column represents the values that should be written to the RASE SF Detection Threshold Registers and the RASE SD Detection Threshold Registers. The Clearing Threshold column represents the values that should be written to the RASE SF Clearing Threshold Registers and the RASE SD Clearing Threshold Period Registers.

Table 5 - RASE-BERM Configuration for SDH STM-0

BER	Evaluation Period (s)	CMODE (SFCMODE/ SDCMODE)	Accumulation Period (SFSAP/SDSAP)	Detection Threshold (SFDTH/SDDTH)	Clearing Threshold (SFCTH/SDCTH)
1.0E-03	0.01	0	00000A	0D7	04A
1.0E-04	0.1	0	000064	0D7	04A
1.0E-05	1	0	0003E8	0D7	04A
1.0E-06	10	0	002710	0D7	04A
1.0E-07	100	0	0186A0	0D7	04A
1.0E-08	1000	0	0F4240	0D7	04A
1.0E-09	10000	0	989680	0D7	04A

Table 6 - RASE-BERM Configuration for SDH STM-1

BER	Evaluation Period (s)	CMODE (SFCMODE/ SDCMODE)	Accumulation Period (SFSAP/SDSAP)	Detection Threshold (SFDTH/SDDTH)	Clearing Threshold (SFCTH/SDCTH)
1.0E-03	0.01	0	00000A	2A2	0CA
1.0E-04	0.1	0	000064	2A2	0CA
1.0E-05	1	0	0003E8	2A2	0CA
1.0E-06	10	0	002710	2A2	0CA
1.0E-07	100	0	0186A0	2A2	0CA
1.0E-08	1000	0	0F4240	2A2	0CA
1.0E-09	10000	0	989680	2A2	0CA

Table 7 - RASE-BERM Configuration for Sonet STS-1

BER	Evaluation Period (s)	CMODE (SFCMODE/ SDCMODE)	Accumulation Period (SFSAP/SDSAP)	Detection Threshold (SFDTH/SDDTH)	Clearing Threshold (SFCTH/SDCTH)
1.0E-03	0.01*	1	00000A	0D9	1B5
1.0E-04	0.04	1	000028	0A7	0B8
1.0E-05	0.3	1	00012C	084	08E
1.0E-06	3	1	000BB8	084	08E
1.0E-07	30	1	007530	084	08E
1.0E-08	250	1	03D090	06D	078
1.0E-09	2000	1	1E8480	055	061

*Detection time objectives and false detection objectives cannot be met simultaneously for STS-1 with a 10^{-3} bit error rate. The given values meet the detection time requirements with a 0.999 probability, and also meet the false detection objectives.

Table 8 - RASE-BERM Configuration for Sonet STS-3

BER	Evaluation Period (s)	CMODE (SFCMODE/ SDCMODE)	Accumulation Period (SFSAP/SDSAP)	Detection Threshold (SFDTH/SDDTH)	Clearing Threshold (SFCTH/SDCTH)
1.0E-03	0.008	1	000008	245	3BE
1.0E-04	0.013	1	00000D	0A3	0B4
1.0E-05	0.1	1	000064	084	08E
1.0E-06	1	1	0003E8	084	08E
1.0E-07	10	1	002710	084	08E
1.0E-08	83	1	014438	06D	077
1.0E-09	667	1	0A2D78	055	061

14 ABSOLUTE MAXIMUM RATINGS

Table 9 - STXC Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±500 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

15 D.C. CHARACTERISTICS

(T_A = -40°C to +85°C)

Table 10 - STXC D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	4.75	5	5.25	Volts	Applies to VDDI[2:0], VDDO[7:0], TAVD1, TAVD2 and TAVD3.
A_{VD}	Power Supply	4.75	5	5.25	Volts	
V_{TAVD4}	Tx Analog Reference Supply Voltage	4.75		5.25	Volts	$\|V_{PIH}-V_{PIL}\|$=600 mV, PECL inputs AC coupled.
V_{RAVD}	Rx Analog Reference Supply Voltage	4.75		5.25	Volts	$\|V_{PIH}-V_{PIL}\|$=600 mV, PECL inputs AC coupled.
V_{IL}	Input Low Voltage (TTL Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{PSWG}	Input Voltage Swing (PECL Only)	550		1000	mV	TXCI+/-, RXD+/- and RXC+/- A.C. coupled
V_{OL}	Output or Bidirectional Low Voltage (TTL Only)		0.1	0.4	Volts	
V_{POL}	Output Low Voltage (PECL Only)		V_{TERM} -0.6		Volts	Note 6
Symbol	Parameter	Min	Typ	Max	Units	Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output or Bidirectional High Voltage (TTL Only)	VDD - 0.5			Volts	
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
I_{ILPU}	Input Low Current	+20	+83	+200	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 1, 3
I_{ILPD}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 4, 3
I_{IHPD}	Input High Current	-200	-83	-20	µA	$V_{IH} = V_{DD}$, Notes 4, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF for MQFP
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF for MQFP

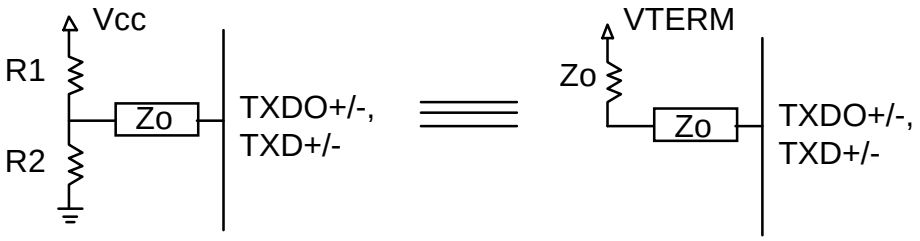
Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF for MQFP
I_{TAVD4}	Tx Reference Supply current		2.5		mA	
I_{RAVD}	Rx Reference Supply current		3.5		mA	
Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{VT2}	Tx Drive Level Reference input current		3.5		mA	
$I_{TAVD1,2,3}$	Total PECL Driver Supply current		44		mA	
I_{DDOP1}	Operating Current STS-3 Bit Serial Mode Enabled		130	190	mA	V_{DD} = 5.25 V, Outputs Unloaded, RXC+/- = 155.52 MHz, TXCI+/- = 155.52 MHz, Random Data
I_{DDOP2}	Operating Current STS-3 Byte Serial Mode Enabled		31	60	mA	V_{DD} = 5.25 V, Outputs Unloaded, RICLK, TICLK = 19.44 MHz, Random Data, AVD = 0 V.
I_{DDOP3}	Operating Current STS-1 Bit Serial Mode Enabled (PECL Outputs)		150	170	mA	V_{DD} = 5.25 V, Outputs Unloaded, RSICLK, TSICLK = 51.84 MHz, Random Data

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DDOP4}	Operating Current STS-1 Byte Serial Mode Enabled		26	40	mA	V_{DD} = 5.25 V, Outputs Unloaded, RICLK, TICLK = 6.48 MHz, Random Data, AVD = 0 V.

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bidirectional pin with internal pull-down resistor.
5. Typical values are given as a design aid. The product is not tested to these values.
6. The PECL output low voltage is specified relative to the termination voltage (VTERM) as illustrated below:

Figure 26 - PECL Output Low Voltage



$$R1 // R2 = Zo$$

$$VTERM = \frac{R2}{(R1 + R2)} * Vcc$$

This specification is applicable when the STXC is operated as illustrated in the Interface Examples section (a 50Ω controlled impedance environment with R1 = 59 Ω and R2 = 312 Ω).

16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±5%)

Table 11 - Microprocessor Interface Read Access (Figure 27, Figure 28)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	20		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	20		ns
tS_{RWB}	RWB to Read Set-up	25		ns
tH_{RWB}	RWB to Read Hold	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 27 - Microprocessor Interface Read Access Timing (Intel Mode)

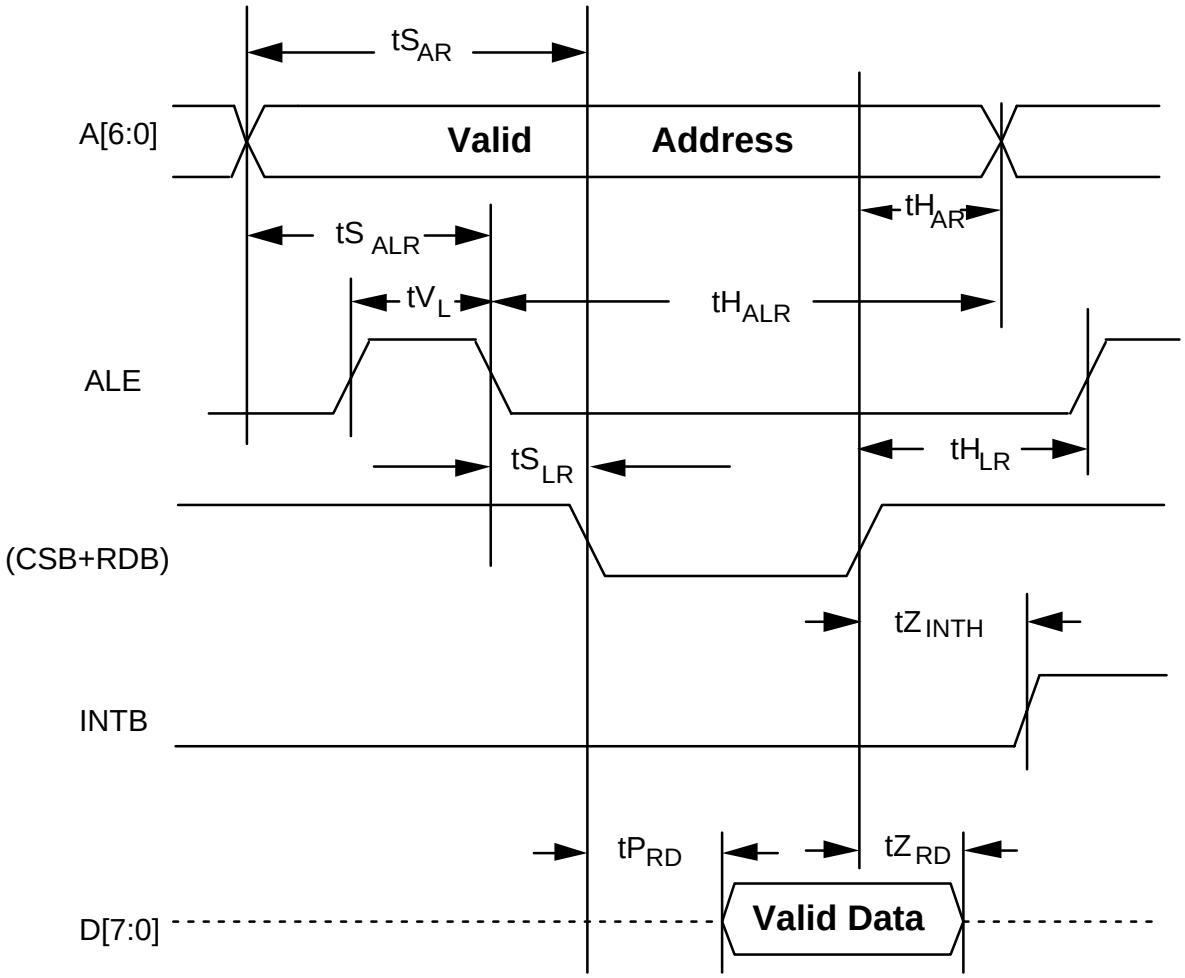
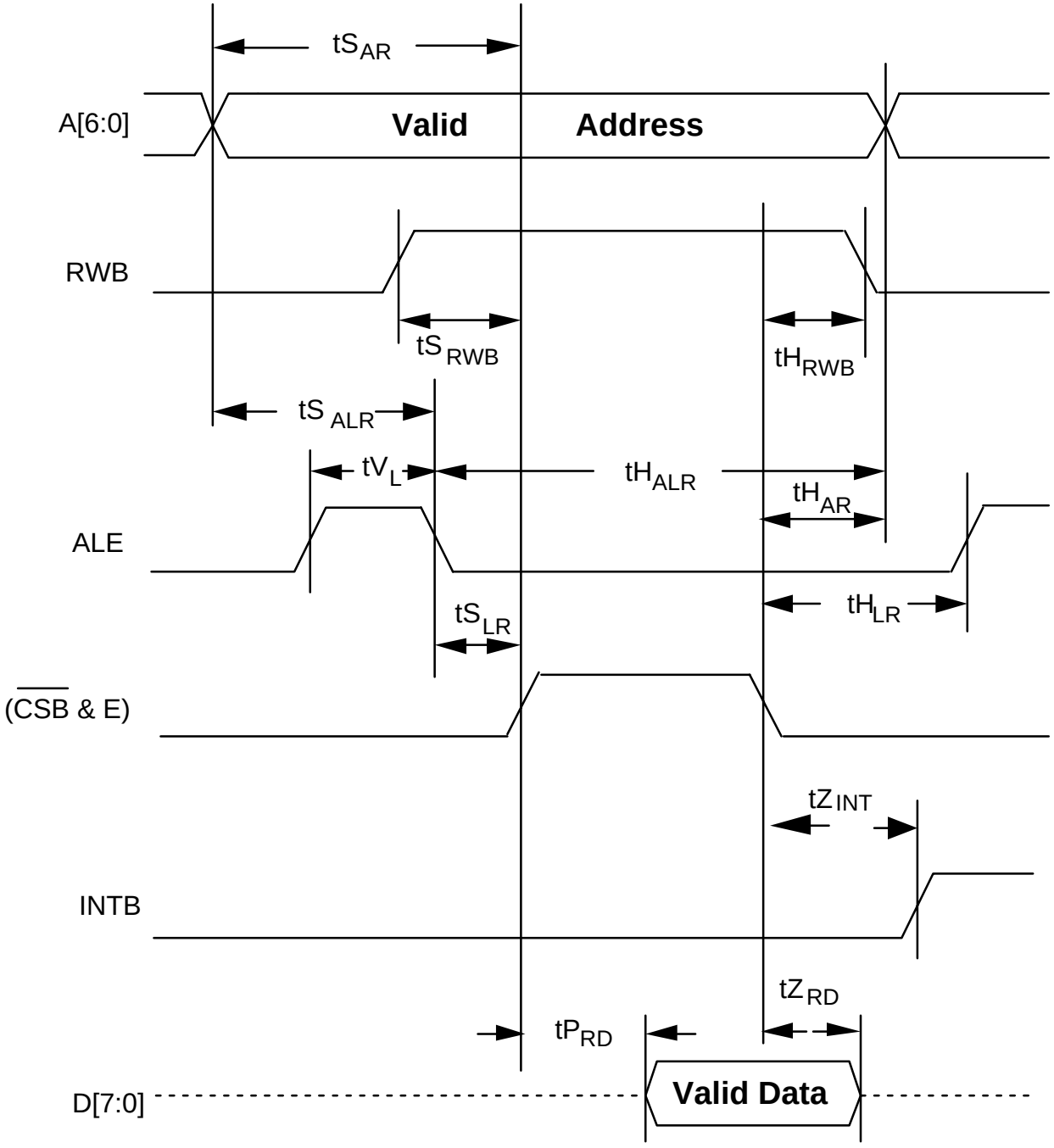


Figure 28 - Microprocessor Interface Read Access Timing (Motorola Mode)



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

   a. In Intel mode, a valid read cycle is defined as a logical OR of the CSB and the RDB signals.

   b. In Motorola mode, a valid read cycle is defined as a logical AND of the E signal, the RWB signal and the inverted CSB signal.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameter tH_{AR} and tS_{AR} are not applicable if address latching is used.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 12 - Microprocessor Interface Write Access (Figure 29, Figure 30)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	20		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	20		ns
tS_{RWB}	RWB to Write Set-up	25		ns
tH_{RWB}	RWB to Write Hold	20		ns
tH_{DW}	Data to Valid Write Hold Time	20		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 29 - Microprocessor Interface Write Access Timing (Intel Mode)

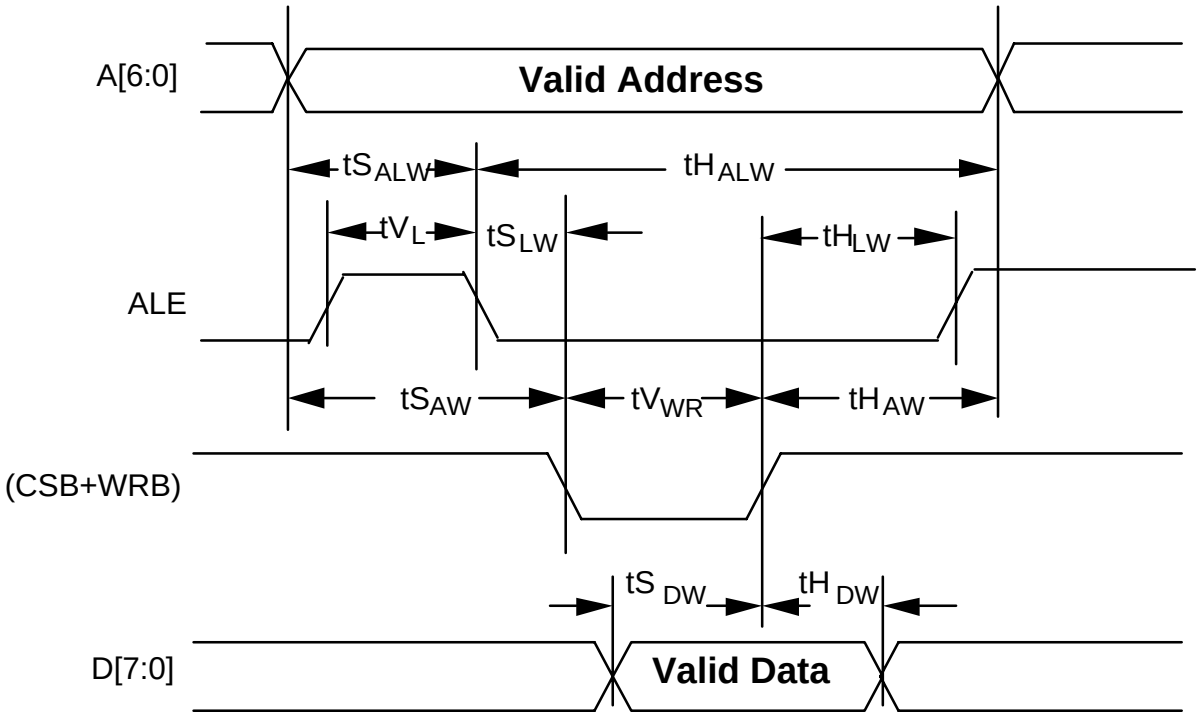
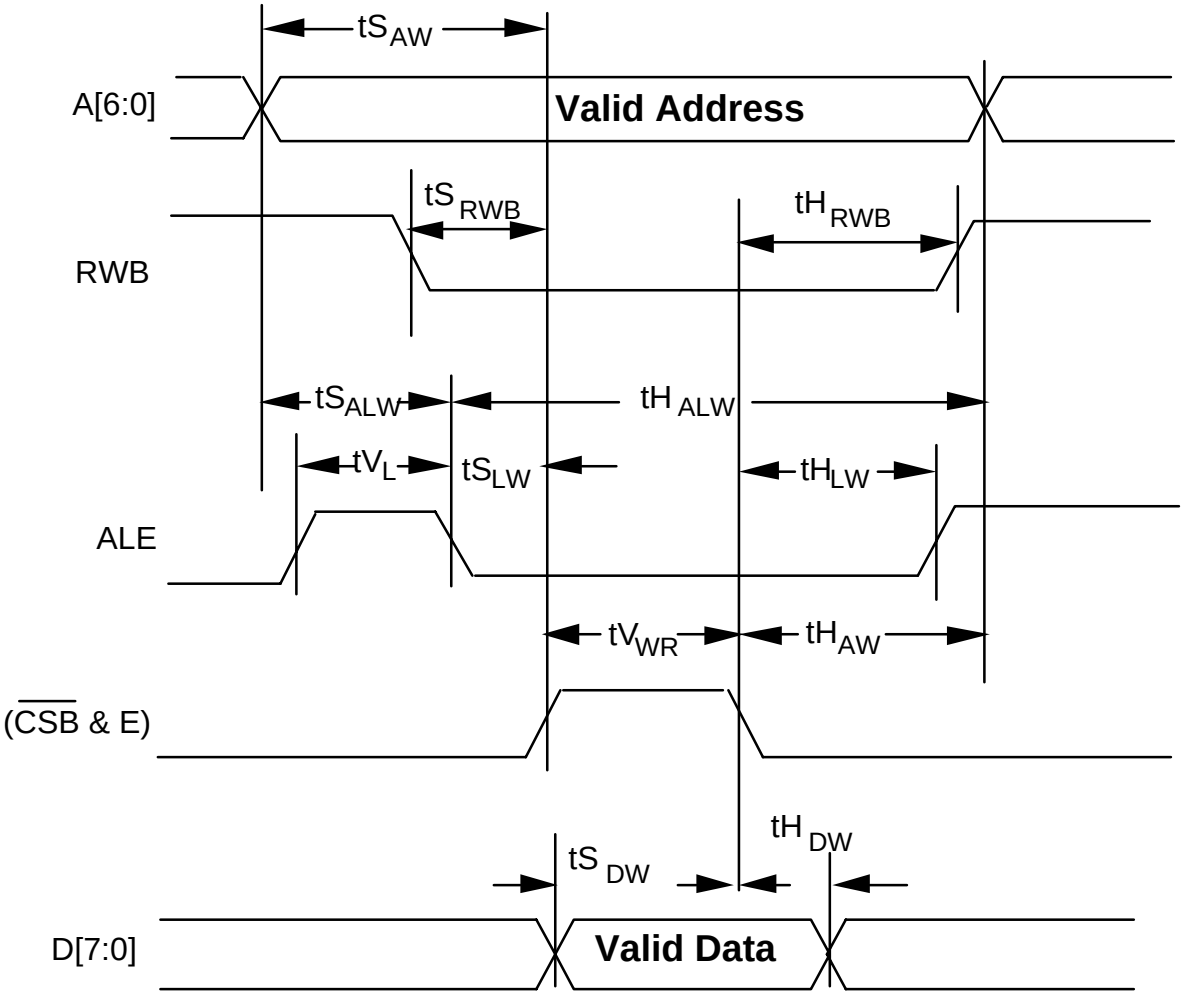


Figure 30 - Microprocessor Interface Write Access Timing (Motorola Mode)



Notes on Microprocessor Interface Write Timing:

1. In Intel mode, a valid write cycle is defined as a logical OR of the CSB and the WRB signals.

   a. In Motorola mode, a valid write cycle is defined as a logical AND of the E signal, the inverted RWB signal and the inverted CSB signal.

2. Microprocessor timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

17 STXC TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±5%)

17.1 INPUT TIMING

Table 13 - Receive Input (Figure 31)

Symbol	Description	Min	Max	Units
	RICLK Frequency (nominally 6.48 MHz, 19.44 MHz)		20	MHz
	RICLK Duty Cycle	33	67	%
tS_{RIN}	RIN[7:0] Set-up Time to RICLK	2		ns
tH_{RIN}	RIN[7:0] Hold Time to RICLK	3		ns
tS_{RLAIS}	RLAIS Set-up Time to RICLK	2		ns
tH_{RLAIS}	RLAIS Hold Time to RICLK	3		ns
tS_{RIFP}	RIFP Set-Up Time to RICLK	2		ns
tH_{RIFP}	RIFP Hold Time to RICLK	3		ns

Figure 31 - Receive Input Timing

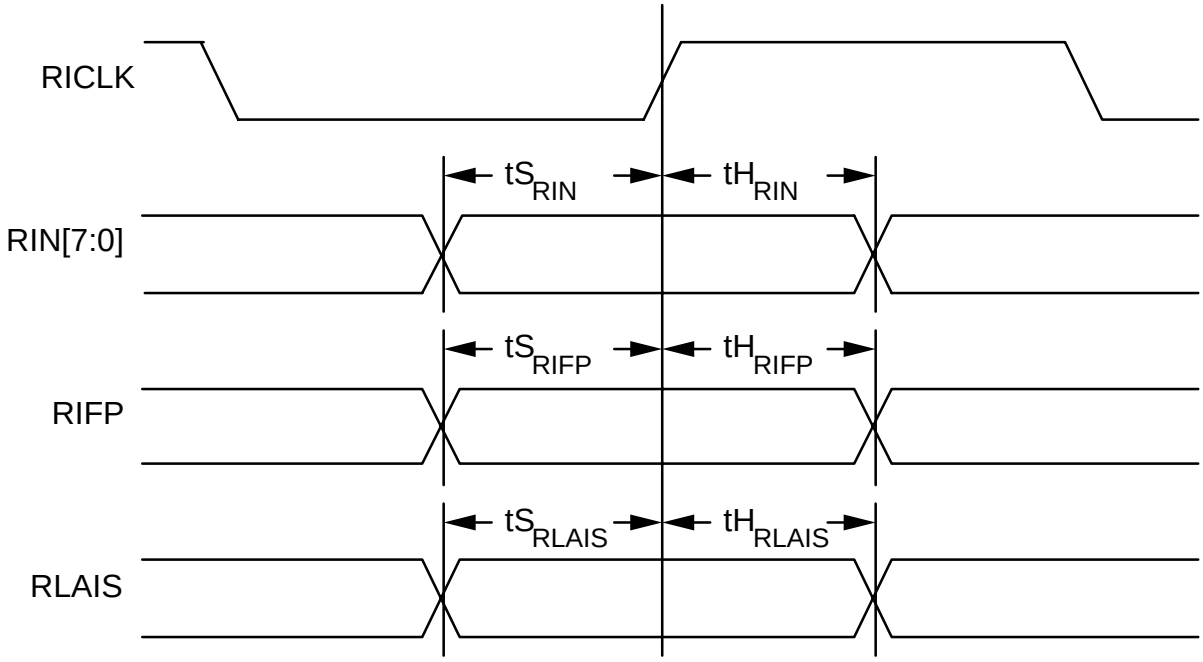


Table 14 - Transmit Input (Figure 32)

Symbol	Description	Min	Max	Units
	TICLK Frequency (nominally 6.48 MHz 19.44 MHz MHz)		20	MHz
	TICLK Duty Cycle	33	67	%
tS_{TIN}	TIN[7:0] Set-up Time to TICLK	2		ns
tH_{TIN}	TIN[7:0] Hold Time to TICLK	3		ns
tS_{TDP}	TDP, TPLSet-up Time to TICLK	10		ns
tH_{TDP}	TDP, TPL Hold Time to TICLK	5		ns
tS_{TFPIN}	TIFP Set-Up Time to TICLK	2		ns
tH_{TFPIN}	TIFP Hold Time to TICLK	3		ns
tS_{TDIS}	TDIS Set-up Time to TICLK	2		ns
tH_{TDIS}	TDIS Hold Time to TICLK	3		ns
tS_{TRDI}	TRDI Set-up Time to TICLK	10		ns

Symbol	Description	Min	Max	Units
tH_{TRDI}	TRDI Hold Time to TICLK	5		ns
tS_{TLAIS}	TLAIS Set-up Time to TICLK	10		ns
tH_{TLAIS}	TLAIS Hold Time to TICLK	5		ns
tS_{TLD}	TLD Set-up Time to TLDCLK	30		ns
tH_{TLD}	TLD Hold Time to TLDCLK	0		ns
tS_{TSD}	TSD Set-up Time to TSDCLK	30		ns
tH_{TSD}	TSD Hold Time to TSDCLK	0		ns
tS_{TOW}	TSOW, TLOW, TSUC Set-up Time to TOWCLK	30		ns
tH_{TOW}	TSOW, TLOW, TSUC Hold Time to TOWCLK	0		ns
tS_{TAPS}	TAPS Set-up Time to TAPSCLK	30		ns
tH_{TAPS}	TAPS Hold Time to TAPSCLK	0		ns
tS_{TTOH}	TTOHCLK Set-up Time to TTOH, TTOHEN	30		ns
tH_{TTOH}	TTOHCLK Hold Time to TTOH, TTOHEN	0		ns

Figure 32 - Transmit Input

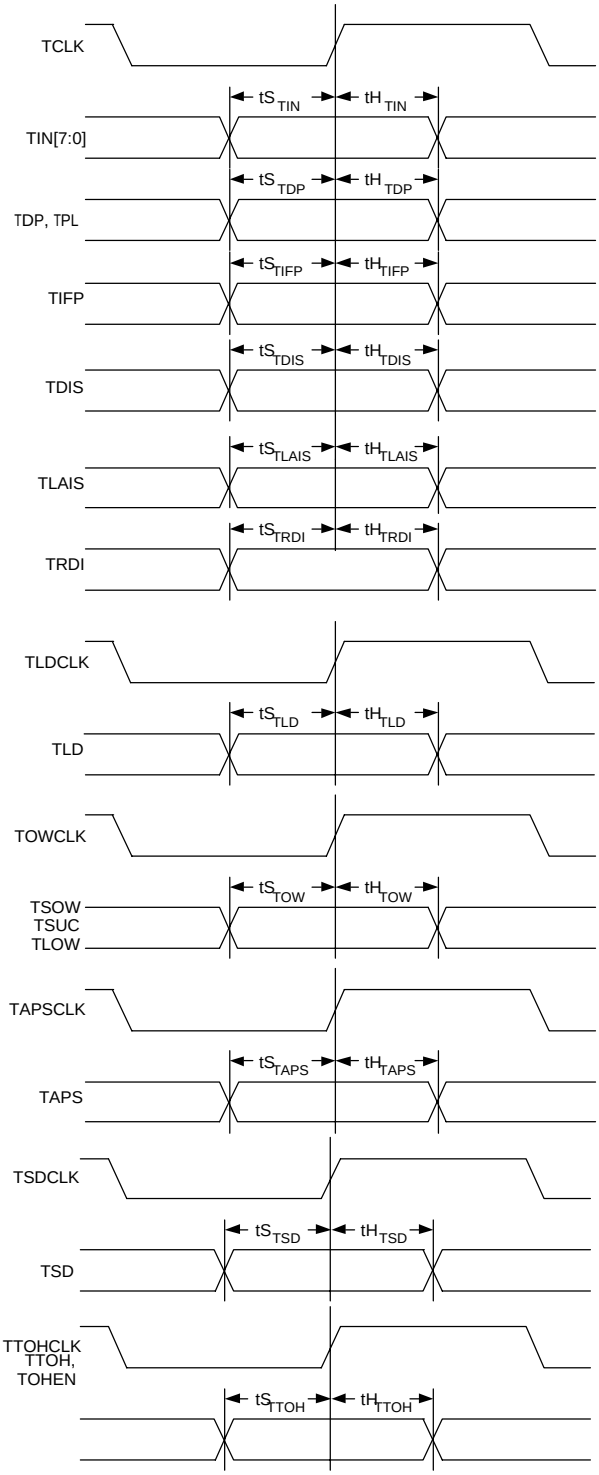


Table 15 - STS-3 Bit Serial Input (Figure 33)

Symbol	Description	Min	Max	Units
	RXC+/- Frequency (nominally 155.52 MHz)		156	MHz
	RXC+/- Duty Cycle	40	60	%
	TXCI+/- Frequency (nominally 155.52 MHz)		156	MHz
	TXCI+/- Duty Cycle	40	60	%
tS_{RXD}	RXD+/- Set-up Time to RXC+/-	2		ns
tH_{RXD}	RXD+/- Hold Time to RXC+/-	1		ns

Figure 33 - STS-3 Bit Serial Input

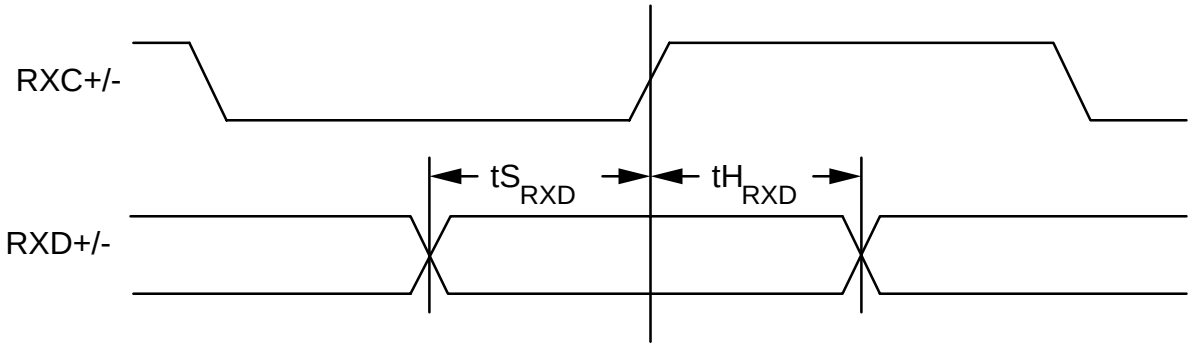


Table 16 - STS-1 Input (Figure 34)

Symbol	Description	Min	Max	Units
	RSICLK Frequency (nominally 51.84 MHz)		52	MHz
	RSICLK Duty Cycle	33	67	%
	TSICLK Frequency (nominally 51.84 MHz)		52	MHz
	TSICLK Duty Cycle	33	67	%
tS_{RSIN}	RSIN Set-up Time to RSICLK	3		ns
tH_{RSIN}	RSIN Hold Time to RSICLK	2		ns

Figure 34 - STS-1 Input

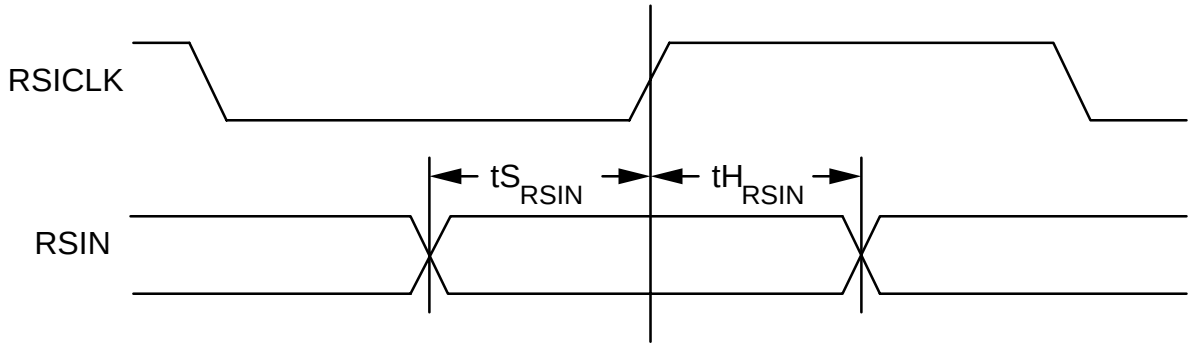
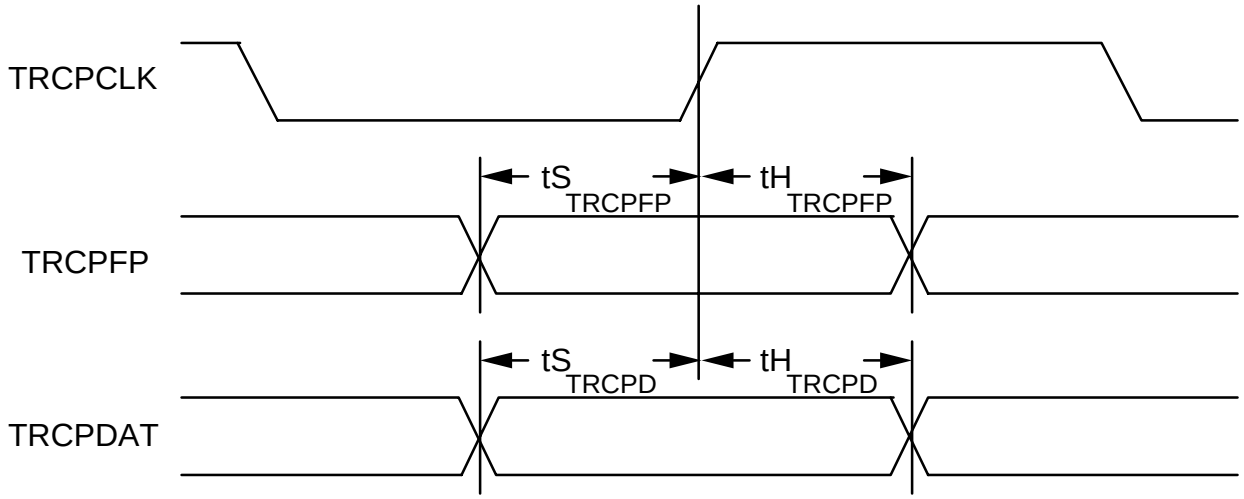


Table 17 - Transmit Ring Control Port Input (Figure 35)

Symbol	Description	Min	Max	Units
	TRCPCLK Frequency (nominally 3.24 MHz)		4	MHz
	TRCPCLK Duty Cycle	33	67	%
tS_{TRCPFP}	TRCPFP Set-up Time to TRCPCLK	10		ns
tH_{TRCPFP}	TRCPFP Hold Time to TRCPCLK	10		ns
tS_{TRCPD}	TRCPDAT Set-up Time to TRCPCLK	10		ns
tH_{TRCPD}	TRCPDAT Hold Time to TRCPCLK	10		ns

Figure 35 - Transmit Ring Control Port Input



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. When a set-up time is specified between a PECL input and a clock, the set-up time is the time in nanoseconds from the crossing point of the input to the crossing point of the clock.

4. When a hold time is specified between a PECL input and a clock, the hold time is the time in nanoseconds from the crossing point of the input to the crossing point of the clock.

17.2 OUTPUT TIMING

Table 18 - Receive Output Timing (Figure 36)

Symbol	Description	Min	Max	Units
tP_{ROUT}	RICLK High to ROUT[7:0] Valid Prop Delay	4	25	ns
tP_{RDP}	RICLK High to RDP Valid Prop Delay	4	35	ns
tP_{ROFP}	RICLK High to ROFP Valid Prop Delay	4	25	ns
tP_{RALM}	RICLK High to OOF, LOF, LOS, LAIS, RDI Valid Prop Delay	4	30	ns
tP_{RLD}	RLDCLK Low to RLD Valid Prop Delay	-15	20	ns
tP_{RSD}	RSDCLK Low to RSD Valid Prop Delay	-15	20	ns
tP_{ROW}	ROWCLK Low to RSOW, RSUC, RLOW Valid Prop Delay	-250	+250	ns
tP_{RAPS}	RAPSCLK Low to RAPS Valid Prop Delay	-15	20	ns
tP_{RTOH}	RTOHCLK Low to RTOH and RTOHFP Valid Prop Delay	-15	20	ns

Figure 36 - Receive Output Timing

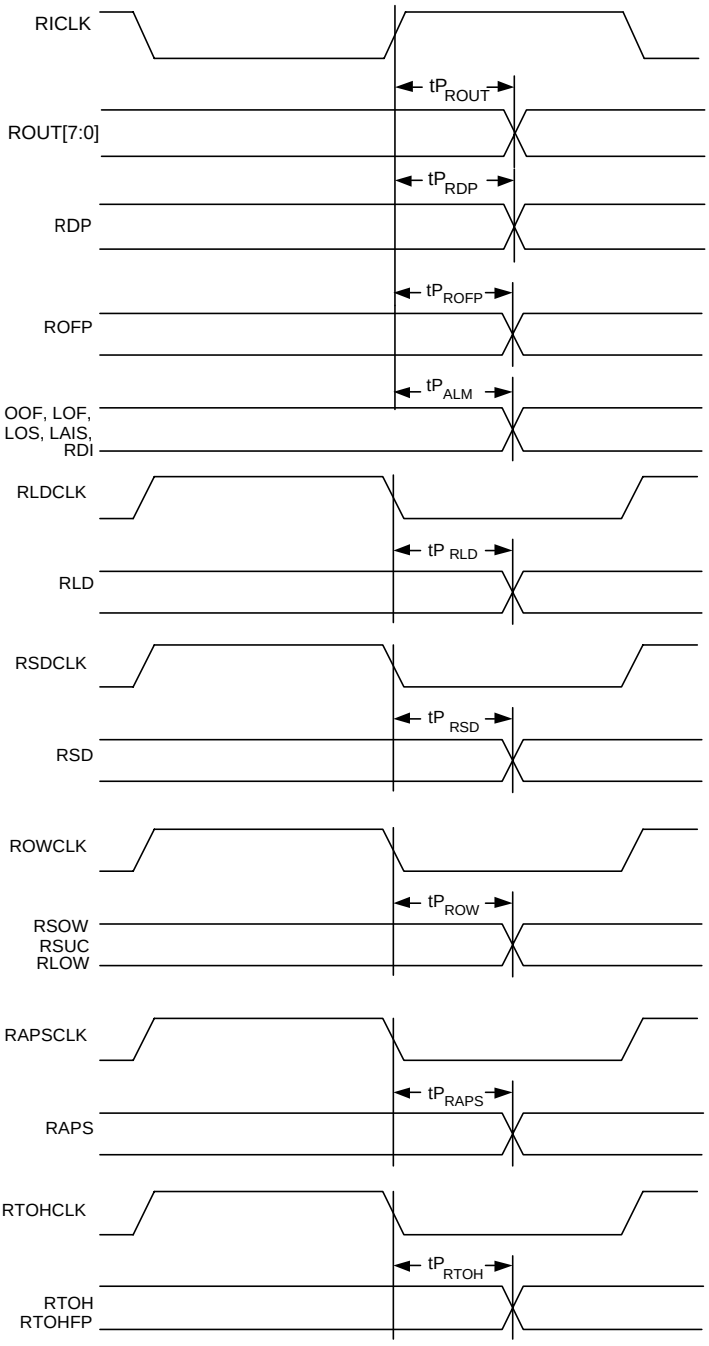


Table 19 - Transmit Output Timing (Figure 37)

Symbol	Description	Min	Max	Units
tPTOUT	TICLK High to TOUT[7:0] Valid Prop Delay	2	20	ns
tPTOFP	TICLK High to TOFP Valid Prop Delay	2	20	ns
tPTTOHFP	TTOHCLK Low to TTOHFP Valid Prop Delay	-20	20	ns

Figure 37 - Transmit Output Timing

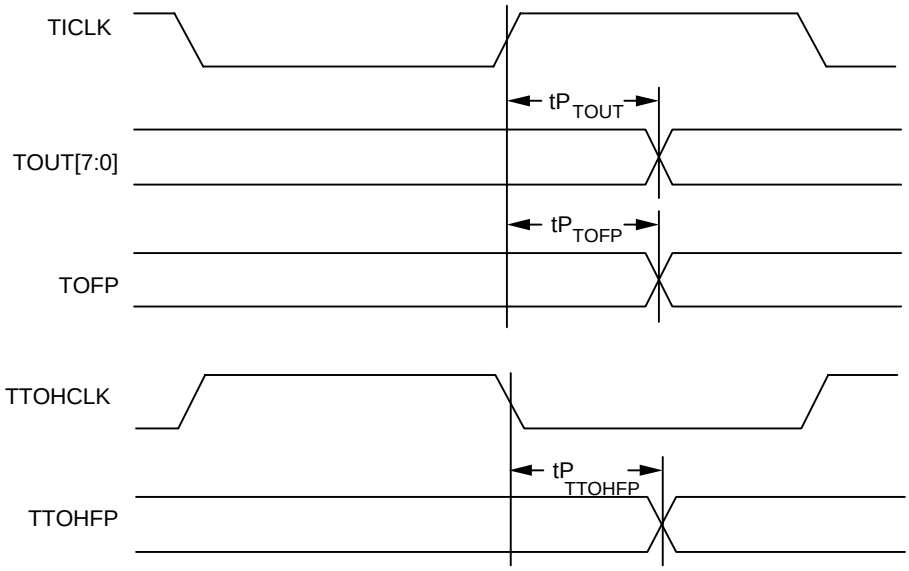


Table 20 - STS-3 Bit Serial Output (Figure 38)

Symbol	Description	Min	Max	Units
tP_{TXD}	TXCO+/- Low to TXD+/- Valid Prop Delay	-1	1	ns
tP_{TXCO}	TXCI+/- High to TXCO+/- Valid Prop Delay	2	20	ns

Figure 38 - STS-3 Bit Serial Output Timing

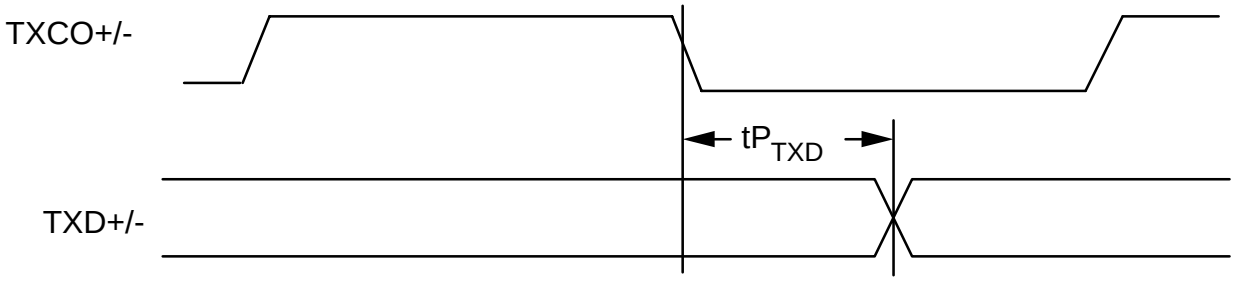


Table 21 - STS-1 Output (Figure 39)

Symbol	Description	Min	Max	Units
tPTSOUT	TSICLK High to TSOUT Valid Prop Delay *	2	15	ns

* Into a 30pF Load.

Figure 39 - STS-1 Output Timing

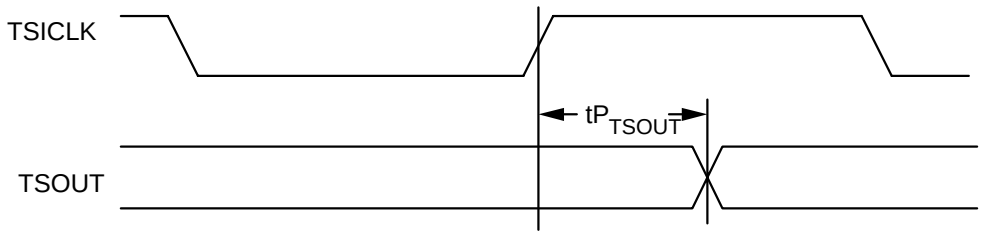
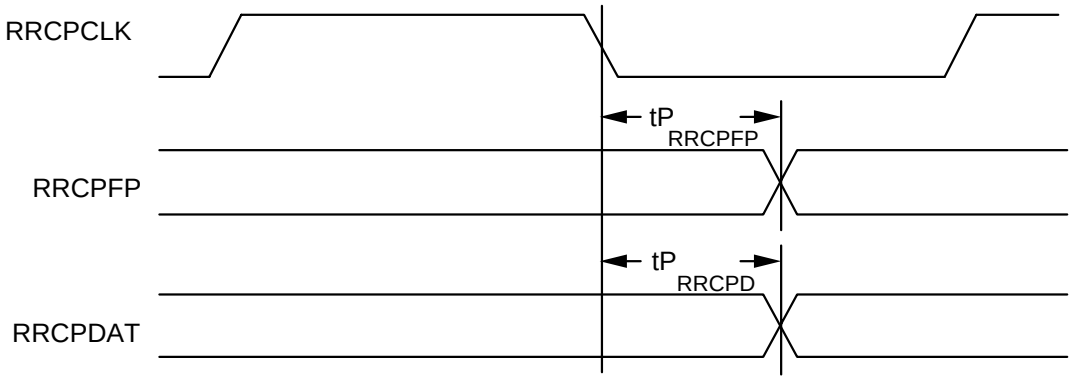


Table 22 - Receive Ring Control Port Output (Figure 40)

Symbol	Description	Min	Max	Units
tP_{RRCPFP}	RRCPCLK High to RRCPFP Valid Prop Delay	-15	20	ns
tP_{RRCPD}	RRCPCLK High to RRCPDAT Valid Prop Delay	-15	20	ns

Figure 40 - Ring Control Port Output



Notes on Output Timing:

1. TTL output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. PECL output propagation delay time is the time in nanoseconds from the crossing point of the reference signal to the crossing point of the output.

3. Maximum and minimum TTL output propagation delays are measured with a 50 pF load on the outputs, with the exception of **tpROUT**, **tpTOUT**, and **tpTSOUT**, which are measured with a 30 pF load on the outputs.

4. Maximum and minimum PECL output propagation delays are measured with the PECL outputs terminated into a 50Ω equivalent load.

18 ORDERING AND THERMAL INFORMATION

Table 23 - STXC Ordering Information

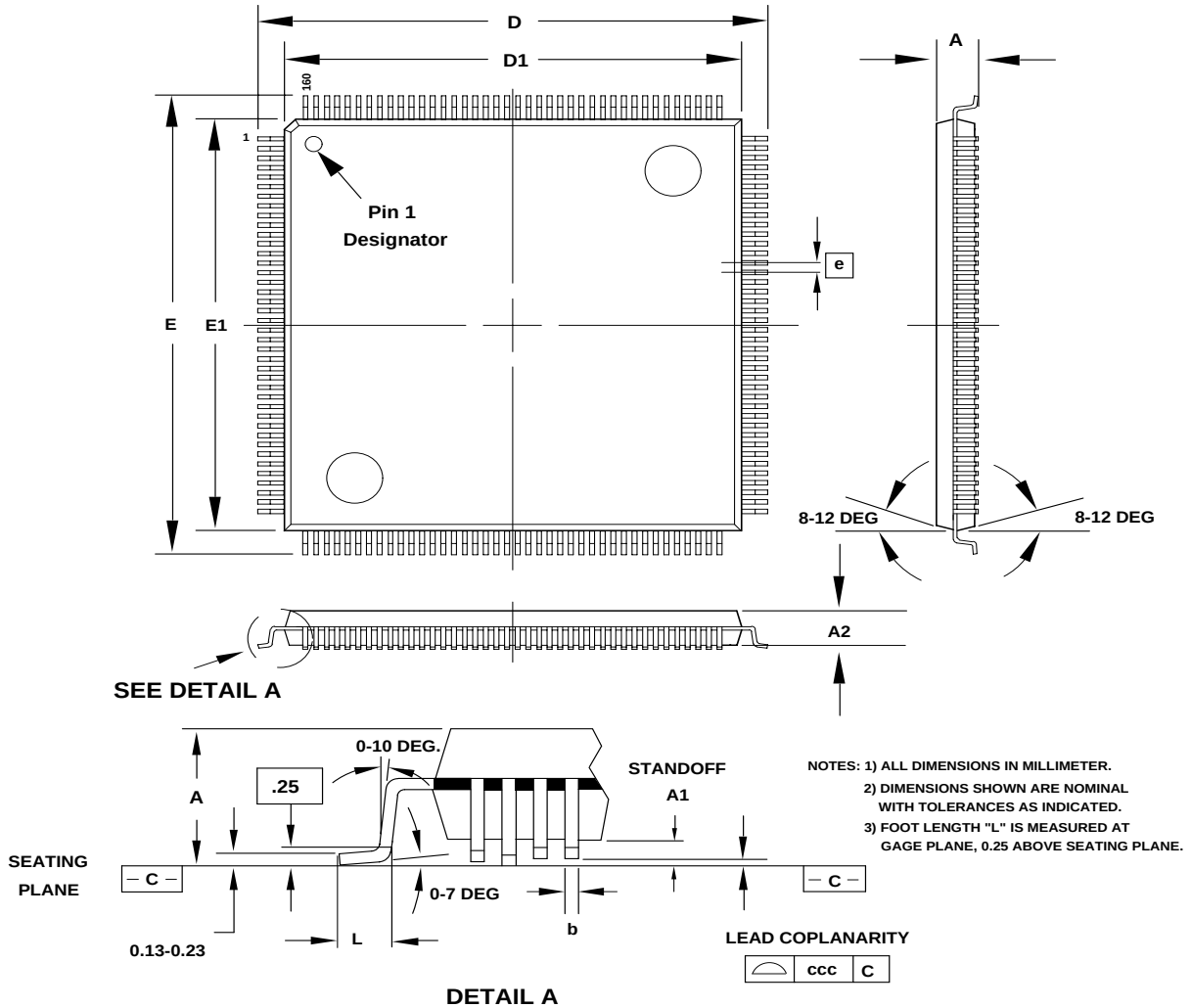
PART NO.	DESCRIPTION
PM5343-RI	160 Copper Leadframe Metric Quad Flat Pack (MQFP)

Table 24 - STXC Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5343-RI	-40°C to 85°C	45 °C/W	15 °C/W

19 MECHANICAL INFORMATION

Figure 41 - 160 Pin Copper Leadframe Metric Quad Flat Pack (R Suffix):



PACKAGE TYPE: 160 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.42	0.25	3.17	30.95	27.85	30.95	27.85	0.73		0.22	
Nom.			3.42	31.20	28.00	31.20	28.00	0.88	0.65		
Max.	4.07	0.39	3.68	31.45	28.10	31.45	28.10	1.03		0.38	0.10

NOTES

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