STEL-2050A

Data Sheet

STEL-2050A

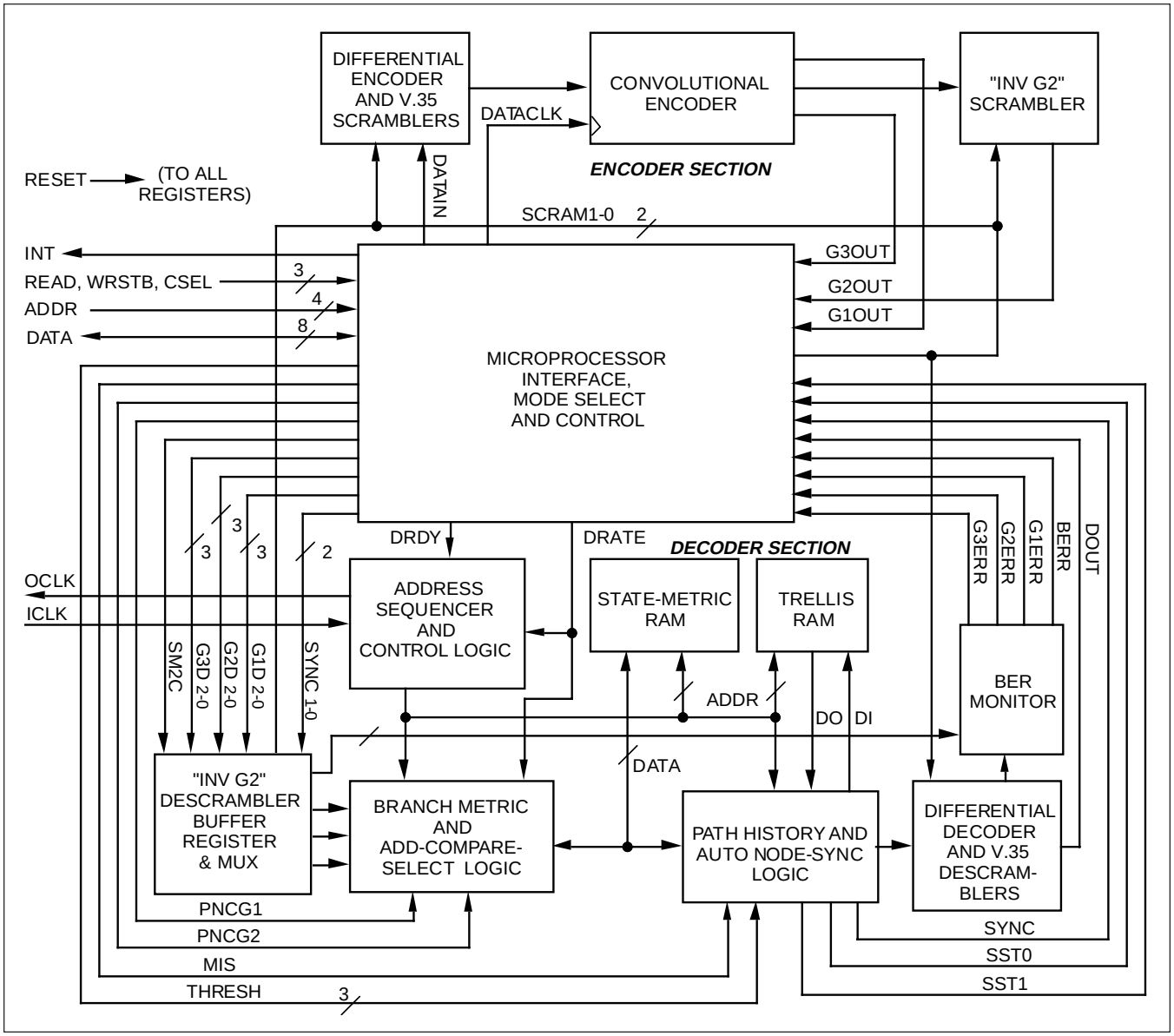
Convolutional Encoder
Viterbi Decoder

intel

FEATURES

- **Constraint Length 7**
- **Rates $^1/_3$, $^1/_2$, $^2/_3$* and $^3/_4$* (*Punctured)**
- **Built in BER Monitor**
- **Programmable Scrambler: V.35 (CCITT or IESS) or "Invert G2"**
- **Differential Encoder and Decoder**
- **Three Bit Soft Decision Inputs in Signed Magnitude or 2's Complement Formats**
- **Up to 256 Kbps Data Rate (–40° to 85° C)**
- **0.6 Micron CMOS Technology**
- **Coding Gain of 5.2 dB (@ 10^{-5} BER, Rate $^1/_2$)**
- **Industry Standard Polynomials G1=171_8, G2=133_8, G3=145_8,**
- **All control and data I/O via Microprocessor Interface**
- **Low Power Consumption**
- **28-pin PLCC and CLDCC Packages**
- **Commercial and Military Temperature Ranges Available**

BLOCK DIAGRAM



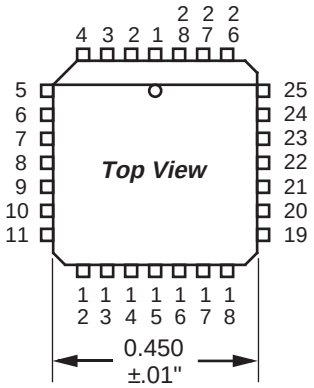
FUNCTIONAL DESCRIPTION

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STEL-2050A is a specialized product designed to perform this specific communications related function.

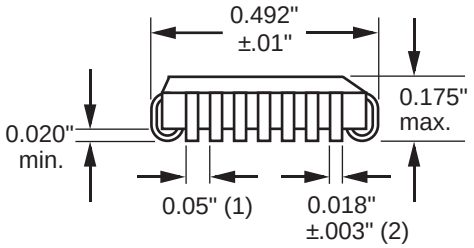
The encoder creates a stream of symbols which are transmitted at 2 (rate $^1/_2$) or 3 (rate $^1/_3$) times the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of information despite a high symbol error rate resulting from a noisy link. The coding overhead can be reduced at the expense of the coding gain by puncturing (deleting) some of the symbols. The STEL-2050A is designed to operate in this way at rates $^2/_3$ and $^3/_4$, when 3 symbols are transmitted for every 2 bits encoded (rate $^2/_3$) or 4 symbols are transmitted for every 3 bits encoded (rate $^3/_4$). The resulting bandwidth overhead is just 50% and 33% respectively, compared with 100% at rate $^1/_2$.

The STEL-2050A incorporates all the memories required to perform these functions. In addition, the STEL-2050A incorporates a differential encoder and decoder, three different scrambling algorithms, a BER monitor and a microprocessor interface. The STEL-2050A is available in a 28-pin PLCC (plastic leaded chip carrier) and also in a ceramic leaded chip carrier (J-bend leads).

PIN CONFIGURATION



Package: 28 pin PLCC (J-bend)
Thermal coefficient, $\theta_{ja} = 45°/W$



Notes: 1 Tolerance not cumulative
2 Dimension at seating plane

PIN CONNECTIONS

1	V_{SS}	8	V_{SS}	15	V_{SS}	22	V_{SS}
2	READ	9	OCLK	16	$DATA_7$	23	$DATA_2$
3	CSEL	10	V_{DD}	17	$DATA_6$	24	$DATA_1$
4	V_{DD}	11	$ADDR_3$	18	V_{DD}	25	$DATA_0$
5	RESET	12	$ADDR_2$	19	$DATA_5$	26	INT
6	V_{SS}	13	$ADDR_1$	20	$DATA_4$	27	I.C.
7	ICLK	14	$ADDR_0$	21	$DATA_3$	28	WRSTB

Notes: 1. I.C. denotes Internal Connection. ThIs pin must be left unconnected. Do not use for a via.
2. Connect all unused inputs to V_{SS}, leave unused outputs unconnected.

FUNCTION BLOCK DESCRIPTION

The convolutional coder is functionally independent of the decoder. Writing a new data bit into address 4_H automatically clocks the data down the 7-bit shift register. The symbols G1, G2, and G3 are generated from the modulo-2 sum (exclusive-OR) of the inputs to the 3 generators from the taps on the shift register. The 3 polynomials are 171_8 (G1), 133_8 (G2), and 145_8 (G3). The three symbols generated for each input data bit are written into the read mode register at address 5_H.

At the decoder symbols are written into addresses 0_H and (for rate $^1/_3$ operation only) 1_H. The **DRATE** bit in address 2_H determines whether the decoder operates in rate $^1/_2$ or rate $^1/_3$ mode. When operating at rate $^1/_2$ the decoding process starts automatically as soon as data is written into address 0_H and the G3 data is ignored by the decoder. When operating at rate $^1/_3$ the G1 and G2 symbols must be written first, since the decoding process starts automatically as soon as data is written into address 1_H. At least 70 cycles of **ICLK** must elapse between each write operation to address 0_H. (rate $^1/_2$) or 1_H (rate $^1/_3$) to allow the decoder to process each data bit.

For hard decision binary symbols the symbol should be written into bits **G1D2**, **G2D2** and **G3D2** respectively, and the other symbol bits set high. Three-bit soft decision symbols may be input in Signed Magnitude or Two's Complement code, according to the setting of the code control bit, **SM2C**, in address 2_H. The bit should be set high when using hard decision data.

A single decoded data bit, **DOUT**, is written into address 3_H (read mode) for every set of input symbols. The data bit corresponding to a particular symbol set will be output after a delay of 71 symbol sets. Therefore, when using the STEL-2050A to decode blocks of data 71 additional dummy zero symbols (G1 and G2 for rate $^1/_3$ or G3 for rate $^1/_3$) must be written into address 0_H or 1_H to flush the last 71 decoded data bits out of the decoder.

Node synchronization (correctly grouping incoming symbols into G1, G2, and G3 sets) is inherent with many communication techniques such as TDMA and spread spectrum systems. If node synchronization is not an inherent property of the communications link then the internal auto node sync circuit can be used to do this. This is accomplished by internally connecting the node sync outputs (**SST0** and **SST1**) to the node sync inputs (**SYNC0** and **SYNC1**) by setting the **AUTONS** bit in address 3_H high. The threshold for determining the out of sync condition is user selectable by means of the $\mathbf{THRESH_{2\text{-}0}}$ bits in address 2_H.

A Bit Error Rate Monitor function is provided by re-encoding the decoded data bits and comparing the result with a delayed version of the input symbols. The error information is available in two ways. First, each time an error occurs the error bits in address 3_H (read mode) are set high according to which symbol is found to be in error, and second a running count of the errors in a block of data is generated. The length of the block is determined by the 24-bit word $\mathbf{BPER_{23\text{-}0}}$ stored in addresses 6_H-8_H multiplied by 1000, i.e.

Block length = 1000 x $\mathbf{BPER_{23\text{-}0}}$

The number of errors in this period is divided by 8 and accumulated. If the accumulator overflows during this period its output will be caused to saturate at a value of $FFFF_H$. At the end of the period the error divider (÷8) and the error and period accumulators are cleared and the error count is stored in addresses 7_H and 8_H (read mode) so that the actual Bit Error Rate over this period is:

$$BER = \frac{8 \times \mathbf{BERCT_{15\text{-}0}}}{1000 \times \mathbf{BPER_{23\text{-}0}}}$$

Note that the BER monitor will indicate an error each time an input symbol is punctured, so that the BER indicated by the $\mathbf{BERCT_{15\text{-}0}}$ output will not be valid when using punctured codes. In addition, the error divider truncates the error count since it takes 8 errors to increase the count by one, and this truncation can cause significant under-reporting of the error rate unless the value of $\mathbf{BERCT_{15\text{-}0}}$ is large enough to make the truncation insignificantly small.

Further information on the theory of operation of Viterbi decoders may be obtained from text books such as "Error-Correcting Codes", by Peterson and Weldon (MIT Press), or "Error Control Coding", by Lin and Costello (Prentice-Hall), or papers such as "Convolutional Codes and their Performance in Communication Systems", by Dr. A. J. Viterbi, IEEE Trans. on Communications, October 1971.

INPUT SIGNALS

RESET

Asynchronous master **Reset**. A logic low on this pin will clear all registers on the STEL-2050AA in both the encoder and decoder sections of the chip. **RESET** should remain low for at least 3 cycles of **ICLK** to clear the decoder. A software reset is also effected by writing dummy data to address 5_H. The address lines, **WRITE** and **CSEL** lines should generate a valid write state for at least 3 cycles of **ICLK** to clear the decoder.

ICLK, OCLK

System Clock. A crystal may be connected between **ICLK** and **OCLK** or a CMOS level clock may be fed into **ICLK**. The clock frequency should be at least 70 times the decoded data rate but no more than 18 MHz.

MICROPROCESSOR INTERFACE

DATA7-0

All I/O and control functions are accessed via the $\mathbf{DATA_{7-0}}$ bus with the associated control signals. The STEL-2050AA is used as a memory or I/O mapped peripheral to the host processor.

ADDR3-0

The 4-bit address bus is used to access the various I/O functions, as shown in the table below. Note that some addresses contain both read and write registers, i.e., the read and write mode registers at these addresses are separate and contain different data.

WRITE

The **Write** input is used to write data to the microprocessor data bus. It is active low and is normally connected to the write line of the host processor.

READ

The **Read** input is used to read data from the microprocessor data bus. It is active low and is normally connected to the read line of the host processor.

CSEL

The **C**hip **Sel**ect input can be used to selectively enable the microprocessor data bus. It is active low.

INT

The **Int**errupt output indicates when the Period Counter in the BER Monitor has completed a count period and that a new value of **BERCT** is ready to be read from addresses 7_H and 8_H, when **INT** will go high for one symbol period.

INPUT (WRITE) FUNCTIONS

ADDRESSES 0_H, 1_H
G1D2-0, G2D2-0, G3D2-0

The three 3-bit soft decision symbols are written into the registers at addresses 0_H and 1_H and the decoding process begins when the data has been written. When operating at rate $^1/_2$ the operation will begin as soon as the $\mathbf{G1D_{2-0}}$ and $\mathbf{G2D_{2-0}}$ data is written into address 0_H; when operating at rate $^1/_3$ the operation begins when the $\mathbf{G3D_{2-0}}$ data is written into address 1_H, so that it is necessary to write the $\mathbf{G1D_{2-0}}$ and $\mathbf{G2D_{2-0}}$ data first. The order in which the symbols are entered into the decoder from the registers depends on the state of the **SYNC0** and **SYNC1** bits. The decoder can make use of soft decision information, which includes both polarity information and a confidence measure, to improve the decoder performance. If hard decision (single bit) symbols are used the signals are written into bits $\mathbf{G1D_2}$, $\mathbf{G2D_2}$ and $\mathbf{G3D_2}$ and the other bits are set high. See **SM2C** for a description of the input data codes.

PNCG1, PNCG2

The **PNCG1** and **PNCG2** bits are used to control the STEL-2050AA when operating in punctured mode and are written along with the symbol data. In unpunctured operation (rates $^1/_2$ and $^1/_3$) these bits should be set low. In punctured operation the **PNCG1** bit must be set high to indicate that the G1 symbol is punctured and the **PNCG2** bit must be set high to indicate that the G2 symbol is punctured. A symbol will be punctured when the **PNCG1** or **PNCG2** bits are high when the symbol data is written into address 0_H. Zero value metrics will be substituted internally for the actual metrics corresponding to the $\mathbf{G1_{2-0}}$ or $\mathbf{G2_{2-0}}$ data at that time.

ADDRESS 2_H
$\mathbf{THRESH_{2-0}}$

A counter is used to determine the number of either traceback mismatches or metric renormalizations per 256 bits in the auto node-sync circuit, and the threshold at which the counter triggers the **SST0** and **SST1** bits to change states is set with the data on the $\mathbf{THRESH_{2-0}}$ bits. The threshold values will be as shown in the following table.

$\mathbf{THRESH_{2-0}}$	Threshold value
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Since the actual error rate obtained will depend on the signal to noise ratio (E_b/N_o) in the signal, the optimum value of the threshold will also depend on E_b/N_o and should be set accordingly. The actual mismatch or renomalization count is stored in the read mode register at address 6_H.

MIS

Two algorithms for auto node-sync are incorporated into the STEL-2050AA. When the **MIS** bit is set high the Traceback **Mis**match algorithm is selected, and when this bit is set low the Metric Renormalization algorithm is selected.

SCRAM0, SCRAM1

The **Scram**ble bits are used to enable the three different scrambler functions included in the STEL-2050AA, as shown in the following table:

SCRAM0	SCRAM1	FUNCTION
0	0	Scrambler disabled
1	0	Invert G2
0	1	V.35 (CCITT compatible)
1	1	V.35 (IESS compatible)

The "Invert G2" scrambler simply inverts the G2 symbols generated in the encoder. The decoder then re-inverts the received G2 symbols before decoding. Two different "V.35" scrambler formats are provided since there are two versions of this standard in existence: the true, CCITT version of the standard, and the IESS version, which has become a de facto standard through widespread use. In each case, the scrambling function is provided at the encoder and the descrambler is provided at the decoder.

SM2C

The state of the **S**igned **M**agnitude/**2**'s **C**omplement bit determines the format of the incoming soft-decision symbols into the decoder. When **SM2C** is set high the input code is Signed Magnitude, and when it is low the code is Two's Complement. The codes are shown in the following table:

CODE CONTROL: SYMBOL INPUT:	SM2C=1 GXD2-GXD0	SM2C=0 GXD2-GXD0
Most Confident '+' level	0 1 1	0 1 1
Data = 0	0 1 0	0 1 0
	0 0 1	0 0 1
Least Confident '+' level	0 0 0	0 0 0
Least Confident '–' level	1 0 0	1 1 1
Data = 1	1 0 1	1 1 0
	1 1 0	1 0 1
Most Confident '–' level	1 1 1	1 0 0

The **SM2C** bit should be set high when using hard decision data. The polarity of the input signals is such that a constant + level on both G1 and G2 produces an output data stream of zeros.

DRATE

The **D**ecoder **Rate** bit selects whether the decoder will read two symbols (**DRATE** set high) or three symbols (**DRATE** set low) for every data bit decoded. During rate $^1/_2$ operation the G3 symbol is completely ignored by the decoder. **DRATE** should be set high for rate $^3/_4$ operation.

ADDRESS 3_H
SYNC0, SYNC1

The Symbol **Sync0** and Symbol **Sync1** bits are used for the node sync operation. When using the internal auto node sync mode these two bits are overwritten by **SST0** and **SST1**, respectively by setting the **AUTONS** bit high. When this is done it is necessary to avoid writing data into address 3_H during the operation of the decoder to prevent manually overwriting the **SYNC0** and **SYNC1** bits, since this will affect the operation of the auto node sync circuit. The operation of the decoder is affected in the following way by the **SYNC0** and **SYNC1** inputs:

RATE	SYNC0	SYNC1	Symbol entered into decoder during symbol period N: G1	G2	G3
1	0	0	$G1_N$	$G2_N$	–
1	1	0	$G2_{N-1}$	$G1_N$	–
1	0	1	$\overline{G2_N}$	$G1_N$	–
1	1	1	$\overline{G2_{N-1}}$	$G1_N$	–
0	0	0	$G1_N$	$G2_N$	$G3_N$
0	1	0	$G3_{N-1}$	$G1_N$	$G2_N$
0	0	1	$G2_{N-1}$	$G3_{N-1}$	$G1_N$
0	1	1	Invalid state		

Note that whenever the states of the **SYNC0** and **SYNC1** inputs are changed there will be a delay of 71 bit periods before valid data starts appearing at the decoder output.

AUTONS

When the **AUTONS** bit is set high it causes the **SST0** and **SST1** bits to overwrite the **SYNC0** and **SYNC1** bits respectively, thereby turning on the internal auto node sync function.

DIFEN

When the **DIFEN** bit is set high the differential encoder and decoder in the STEL-2050AA are enabled. Differential encoding is done after V.35 scrambling (when used) but before Invert G2 scrambling (when used) in the encoder. The sequence is reversed in the decoder. Note that the BER monitor function will only operate correctly when this bit is set low.

ADDRESS 4_H
DATAIN

The Encoder input data bit is written into the register at address 4_H. A **DATACLK** signal is automatically generated internally each time data is written into this location, causing the data to be latched into the encoder shift register and generating a new set of encoded symbols. When the encoder is used in a burst application the encoder register should be flushed with seven dummy data bits (zeroes) at the end of the burst.

ADDRESS 5_H
RESET

A software reset is effected by writing dummy data to address 5_H. The address lines, **WRITE** and **CSEL** lines

should generate a valid write state for at least 3 cycles of **ICLK** to clear the decoder.

ADDRESSES 6_H - 8_H
$BPER_{23-0}$

The 24-bit **B**ER **Per**iod data is used to set the period (number of data bits) over which the mean BER is measured by the BER Monitor. The period used is 1000 times the value of $BPER_{23-0}$.

OUTPUT (READ) FUNCTIONS

ADDRESS 3_H
DOUT

Decoded **D**ata **Out**. The signal is stored in the read register at address 3_H when the next symbol data is written to start the decoding process for the next bit. There is a delay of 71 data bits from the time a set of symbols is written into the STEL-2050AA to the time the corresponding data bit is available. Consequently, in order to flush the last 71 bits of data out of the system at the end of a burst it is necessary to continue writing dummy input symbols and reading the output data for 71 symbol periods after the last valid symbol has been entered.

G1ERR, G2ERR and G3ERR

The **G1 Err**or, **G2 Err**or and **G3 Err**or bits indicate that an error has been detected in the G1, G2 or G3 symbols, respectively, corresponding to the current output bit. These functions will only be valid when operating at rates $^1/_2$ and $^1/_3$ with the **DIFEN** bit set low.

BERR

The **B**it **Err**or bit indicates that an error has been detected in any of the symbols corresponding to the current output bit. This function is the logical OR of **G1ERR**, **G2ERR**, and (at rate $^1/_3$ only) **G3ERR**. This function will only be valid when operating at rates $^1/_2$ and $^1/_3$ with the **DIFEN** bit set low.

ADDRESS 4_H
SYNC

The **Sync** bit provides an indication of the status of the internal auto node sync circuit. This bit will pulse high for one symbol period if the mismatch or renormalization count exceeds the threshold value, indicating that the node sync has been changed.

SST0, SST1

The **S**ync **St**ate **0** and **S**ync **St**ate **1** signals are the outputs of the internal auto node sync circuit. They will overwrite the **SYNC0** and **SYNC1** bits respectively when **AUTONS** is set high. They may also be used in conjunction with an external node sync algorithm implementation which can use the **SST0** and **SST1** data.

MSMCH

The **MSMCH** bit is normally set high. It will be set low each time a traceback mismatch occurs and will stay low for one bit period. When using the Traceback Mismatch algorithm for automatic node sync the mismatch counter will be incremented at the same time.

RNORM

The **RENORM** bit is normally set low. It will be set high each time the metrics are renormalized and will stay high for one bit period. When using the Metric Renormalization algorithm for automatic node sync the renormalization counter will be incremented at the same time.

ADDRESS 5_H
G1OUT, G2OUT, G3OUT

These are the output Symbols from the Encoder. They depend on the seven most recent data bits (**DATAIN**) clocked into the encoder shift register and are formed by the modulo-2 sum of the inputs to the generators from the 7-bit shift register. They are stored in the read mode register at address 5_H.

ADDRESS 6_H
COUNT7-0

The 8-bit **Count** data gives the current value of the mismatch or renormalization count which is used for comparison with the threshold.

ADDRESSES 7_H - 8_H
BERCT15-0

The 16-bit **B**it **Err**or **C**oun**t** data represents the mean Bit Error Rate over the period determined by the BER Period data $BPER_{23-0}$. The actual BER is given by:

$$BER = \frac{8 \times BERCT_{15-0}}{1000 \times BPER_{23-0}}$$

The value will be updated each time the period counter completes its count. This will be indicated by the **INT** output going high for one clock cycle. If the accumulator overflows during a measurement period its output will be caused to saturate at a value of $FFFF_H$. Note that the BER monitor will indicate an error each time an input symbol is punctured, so that the BER indicated by the $BERCT_{15-0}$ output will not be valid when using punctured codes unless the effect of the puncturing can be compensated externally.

ADDRESS E_H
ACK

Acknowledge. The signal is stored in the read register at address E_H. This bit goes high when a new symbol set has been written into the decoder and the decoding process has started and goes low again 70 clock cycles later to indicate that a new data bit is ready to be read.

MICROPROCESSOR INTERFACE MEMORY MAP

WRITE MODE REGISTERS

$ADDR_{3-0}$	$DATA_7$	$DATA_6$	$DATA_5$	$DATA_4$	$DATA_3$	$DATA_2$	$DATA_1$	$DATA_0$
0*	PNCG1	G1D2	G1D1	G1D0	PNCG2	G2D2	G2D1	G2D0
1*						G3D2	G3D1	G3D0
2*	DRATE	SM2C	SCRAM0	SCRAM1	MIS	$THRESH_2$	$THRESH_1$	$THRESH_0$
3					DIFEN	AUTONS	SYNC1	SYNC0
4								DATAIN
5								RESET
6	$BPER_7$	$BPER_6$	$BPER_5$	$BPER_4$	$BPER_3$	$BPER_2$	$BPER_1$	$BPER_0$
7	$BPER_{15}$	$BPER_{14}$	$BPER_{13}$	$BPER_{12}$	$BPER_{11}$	$BPER_{10}$	$BPER_9$	$BPER_8$
8	$BPER_{23}$	$BPER_{22}$	$BPER_{21}$	$BPER_{20}$	$BPER_{19}$	$BPER_{18}$	$BPER_{17}$	$BPER_{16}$

* Indicates that these are also readable registers

READ MODE REGISTERS

$ADDR_{3-0}$	$DATA_7$	$DATA_6$	$DATA_5$	$DATA_4$	$DATA_3$	$DATA_2$	$DATA_1$	$DATA_0$
3				BERR	G3ERR	G2ERR	G1ERR	DOUT
4				RNORM	MSMCH	SST1	SST0	SYNC
5						G3OUT	G2OUT	G1OUT
6	$COUNT_7$	$COUNT_6$	$COUNT_5$	$COUNT_4$	$COUNT_3$	$COUNT_2$	$COUNT_1$	$COUNT_0$
7	$BERCT_7$	$BERCT_6$	$BERCT_5$	$BERCT_4$	$BERCT_3$	$BERCT_2$	$BERCT_1$	$BERCT_0$
8	$BERCT_{15}$	$BERCT_{14}$	$BERCT_{13}$	$BERCT_{12}$	$BERCT_{11}$	$BERCT_{10}$	$BERCT_9$	$BERCT_8$
E	ACK							

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{ss}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125	°C (Plastic package)
		–65 to +150	°C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD}+0.3	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 5%	Volts (Commercial grade)
		+5 ± 10%	Volts (Military grade)
T_a	Operating Temperature (Ambient)	0 to +70	°C (Commercial grade)
		–55 to +125	°C (Military grade)

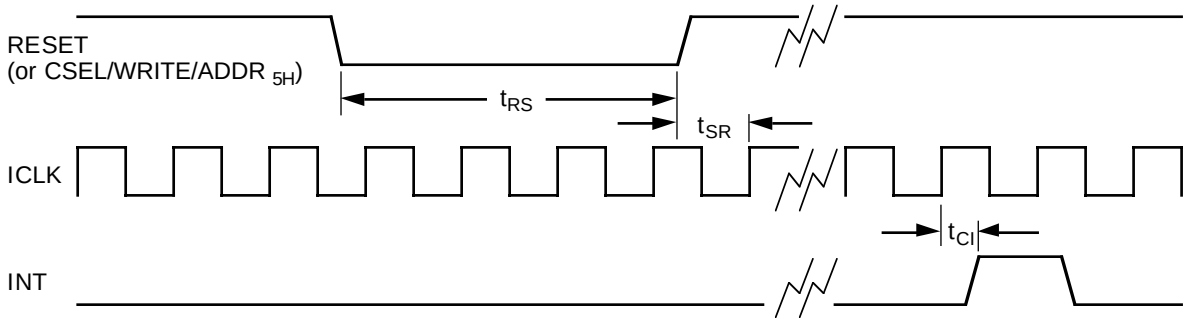
D.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			2.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	µA	$V_{IN} = V_{DD}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –6.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +6.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

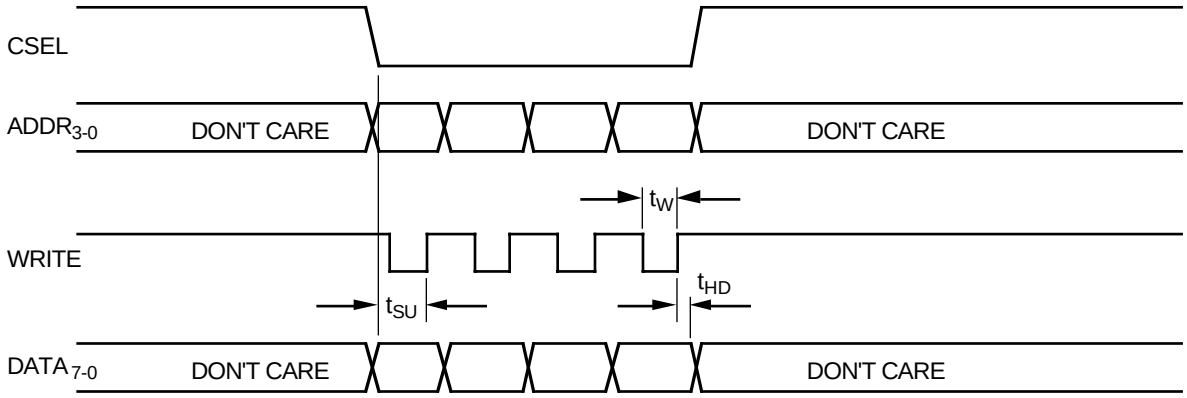
A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military)

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{RS}	**RESET** pulse Width	$3*t_{ICLK}$			
t_{SR}	**RESET** to **ICLK** Setup	2		nsec.	
t_W	**WRITE** Pulse Width	5		nsec.	
t_{CI}	**ICLK** to **INT** Delay	10	35	nsec.	
t_{SU}	**CSEL**, **DATA** or **ADDR** to **WRITE** or **READ** setup	5		nsec.	
t_{HD}	**WRITE** or **READ** to **CSEL**, **DATA** or **ADDR** hold	5		nsec.	
t_{ZV}	**DATA** Hi-Z to valid		12	nsec.	Load = 15 pF
t_{VZ}	**DATA** valid to Hi-Z		12	nsec.	Load = 15 pF

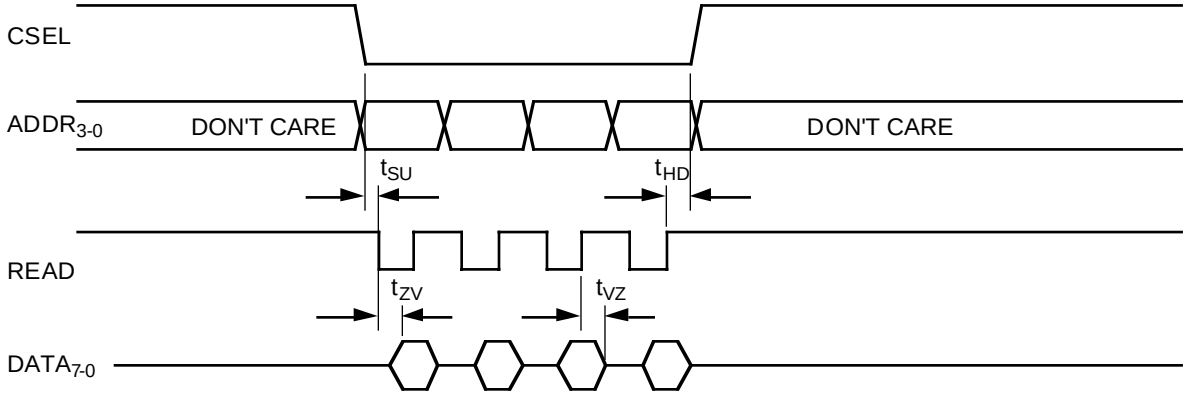
RESET AND MICROPROCESSOR INTERFACE TIMING



1. WRITE OPERATONS



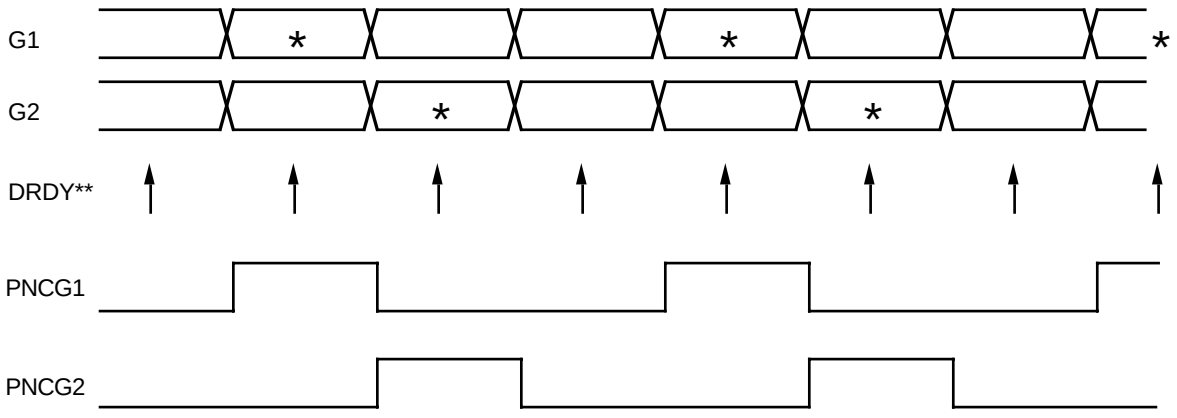
2. READ OPERATONS



PUNCTURED MODE OPERATION

In punctured codes some of the symbols generated by the convolutional encoder are deleted, or punctured, from the transmitted sequence. For example, in an unpunctured rate $^1/_2$ sequence, four bits would be transmitted for every two data bits. If every fourth bit was punctured from the sequence then only three bits would be transmitted for every two data bits. This would result in a rate $^2/_3$ code. The STEL-2050A is designed to operate in punctured mode as well as normal, rate $^1/_2$, mode. This is easily accomplished by means of the **PNCG1** and **PNCG2** bits, which delete the symbol which would normally have been loaded into the decoder at the time when either of these bits is set high. The punctured symbols are replaced internally by zero metric values. The Viterbi algorithm treats the zero value metrics by giving them zero weight in the computations relative to the other symbols. The coding gain is significantly less than that for unpunctured operation, but this is the trade-off for the reduced bandwidth required to transmit the symbols. The recommended puncturing sequences for rates $^2/_3$ and $^3/_4$ punctured operation are shown in the table. The sequences shown in boldface are the basic sequence, which are then repeated. The use of the **PNCG1** and **PNCG2** bits is shown below for rate $^3/_4$. The punctured symbols are marked with asterisks. Rates higher than $^3/_4$ are not recommended with the STEL-2050A.

Rate	Symbol sequence
$^2/_3$	**G1 G2 G1 P** G1 G2 G1 P G1 G2 G1 P G1 G2 G1 P G1 G2
$^3/_4$	**G1 G2 P G2 G1 P** G1 G2 P G2 G1 P G1 G2 P G2 G1 P



* Denotes punctured symbols.
** Denotes that DRDY is set high at these times.

USING AUTOMATIC NODE SYNC

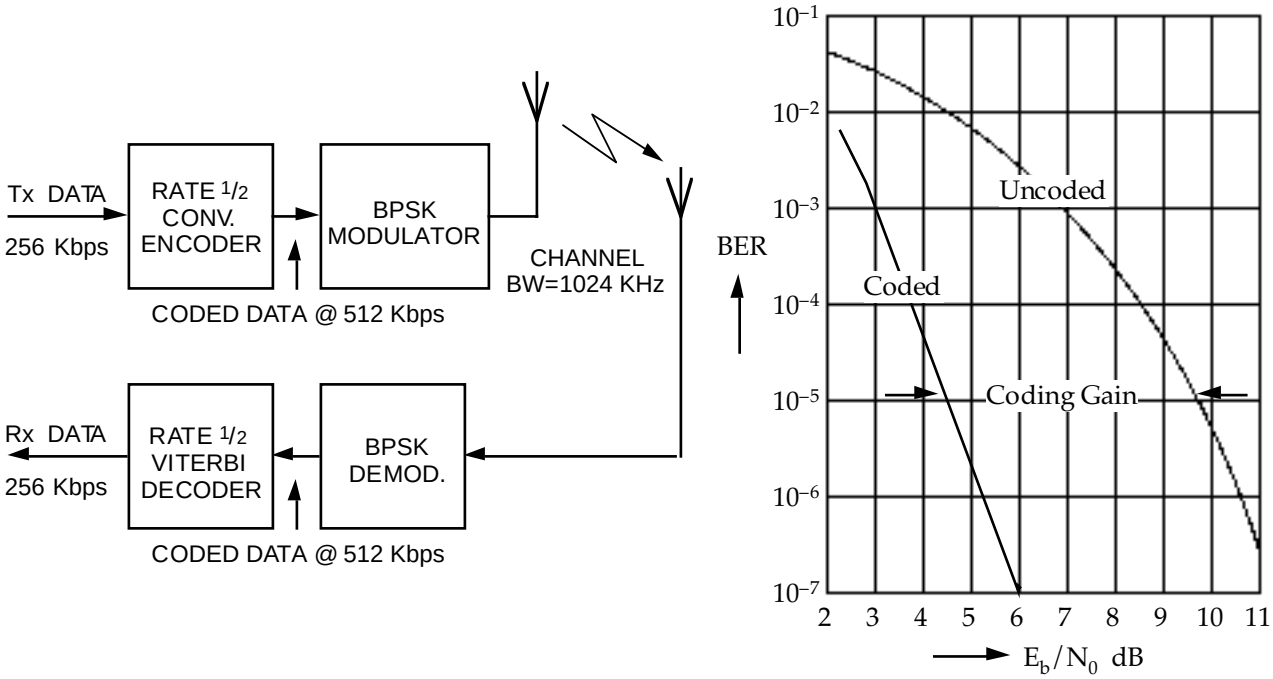
The automatic node sync circuit built into the STEL-2050A can be used to provide node sync in applications where this is not intrinsic to the nature of the operation. The automatic node sync is enabled by setting the **AUTONS** bit high. The threshold should be set according to the expected signal to noise ratio of the input signal for optimum operation of the system.

BPSK COMMUNICATION SYSTEM USING CONVOLUTIONAL ENCODING AND VITERBI DECODING. RATE = 1/2

The STEL-2050A can be used in a variety of different environments. One example is shown below. It cannot be used as a common encoder or decoder in multi-channel applications because of the memory incorporated on the chip which is dedicated to a single channel.

An example of a system using the convolutional coder and Viterbi decoder is illustrated here. The system modulates a data stream of rate 512 Kbps using binary PSK (BPSK). To be able to use convolutional coding/decoding, the system must have available the additional bandwidth needed to transmit symbols at twice the data rate (for rate 1/2 encoding). Alternatively, the system could make use of two parallel channels to transmit two streams of symbols at the data rate. The performance improvement that can be expected is shown in the graph below.

The convolutional encoder is functionally independent from the decoder. A single data bit is clocked into the 7 bit shift register on the rising edge of **DATA CLK**. The decoder portion of the STEL-2050A is designed to accept symbols synchronously. **DRDY** is supplied by the user to clock in the symbols. The maximum data rate is 256 Kbps, using a clock frequency of 18 MHz. This corresponds to 512 K symbols per second at rate 1/2 and 768 K symbols per second at rate 1/3. 18 MHz crystals are readily available, and this clock frequency can be used at all data rates, although the power consumption can be reduced by using lower clock frequencies.



BPSK Communication System using Convolutional Encoding and Viterbi Decoding. Rate = 1/2

For Further Information Call or Write

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