2.5V/3V, 3.0GHz CML AnyGate™ ANY LOGIC w/50Ω or 100Ω OUTPUTS

FEATURES

- **Guaranteed AC parameters over temperature:**
  - **f_{MAX} > 3.0GHz (SY55851A)**
  - **t_r / t_f < 100ps**
  - **Propagation delay < 280ps**
- **Guaranteed operation over –40°C to +85°C temperature range**
- **Wide supply voltage range: 2.3V to 3.6V**
- **Single IC provides 8 logic functions**
- **2:1 MUX capability**
- **Fully differential I/O**
- **Source terminated CML outputs for fast edge rates:**
  - **SY55851 for 100Ω load**
  - **SY55851A for 50Ω load**
- **Guaranteed matched propagation delays:**
  - **Select (S)-to-out: < 280ps**
  - **Input (A and B)-to-out: < 280ps**
- **Accepts PECL, LVPECL, CML input signals**
- **Functions as a PECL/LVPECL-to-CML translator**
- **Available in a 10-pin (3mm × 3mm) MSOP package**

DESCRIPTION

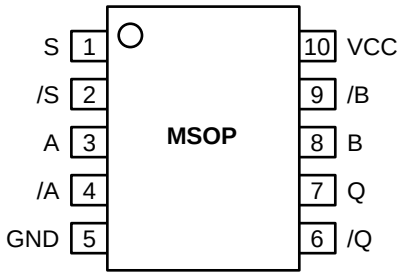
The SY55851 and SY55851A are highly flexible, universal logic gates capable of up to 3.0GHz operation (SY55851A). These AnyGate differential logic devices will produce all possible logic functions of two Boolean variables. They can be configured as any of the following gates: AND, NAND, OR, NOR, XOR, XNOR, DELAY, NEGATION (NOT). The SY55851 and SY55851A can also function as a 2-input multiplexer.

The SY55851 has an output stage optimized for 100Ω loads, and the SY55851A is optimized for 50Ω loads. The differential inputs for both devices are normally terminated with a single resistor (100Ω) between the true and complement pins.

APPLICATIONS

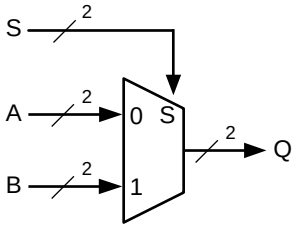
- **Port bypass**
- **Data communication systems**
- **Wireless communication systems**
- **Telecom systems**

PIN CONFIGURATION



SY55851 and SY55851A

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

Pin	Function
A, /A	CML, PECL, LVPECL Input
B, /B	CML, PECL, LVPECL Input
Q, /Q	Differential CML Output
S, /S	CML, PECL, LVPECL Input Selector
GND	Ground
V_{CC}	V_{CC}

PIN DESCRIPTIONS

A, /A – CML Input (Differential)

This is one of the differential inputs to the logic block. For a 2-variable logic function, it is either a constant value or a Boolean input. For a 2-input mux, this signal represents the output when S is set to logic zero.

B, /B – CML Input (Differential)

This is one of the differential inputs to the logic block. For a 2-variable logic function, it is either a constant value or a Boolean input. For a 2-input mux, this signal represents the output when S is set to logic one.

Q, /Q – CML Output (Differential)

This is the differential CML output for the logic block. For termination guidelines, see **Figure 3**.

S, /S – CML Input (Differential)

This differential CML input is one of the inputs to the logic block. It represents either one Boolean input for a 2-variable logic function, or the select input for a 2-input mux.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased to $V_{CC}/2$ through an internal voltage divider consisting of two 75kΩ resistors. Since some logic functions necessitate an output to be connected to two inputs, SY55851/A inputs have no internal terminations. Typically, one resistor between the true and complement input is all that is required, as per **Figure 3**. To keep an input at static logic zero at $V_{CC} \geq 3.0V$, leave both inputs unconnected or tie the complement input to V_{CC}. For $V_{CC} < 3.0V$ applications, connect the complement input to V_{CC} and leave the true input unconnected. To make an input static logic one, connect the true input to V_{CC}, and leave the complement input unconnected. These are the only safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (no connect) pins should be unconnected.

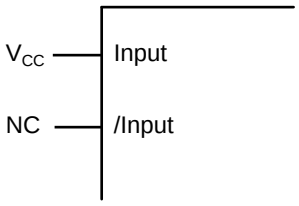
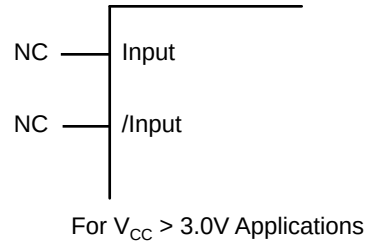


Figure 1. Hard Wiring A Logic "1" (1)

NOTE:

1. Input is either A, B, S input, and /Input is either /A, /B, /S input.



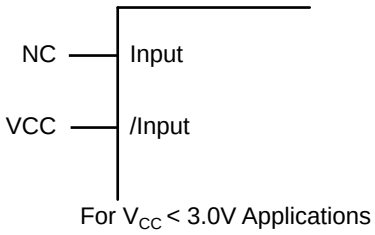
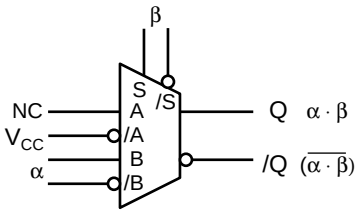


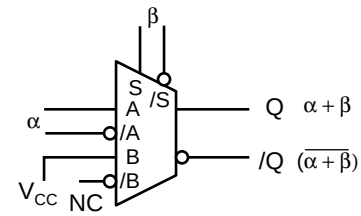
Figure 2. Hard Wiring A Logic "0" (1)

TRUTH TABLES



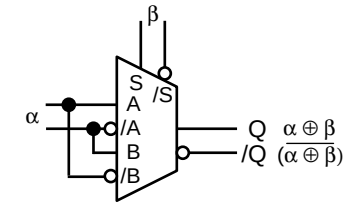
AND/NAND

A	α B	β S	α·β Q	(α·β) /Q
L	L	L	L	H
L	H	L	L	H
L	L	H	L	H
L	H	H	H	L



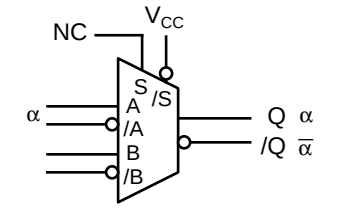
OR/NOR

α A	B	β S	α + β Q	(α + β) /Q
L	H	L	L	H
H	H	L	H	L
L	H	H	H	L
H	H	H	H	L



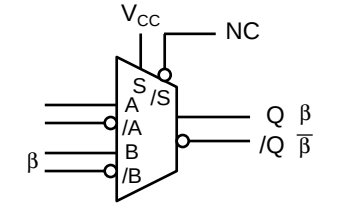
XOR/XNOR

α A	B	β S	α ⊕ β Q	(α ⊕ β) /Q
L	H	L	L	H
L	H	H	H	L
H	L	L	H	L
H	L	H	L	H

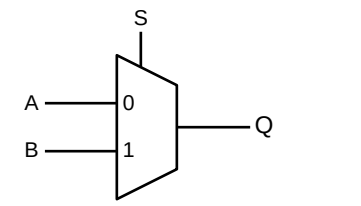


DELAY/NEGATION

α A	B	S	α Q	$\overline{\alpha}$ /Q
L	X	L	L	H
H	X	L	H	L



A	β B	S	β Q	$\overline{\beta}$ /Q
X	L	H	L	H
X	H	H	H	L



2:1 MUX

S	Q
H	B
L	A

CML TERMINATION AND TTL INTERFACE

All inputs accept the output from any other member of this family. All outputs are source terminated 100Ω or 50Ω CML differential drivers as shown in Figure 3. All inputs to the SY55851/A must be externally terminated. SY55851/A inputs are designed to accept a termination resistor between the true and complement inputs of a differential pair. 0402 form factor chip resistors will fit with some trace fanout.

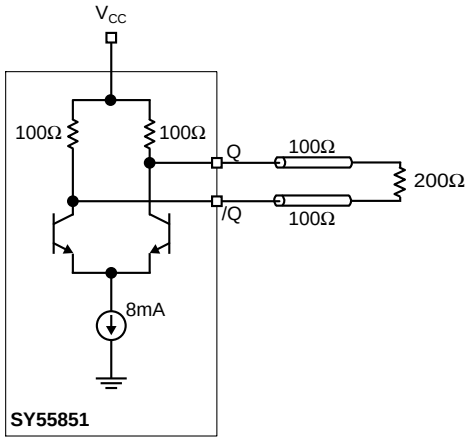


Figure 3a. SY55851
100Ω Load CML Output

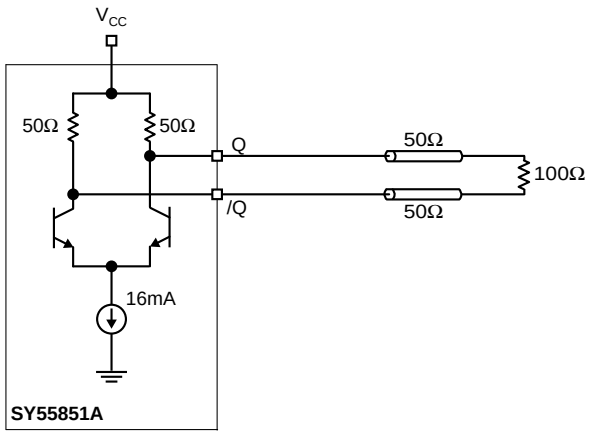


Figure 3b. Differentially Terminated SY55851A
(50Ω Load CML Output)

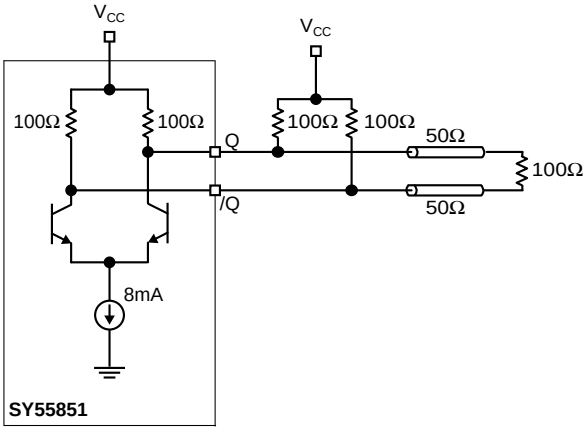


Figure 3c. Differentially Terminated SY55851
(50Ω Load CML Output)

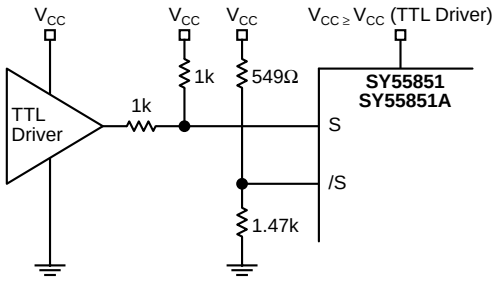


Figure 4. Interfacing TTL-to-CML Select Inputs

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{CC}	Power Supply Voltage		–0.5 to +6.0	V
V_{IN}	Input Voltage		–0.5 to V_{CC} +0.5	V
V_{OUT}	CML Output Voltage		V_{CC} –1.0 to V_{CC} +0.5	V
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)	–Still-Air (multi-layer PCB) –500lfpm (multi-layer PCB)	113 96	°C/W °C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)		42	°C/W

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	2.3	—	3.6	V	
I_{CC}	Power Supply Current					
	SY55851	—	—	40	mA	No Load
	SY55851A	—	46	60	mA	No Load

CML DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.3V to 3.6V; GND = 0V; T_A = –40°C to +85°C[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{ID}	Differential Input Voltage	100	—	—	mV	
V_{IH}	Input HIGH Voltage	1.6	—	V_{CC}	V	
V_{IL}	Input LOW Voltage	1.5	—	V_{CC} – 0.1	V	
V_{OH}	Output HIGH Voltage	V_{CC} – 0.040	V_{CC} – 0.010	V_{CC}	V	No Load
V_{OL}	Output LOW Voltage	V_{CC} – 1.00	V_{CC} – 0.800	V_{CC} – 0.65	V	No Load
V_{OUT}	Output Voltage Swing[2]	0.650	0.800	1.00	V	No Load
	SY55851	— —	0.400 0.200	— —	V V	100Ω Load[3] 50Ω Load[4] (SY55851)
	SY55851A	—	0.400	—	V	50Ω Load[5] (SY55851A)
R_{OUT}	Output Source Impedance					
	SY55851	80	100	120	Ω	
	SY55851A	40	50	60	Ω	

NOTES:

1. The DC parameters are guaranteed after thermal equilibrium has been established.
2. Actual voltage levels and differential swing will depend on customer termination scheme. Refer to the “CML Termination” diagram for more details.
3. Applies to SY55851: 200Ω termination resistor across Q and /Q. See **Figure 3a**.
4. Applies to the SY55851. See **Figure 3c**.
5. Applies to the SY55851A: 100Ω termination resistor across Q and /Q. See **Figure 3b**.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 2.3V to 3.6V; GND = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{MAX}[2]	Max. Operating Frequency					
	SY55851	2.5	—	—	GHz	
	SY55851A	3.0	—	—	GHz	
$t_{PD(S-Q)}$	Propagation Delay					
	(S to Q) SY55851	—	—	350	ps	
	SY55851A	130	—	280	ps	
t_{PD}	Propagation Delay					
(A-Q and B-Q)	(A-Q and B-Q) SY55851	—	—	350	ps	
	SY55851A	130	—	280	ps	
t_r	CML Output Rise/Fall Times					
t_f	(20% to 80%) SY55851	—	—	110	ps	
	SY55851A	—	65	100	ps	

NOTES:

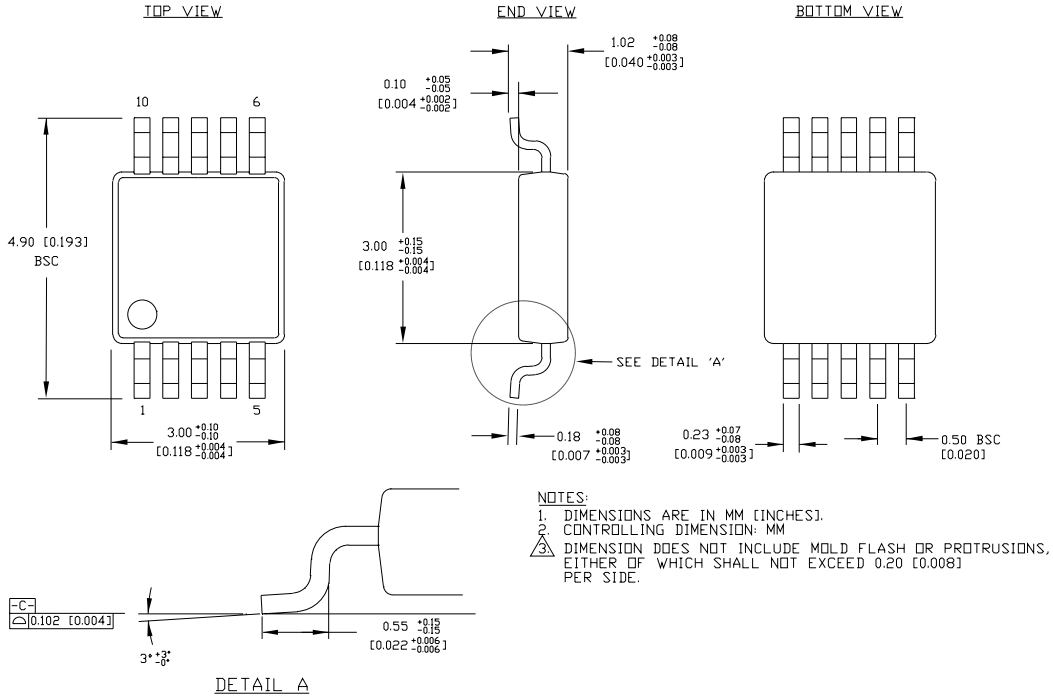
1. SY55851: outputs terminated to 50Ω equivalent load. See **Figure 3c**.
   SY55851A: outputs terminated to 50Ω load. See **Figure 3b**
2. f_{MAX} represents a maximum toggle rate in which the output still meets CML logic swing.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Package Marking	Description
SY55851UKI	K10-1	Industrial	851U	100Ω Load
SY55851UKITR*	K10-1	Industrial	851U	100Ω Load
SY55851AUKI	K10-1	Industrial	851A	50Ω Load
SY55851AUKITR*	K10-1	Industrial	851A	50Ω Load

*Tape and Reel.

10 LEAD MSOP (K10-1)



Rev. 00

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB http://www.synergysemi.com http://www.micrel.com