DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

# μPD168101

## MONOLITHIC QUAD H-BRIDGE DRIVER CIRCUIT

### DESCRIPTION

The μPD168101 is monolithic quad H-bridge driver LSI which uses power MOSFETs in the output stages. By using the MOS process, this driver IC has substantially improved the voltage loss of the output stage and power consumption as compared with conventional driver circuits using bipolar transistors.

By eliminating the charge pump circuit, the current during power-OFF is drastically decreased.

In addition, a low-voltage malfunction prevention circuit is also provided that prevents the IC from malfunctioning when the supply voltage drops.

As the package, a 24-pin plastic TSSOP is adopted to enable the creation of compact, slim application sets.

This driver IC can drive two stepping motor at the same time, and is ideal for driving stepping motors in the lens of a camera. It is the best for lens drive drivers, such as a digital camera and a video camera. Moreover, since the input of two terminals is respectively owned to H bridge 1 circuit, a maximum of four loads, such as DC motor, can be driven simultaneously.

### FEATURES

- ○ Four H bridge circuits employing power MOSFETs
- ○ Low current consumption by eliminating charge pump
  $V_M$ pin current when power-OFF: 10 μA MAX. $V_{DD}$ pin current: 10 μA MAX.
- ○ Input logic frequency: 100 kHz
- ○ 3-V power supply
  Minimum operating supply voltage: 2.5 V
- ○ Low voltage malfunction prevention circuit
- ○ 24-pin plastic TSSOP (5.72 mm (225))

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD168101MA-6A5 | 24-pin plastic TSSOP (5.72 mm (225)) |

**The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
**Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.**

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## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

**When mounted on a glass epoxy board (10 cm × 10 cm × 1 mm, 15% copper foil)**

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Control block supply voltage | $V_{DD}$ | | –0.5 to +6.0 | V |
| | $V_M$ | | –0.5 to +6.0 | V |
| Input voltage | $V_{IN}$ | | –0.5 to $V_{DD}$ + 0.5 | V |
| Output terminal voltage | $V_{OUT}$ | | 6.2 | V |
| Output current | $I_{M(DC)}$ | DC | ±0.35 | A/ch |
| | $I_{M(pulse)}$ | PW ≤ 10 ms, Duty ≤ 5% | ±0.7 | A/ch |
| Power consumption | $P_T$ | | 0.7 | W |
| Peak junction temperature | $T_{CH(MAX)}$ | | 150 | °C |
| Storage temperature range | $T_{stg}$ | | –55 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

**When mounted on a glass epoxy board (10 cm × 10 cm × 1 mm, 15% copper foil)**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Control block supply voltage | $V_{DD}$ | | 2.5 | | 5.5 | V |
| | $V_M$ | | 2.7 | | 5.5 | V |
| Output current | $I_{M(DC)}$ | DC | –0.25 | | +0.25 | A |
| Operating frequency | $f_{IN}$ | IN terminal | | | 100 | kHz |
| Operating temperature range | $T_A$ | | –10 | | 85 | °C |
| Peak junction temperature | $T_{CH(MAX)}$ | | | | 125 | °C |

## CHARACTERISTICS (Unless otherwise specified, $V_{DD}$ = $V_M$ = 3 V, $T_A$ = 25°C)

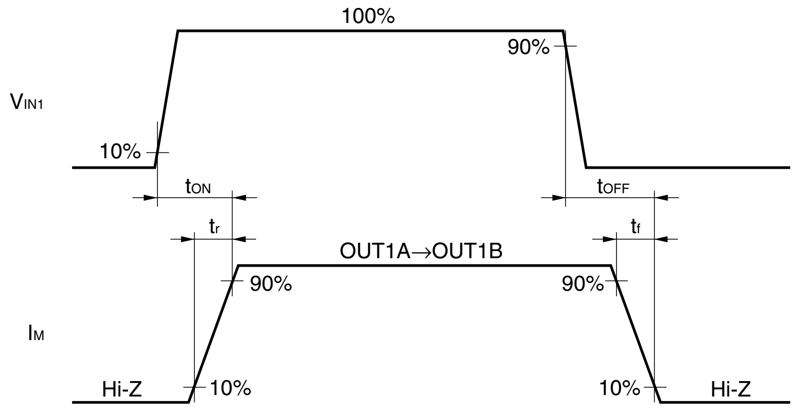
| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Off state $V_M$ pin current | $I_{M(OFF)}$ | All control terminal = 0 V<br>Per $V_M$ terminal | | | 10 | $\mu$A |
| $V_{DD}$ terminal current at the time of standby | $I_{DD(ST)}$ | All control terminal = 0 V | | | 10 | $\mu$A |
| $V_{DD}$ terminal current at the time of operation | $I_{DD}$ | | | | 1 | mA |
| High level input current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | | | 0.06 | mA |
| Low level input current | $I_{IL}$ | $V_{IN}$ = 0 V | –1.0 | | | $\mu$A |
| Input pull down resistance | $R_{IND}$ | | 50 | | 200 | kΩ |
| High level input voltage | $V_{IH}$ | 2.5 V ≤ $V_{DD}$ ≤ 5.5 V | 0.7 × $V_{DD}$ | | $V_{DD}$+0.3 | V |
| Low level input voltage | $V_{IL}$ | 2.5 V ≤ $V_{DD}$ ≤ 5.5 V | –0.3 | | 0.3 × $V_{DD}$ | V |
| H-bridge ON resistance | $R_{ON}$ | 2.7 V ≤ $V_M$ = $V_{DD}$ ≤ 5.5 V<br>$I_M$ = 0.25 A, Upper + lower | | 0.7 | 1.1 | Ω |
| Low voltage malfunction prevention circuit operating voltage | $V_{DDS1}$ | $V_M$ = 5 V, –10°C ≤ $T_A$ ≤ +85°C | 0.8 | | 2.5 | V |
| | $V_{DDS2}$ | $V_M$ = 3 V, –10°C ≤ $T_A$ ≤ +85°C | 0.65 | | 2.5 | V |
| H bridge output turn-on time 1 | $t_{ON1}$ | $R_M$ = 20 Ω, Figure 1<br>$t_{ON1}$: turn-on time from all control = 0 V<br>$t_{ON2}$: turn-on time at operation | | 1.0 | | $\mu$s |
| H bridge output turn-on time 2 | $t_{ON2}$ | | | 0.7 | 2.0 | $\mu$s |
| H bridge output turn-off time | $t_{OFF}$ | | | 0.2 | 0.5 | $\mu$s |
| H bridge output rise time | $t_r$ | | | 0.3 | 1.0 | $\mu$s |
| H bridge output fall time | $t_f$ | | | 0.07 | 0.2 | $\mu$s |

**Remarks 1.** As for thermal shutdown circuit (TSD), junction temperature operates above 150°C. At the time of over thermal detection, current supply is stopped by making all output terminals into high impedance. In addition, thermal shutdown circuit does not operate at the time of standby.

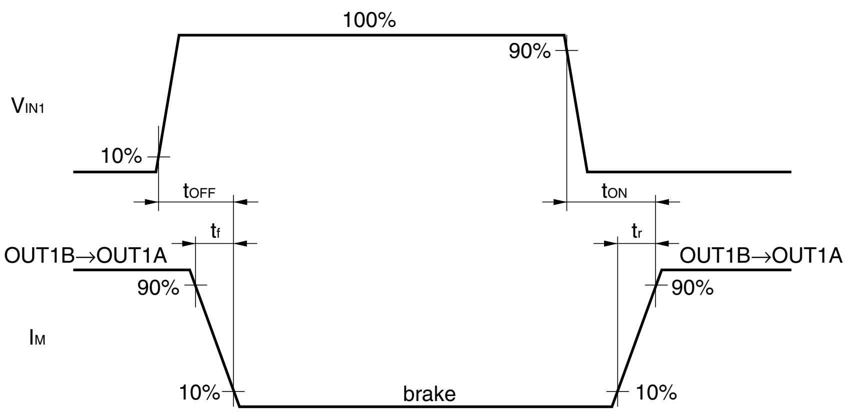
**2.** A low voltage malfunction operation prevention circuit operates, if a voltage power supply ($V_{DD}$) becomes less than 2.5 V. All output terminals be high impedance at the time of UVLO operation.

**Figure 1. Switching time condition**

**(1) IN2 = Low-level**




**(2) IN2 = High-level**




## FUNCTION TABLE

The logic of each channel is as follows

Channel 1

| IN1 | IN2 | OUT1A | OUT1B |
|---|---|---|---|
| L | L | Z | Z |
| L | H | L | H |
| H | L | H | L |
| H | H | L | L |

Channel 2

| IN3 | IN4 | OUT2A | OUT2B |
|---|---|---|---|
| L | L | Z | Z |
| L | H | L | H |
| H | L | H | L |
| H | H | L | L |

Channel 3

| IN5 | IN6 | OUT3A | OUT3B |
|---|---|---|---|
| L | L | Z | Z |
| L | H | L | H |
| H | L | H | L |
| H | H | L | L |

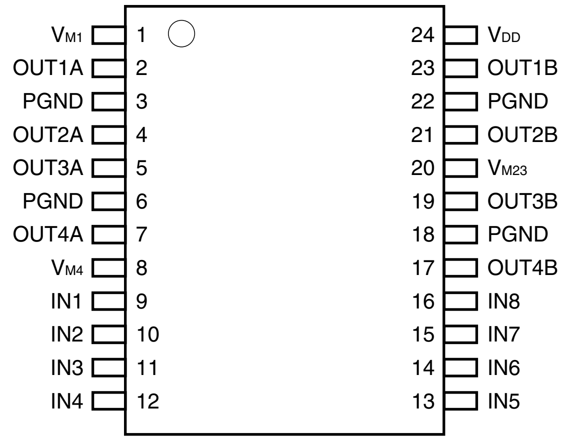
Channel 4

| IN7 | IN8 | OUT4A | OUT4B |
|---|---|---|---|
| L | L | Z | Z |
| L | H | L | H |
| H | L | H | L |
| H | H | L | L |

H: High-level, L: Low-level, Z: High impedance

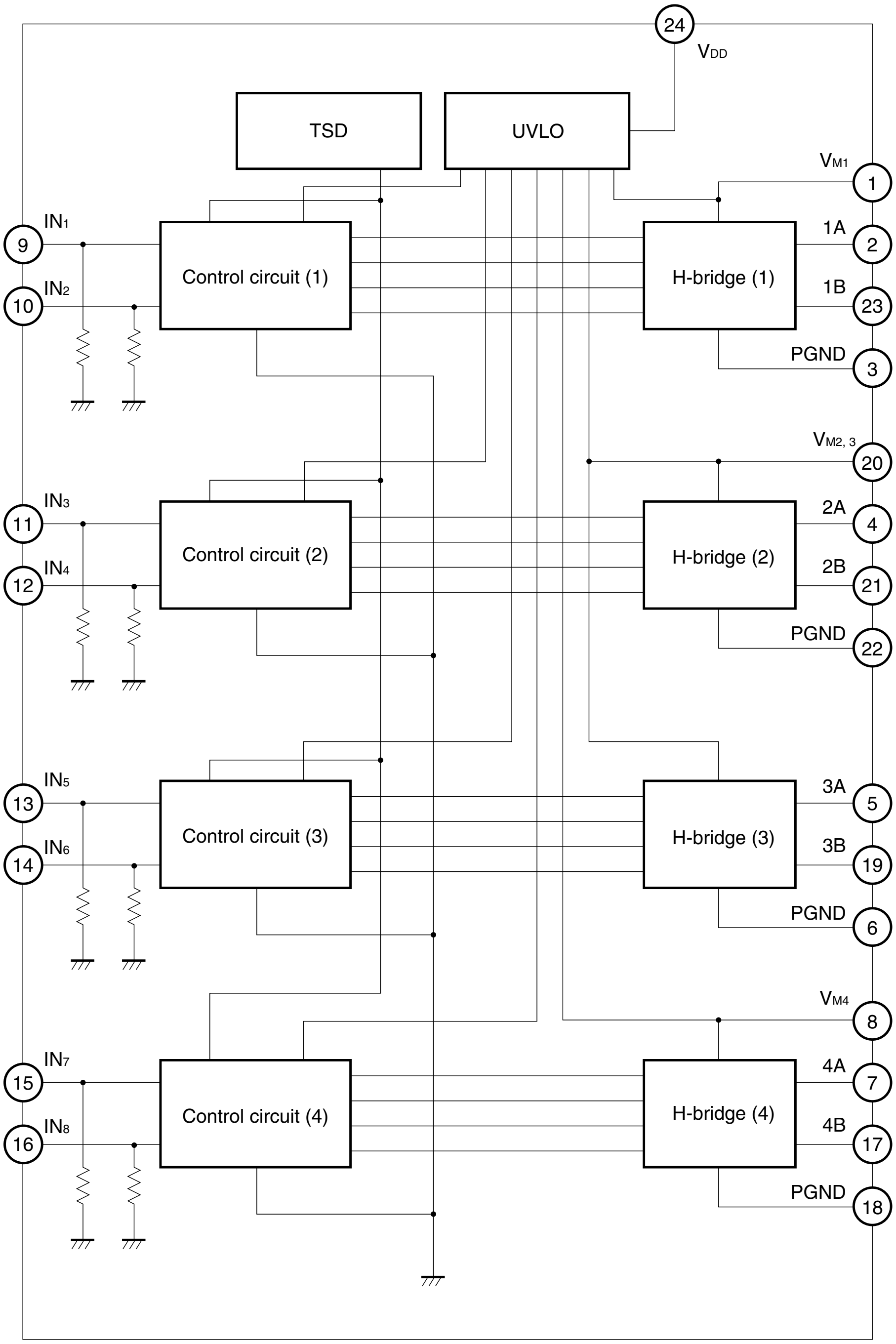
When all control pin is low-level, IC becomes stand-by state and current consumption is reduced.

## PIN CONNECTION




| Pin No. | Pin name | Pin function |
|---|---|---|
| 1 | $V_{M1}$ | Output block supply voltage input terminal |
| 2 | OUT1A | Output terminal |
| 3 | PGND | Ground terminal |
| 4 | OUT2A | Output terminal |
| 5 | OUT3A | Output terminal |
| 6 | PGND | Ground terminal |
| 7 | OUT4A | Output terminal |
| 8 | $V_{M4}$ | Output block supply voltage input terminal |
| 9 | IN1 | Control terminal (channel 1) |
| 10 | IN2 | Control terminal (channel 1) |
| 11 | IN3 | Control terminal (channel 2) |
| 12 | IN4 | Control terminal (channel 2) |
| 13 | IN5 | Control terminal (channel 3) |
| 14 | IN6 | Control terminal (channel 3) |
| 15 | IN7 | Control terminal (channel 4) |
| 16 | IN8 | Control terminal (channel 4) |
| 17 | OUT4B | Output terminal |
| 18 | PGND | Ground terminal |
| 19 | OUT3B | Output terminal |
| 20 | $V_{M23}$ | Output block supply voltage input terminal |
| 21 | OUT2B | Output terminal |
| 22 | PGND | Ground terminal |
| 23 | OUT1B | Output terminal |
| 24 | $V_{DD}$ | Control block supply voltage input terminal |

## BLOCK DIAGRAM




**Cautions 1. The terminal which has more than one should connect not only one terminal but all terminals.**

**2. Pull down resistance is connected to the input terminal. It's not necessary that the input terminal is connected when it isn't used.**

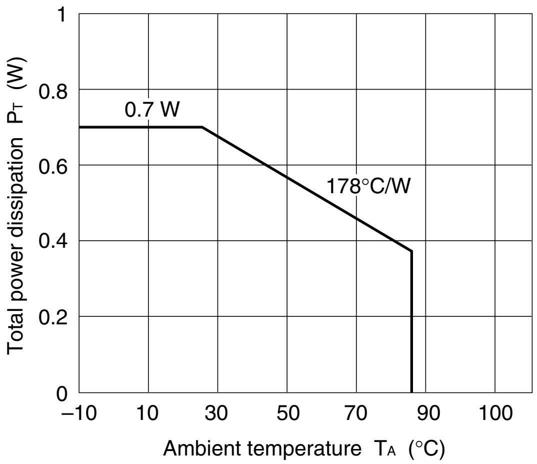
**3. The motor part power supply terminals $V_{M1}$, $V_{M23}$, and $V_{M4}$ are separated inside, and can impress an individually different power supply.**

**4. The motor part power supply terminal of the output which is not used should impress voltage of recommended operation condition, or should connect to GND.**

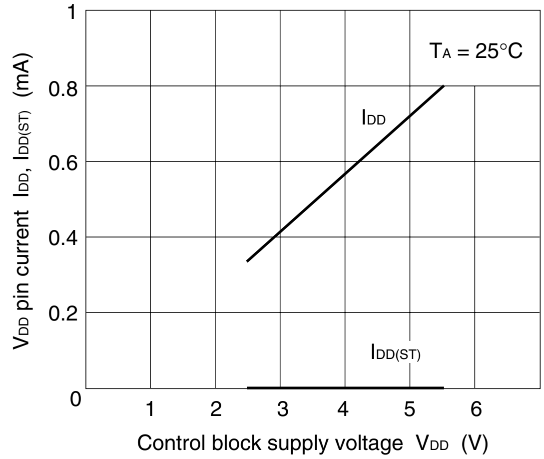
**In addition, if voltage is impressed to $V_M$ terminal even when an input is open, $V_M$ terminal current (10 μAMAX) is flow at the time of standby.**

## TYPICAL CHARACTERISTICS

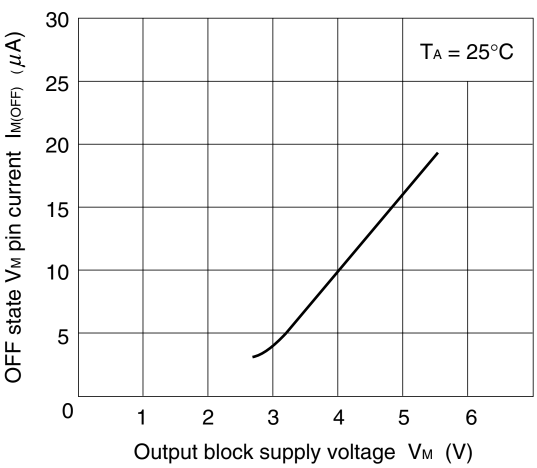
PT vs. TA characteristics



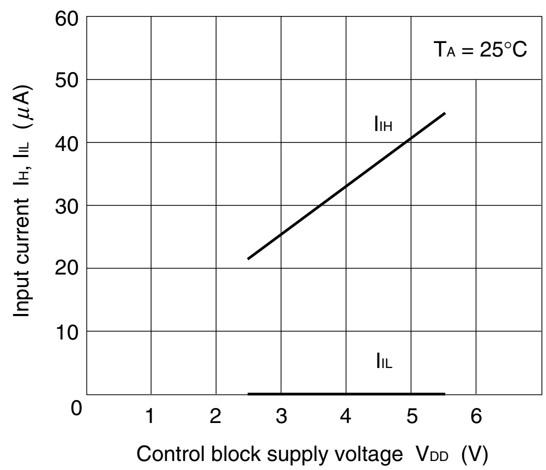

IDD, IDD(ST) vs. VDD characteristics



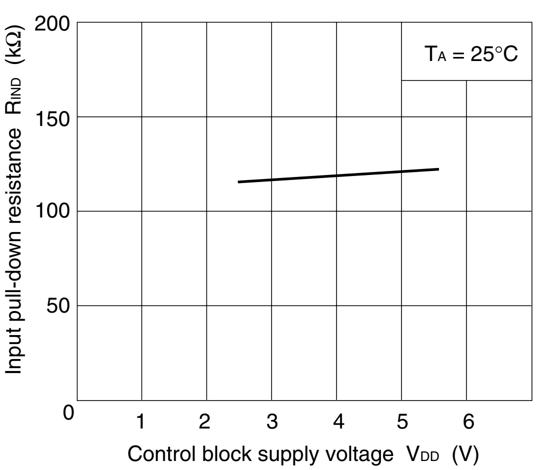

IM vs. VM characteristics



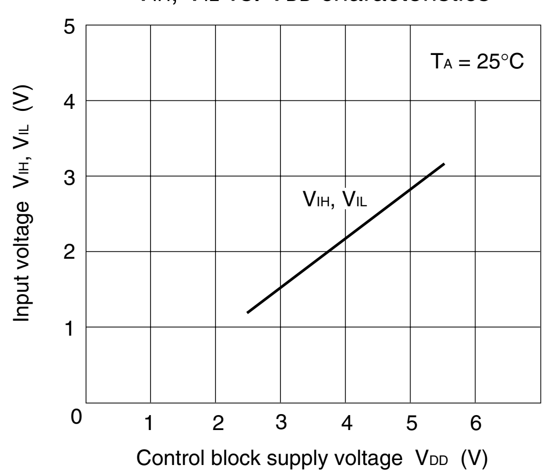

IIH, IIL vs. VDD characteristics



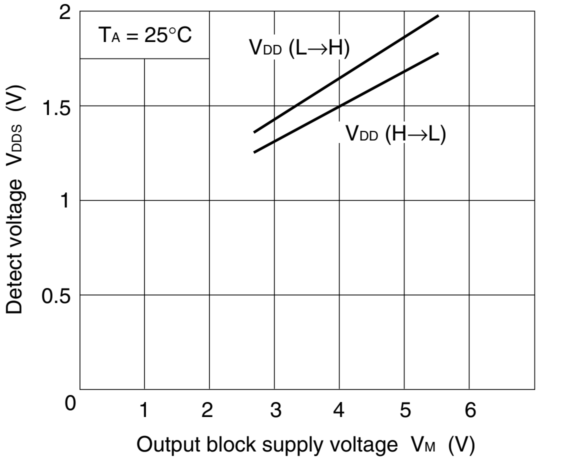

RIND vs. VDD characteristics



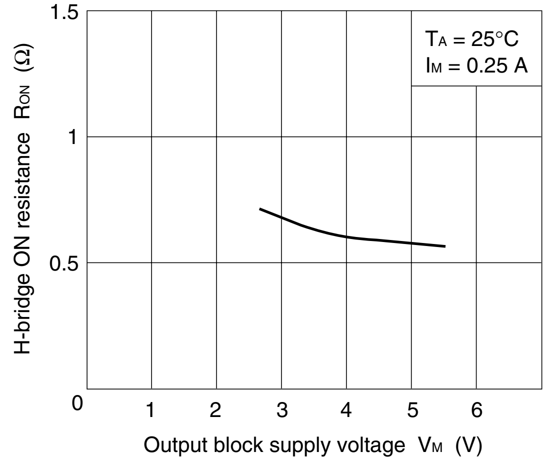

VIH, VIL vs. VDD characteristics



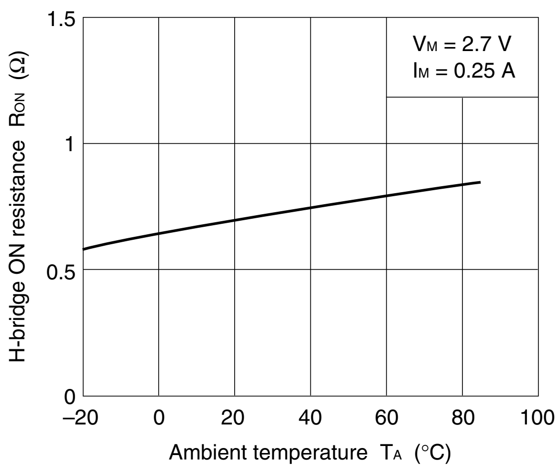
Detect voltage at low voltage characteristics



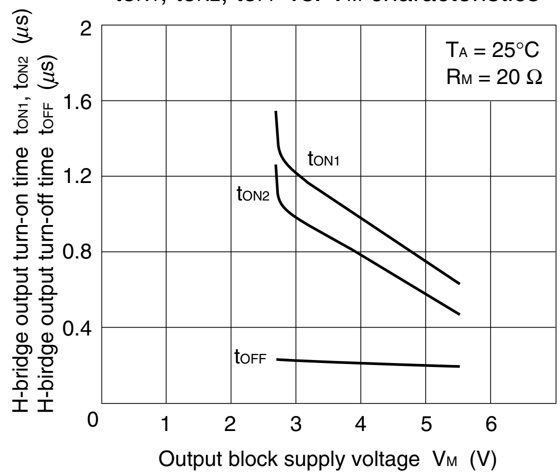

$R_{ON}$ vs. $V_M$ characteristics



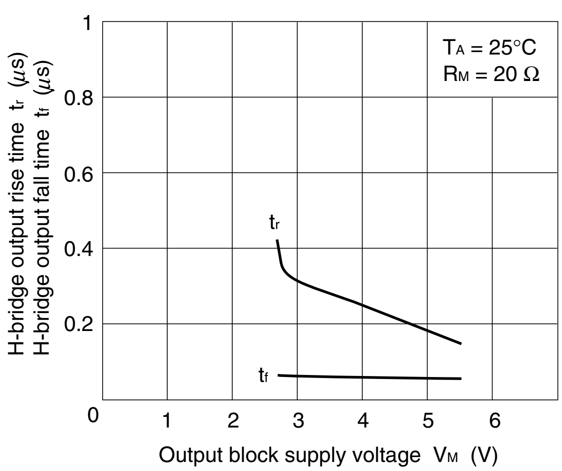

$R_{ON}$ vs. $T_A$ characteristics



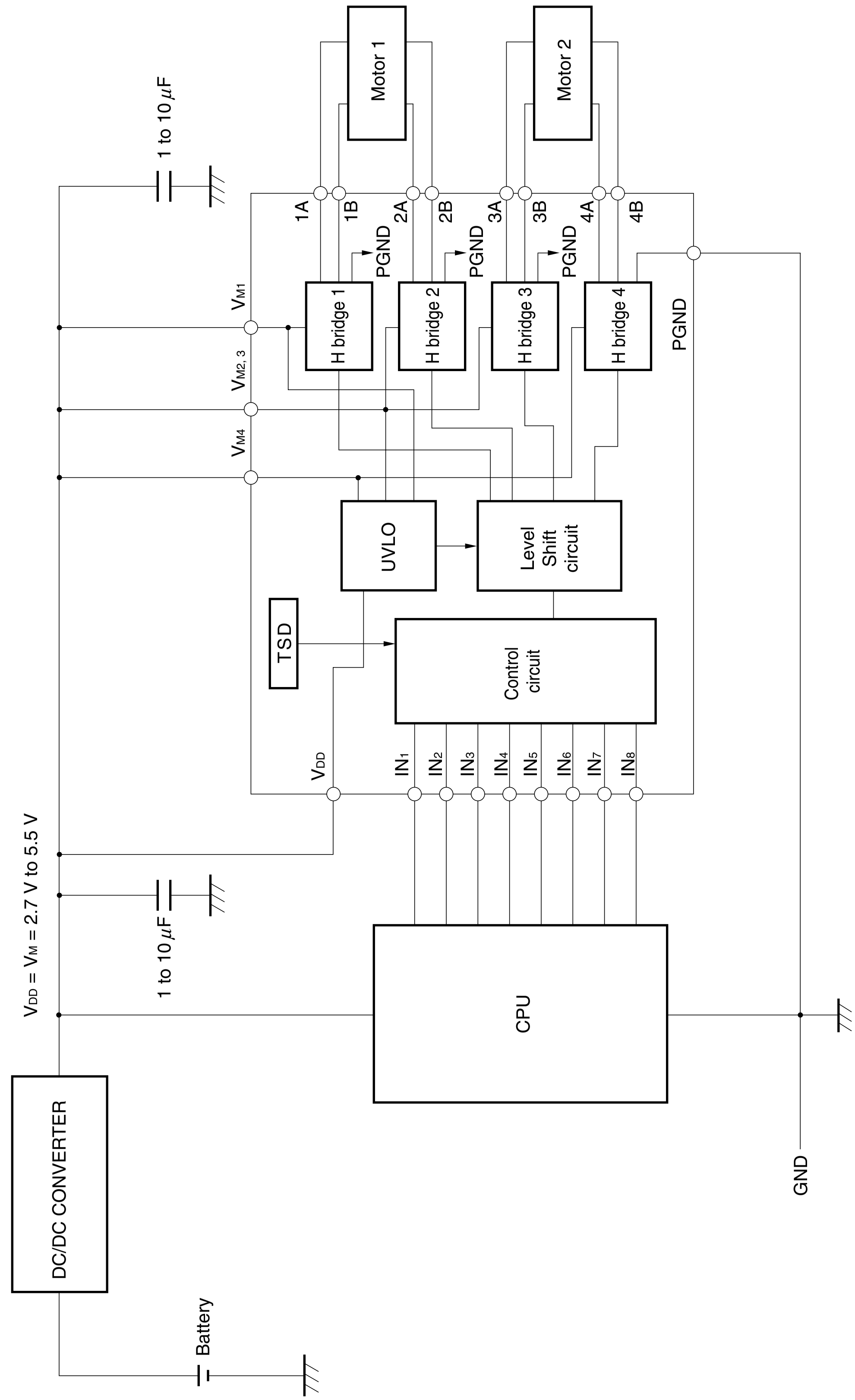

$t_{ON1}$, $t_{ON2}$, $t_{OFF}$ vs. $V_M$ characteristics




$t_r$, $t_f$ vs. $V_M$ characteristics



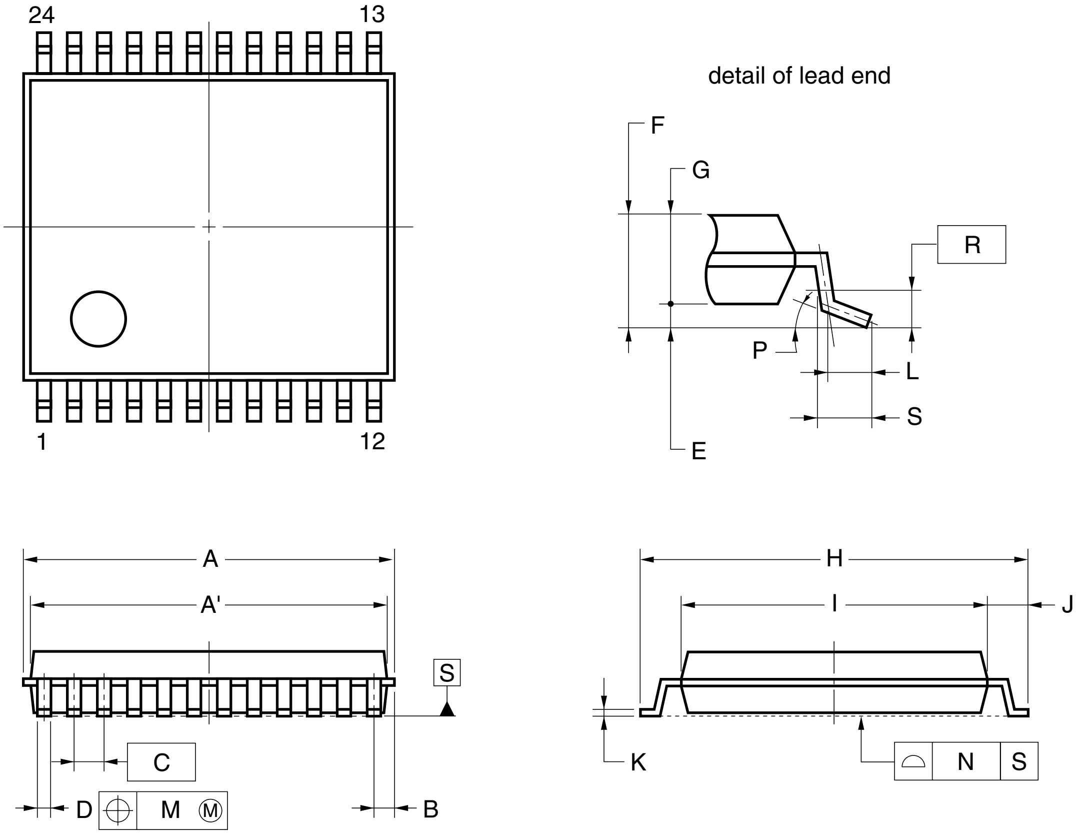
**STANDARD CONNECTION EXAMPLE**




This circuit diagram is an example of connection, and is not a thing aiming at mass production.

## PACKAGE DIMENSION

## 24-PIN PLASTIC TSSOP (5.72 mm (225))




**NOTE**

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 6.65±0.10 |
| A' | 6.5±0.1 |
| B | 0.575 |
| C | 0.5 (T.P.) |
| D | 0.22±0.05 |
| E | 0.1±0.05 |
| F | 1.2 MAX. |
| G | 1.0±0.05 |
| H | 6.4±0.1 |
| I | 4.4±0.1 |
| J | 1.0±0.1 |
| K | 0.17±0.025 |
| L | 0.5 |
| M | 0.10 |
| N | 0.08 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| R | 0.25 |
| S | 0.6±0.15 |

**P24MA-50-6A5**

## RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.
For soldering methods and conditions other than those recommended, consult NEC.

For details of the recommended soldering conditions, refer to information document **“Semiconductor Device Mounting Technology Manual”**.

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C; Time: 30 secs. max. (210°C min.);<br>Number of times: 3 times max; Number of day: none;<br>Flux: Rosin-based flux with little chlorine content (chlorine: 0.2Wt% max.) is recommended. | IR35-00-3 |
| VPS | Package peak temperature: 215°C; Time: 40 secs. max. (200°C min.);<br>Number of times: 3 times max.; Number of day: none;<br>Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt% max.) is recommended. | VP15-00-3 |
| Wave soldering | Package peak temperature: 260°C; Time: 10 secs. max.;<br>Preheating temperature: 120°C max.; Number of times: once;<br>Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt% max.) is recommended. | WS60-00-1 |

**Caution Do not use two or more soldering methods in combination.**

[MEMO]

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

# Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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