UT54ACS164245S

RadHard Schmitt CMOS 16-bit Bidirectional MultiPurpose Transceiver
Datasheet

January 17, 2001

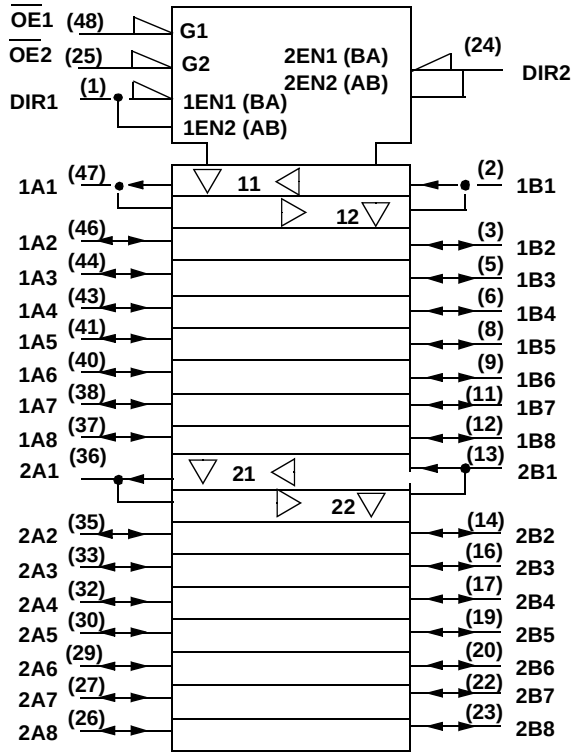
FEATURES

- Voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus
- Cold sparing
  - 1MΩ minimum input impedance power-off
- 0.6µm Commercial RadHard™ CMOS
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune
- High speed, low power consumption
- Schmitt trigger inputs to filter noisy signals
- Available QML Q or V processes
- Standard Microcircuit Drawing 5962-98580
- Package:
  - 48-lead flatpack, 25 mil pitch (.390 x .640)

DESCRIPTION

The 16-bit wide UT54ACS164245S MultiPurpose transceiver is built using UTMC's Commercial RadHard™ epitaxial CMOS technology and is ideal for space applications. This high speed, low power UT54ACS164245S transceiver is designed to perform multiple functions including: asynchronous two-way communication, signal buffering, voltage translation, and cold sparing. With V_{DD} equal to zero volts, the UT54ACS164245S outputs and inputs present a minimum impedance of 1MΩ making it ideal for "cold spare" applications. Balanced outputs and low "on" output impedance make the UT54ACS164245S well suited for driving high capacitance loads and low impedance backplanes. The UT54ACS164245S enables system designers to interface 3.3 volt CMOS compatible components with 5 volt CMOS components. For voltage translation, the A port interfaces with the 3.3 volt bus; the B port interfaces with the 5 volt bus. The direction control (DIRx) controls the direction of data flow. The output enable ($\overline{OE}$x) overrides the direction control and disables both ports. These signals can be driven from either port A or B. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver.

LOGIC SYMBOL



PIN DESCRIPTION

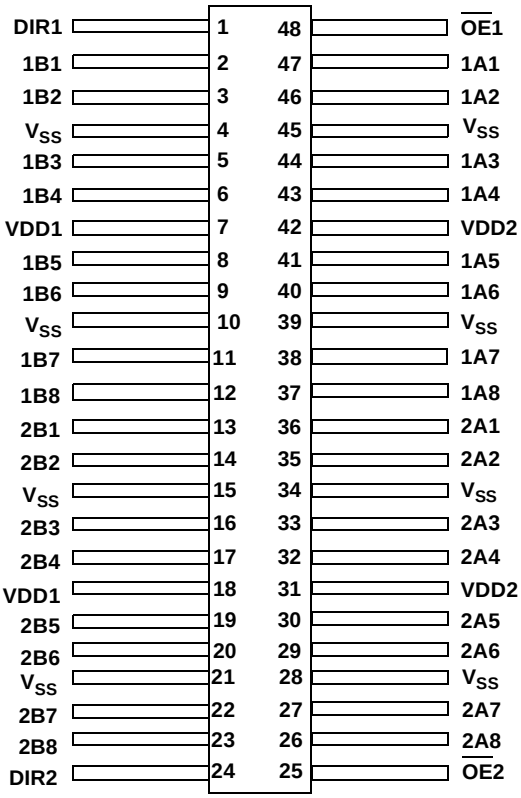
Pin Names	Description
$\overline{OE}$x	Output Enable Input (Active Low)
DIRx	Direction Control Inputs
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

FUNCTION TABLE

ENABLE $\overline{OE}$x	DIRECTION DIRx	OPERATION
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation

PINOUTS

48-Lead Flatpack
Top View



POWER TABLE[1]

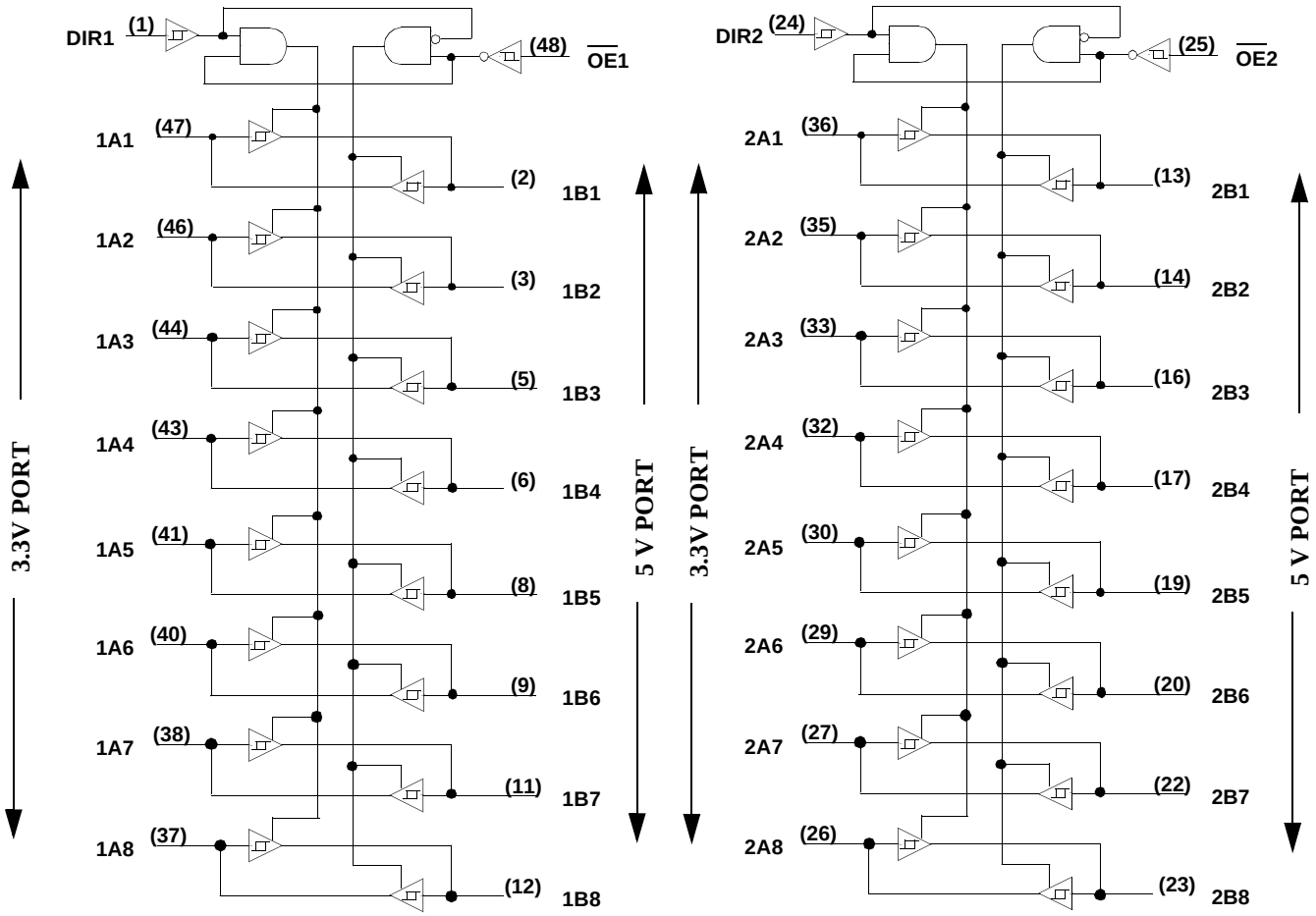
Port B	Port A	OPERATION
5 Volts	3.3 Volts	Voltage Translator
5 Volts	5 Volts	Non Translating
3.3 Volts	3.3 Volts	Non Translating
V_{SS}	V_{SS}	Cold Spare
V_{SS}	3.3V or 5V	Port B Cold Spare

NOTE:

1. V_{DD2} cannot be tied to V_{SS} while power is applied to V_{DD1}.

Control signals DIRx and $\overline{OEx}$ are 5 volt tolerant inputs. When V_{DD2} is at 3.3 volts, either 3.3 or 5 volt CMOS logic levels can be applied to all control inputs. For proper operation connect power to all V_{DD} and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} input pins). If V_{DD1} and V_{DD2} are not powered up together, then V_{DD2} should be powered up first for proper control of $\overline{OE}$ and $\overline{DIR}$. Until V_{DD2} reaches 2.75V $\pm$ 5%, control of the outputs by $\overline{OE}$ and DIR cannot be guaranteed. Tie unused inputs to V_{SS}. Always insure $V_{DD1} \geq V_{DD2}$ during operation of the part.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rad(Si)
SEL Latchup	>120	MeV-cm^2/mg
Neutron Fluence[2]	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent of CMOS technology.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
$V_{I/O}$	Voltage any pin	-.3 to V_{DD1} +.3	V
V_{DD1}	Supply voltage	-0.3 to 6.0	V
V_{DD2}	Supply voltage	-0.3 to 6.0	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

DUAL SUPPLY OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD1}	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{DD2}	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD1}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS [1]
(-55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_T+	Schmitt Trigger, positive going threshold[2]	V_{DD} from 3.00 to 5.5		.7V_{DD}	V
V_T-	Schmitt Trigger, negative going threshold[2]	V_{DD} from 3.00 to 5.5	.3V_{DD}		V
V_{H1}	Schmitt Trigger range of hysteresis[10]	V_{DD} from 4.5 to 5.5	0.6		V
V_{H2}	Schmitt Trigger range of hysteresis[10]	V_{DD} from 3.00 to 3.6	0.4		V
I_{IN}	Input leakage current[10]	V_{DD} from 3.6 to 5.5 V_{IN} = V_{DD} or V_{SS}	-1	3	µA
I_{OZ}	Three-state output leakage current[10]	V_{DD} from 3.6 to 5.5 V_{IN} = V_{DD} or V_{SS}	-1	3	µA
I_{CS}	Cold sparing leakage current[3]	V_{IN} = 5.5 V_{DD} = V_{SS}	-1	5	µA
I_{OS1}	Short-circuit output current [6, 11]	V_O = V_{DD} or V_{SS} V_{DD} from 4.5 to 5.5	-200	200	mA
I_{OS2}	Short-circuit output current [6, 11]	V_O = V_{DD} or V_{SS} V_{DD} from 3.00 to 3.6	-100	100	mA
V_{OL1}	Low-level output voltage[4, 10]	I_{OL}= 8mA I_{OL}= 100µA V_{DD} = 4.5		0.4 0.2	V
V_{OL2}	Low-level output voltage[4, 10]	I_{OL}= 8mA I_{OL}= 100µA V_{DD} = 3.00		0.5 0.2	V
V_{OH1}	High-level output voltage[4, 10]	I_{OH}= -8mA I_{OH}= -100µA V_{DD} = 4.5	V_{DD} - 0.7 V_{DD} - 0.2		V
V_{OH2}	High-level output voltage[4, 10]	I_{OH}= -8mA I_{OH}= -100µA V_{DD} = 3.00	V_{DD} - 0.9 V_{DD} - 0.2		V

P_{total1}	Power dissipation [5,7, 8]	C_L = 50pF V_{DD} from 4.5 to 5.5		2.0	mW/ MHz
P_{total2}	Power dissipation [5, 7, 8]	C_L = 50pF V_{DD} from 3.00 to 3.6		1.5	mW/ MHz
I_{DD}	Standby Supply Current V_{DD1} or V_{DD2} Pre-Rad 25°C Pre-Rad -55°C to +125°C Post-Rad 25°C	V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5 $\overline{OE}$=V_{DD} $\overline{OE}$=V_{DD} $\overline{OE}$=V_{DD}		 10 100 500	 µA µA µA
C_{IN}	Input capacitance [9]	*f* = 1MHz @ 0V V_{DD} from 3.00 to 5.5		15	pF
C_{OUT}	Output capacitance[9]	*f* = 1MHz @ 0V V_{DD} from 3.00 to 5.5		15	pF

Notes:

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
3. All combinations of $\overline{OE}$x and DIRx
4. Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
5. Guaranteed by characterization.
6. Not more than one output may be shorted at a time for maximum duration of one second.
7. Power does not include power contribution of any CMOS output sink current.
8. Power dissipation specified per switching output.
9. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
10. Guaranteed; tested on a sample of pins per device.
11. Supplied as a design limit, but not guaranteed or tested.

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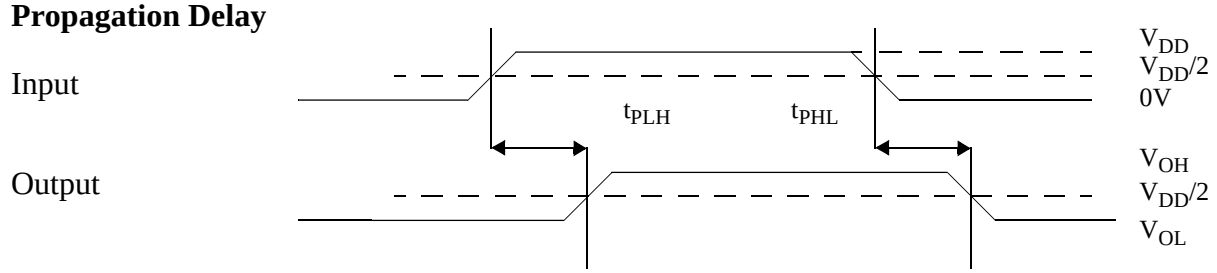
AC ELECTRICAL CHARACTERISTICS[1] (Port B = 5 Volt, Port A = 3.3 Volt)

(V_{DD1} = 5V ±10%; V_{DD2} = 3.00V to 3.6V, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	1	20	ns
t_{PHL}	Propagation delay Data to Bus	1	20	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	1	18	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	1	18	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	20	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	20	ns
t_{PZL}[2]	Output enable time DIRx to Bus	1	18	ns
t_{PZH}[2]	Output enable time DIRx to Bus	1	18	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	1	20	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance	1	20	ns

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested.

Propagation Delay



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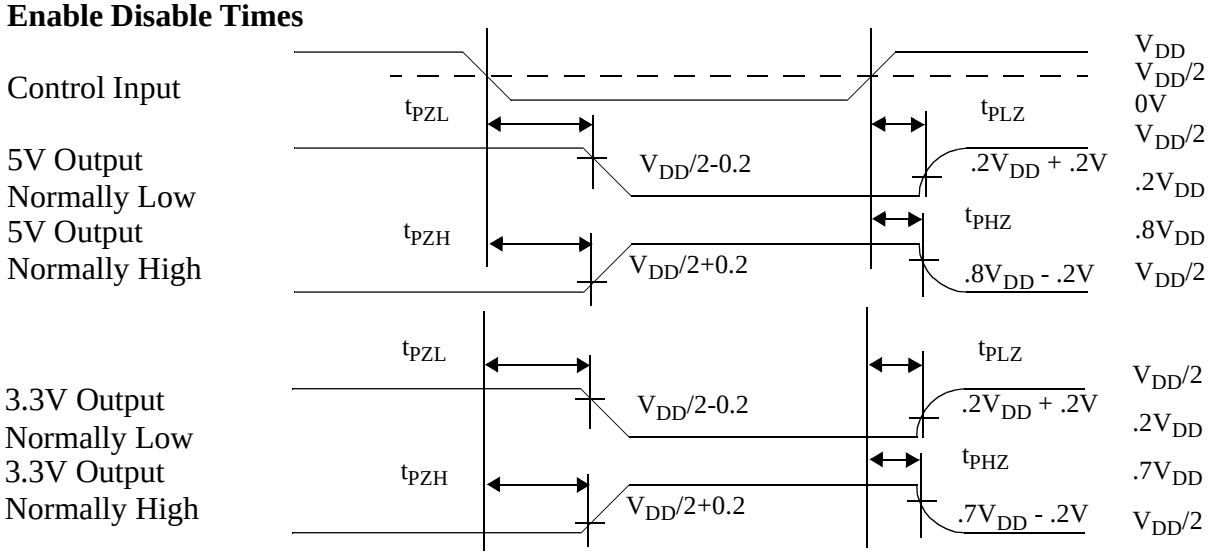


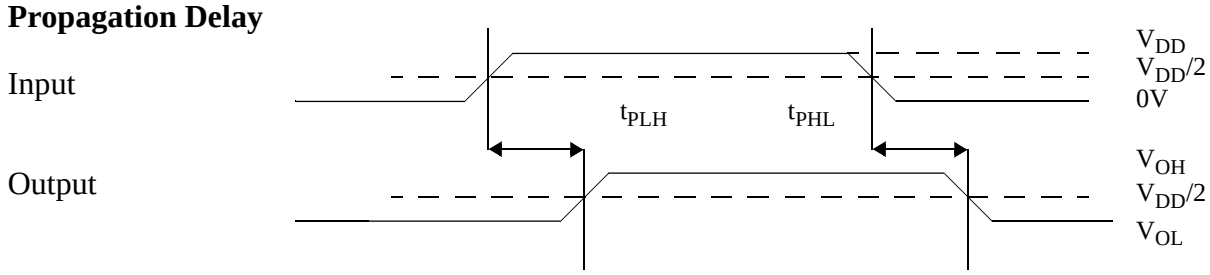
AC ELECTRICAL CHARACTERISTICS[1] (Port A = Port B, 5 Volt Operation)

(V_{DD1} = 5V ±10%; V_{DD2} = 5.0V ±10%, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	1	15	ns
t_{PHL}	Propagation delay Data to Bus	1	15	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	1	12	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	1	12	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	15	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	15	ns
t_{PZL}[2]	Output enable time DIRx to Bus	1	12	ns
t_{PZH}[2]	Output enable time DIRx to Bus	1	12	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	1	15	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance	1	15	ns

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested

Propagation Delay



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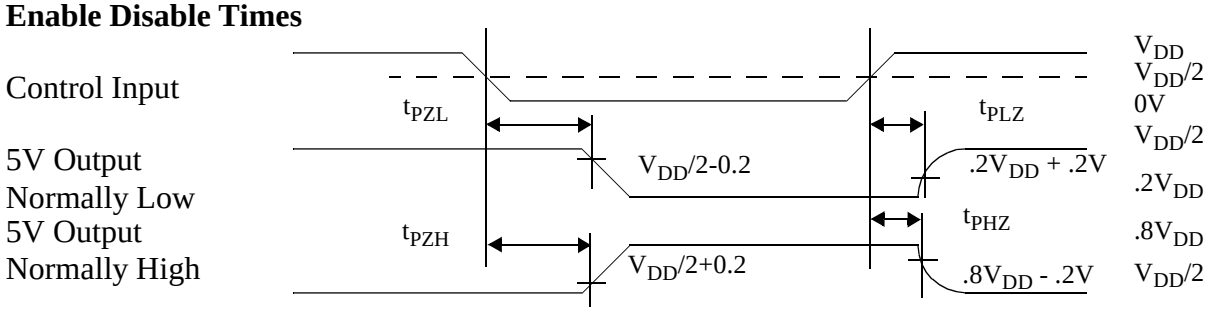


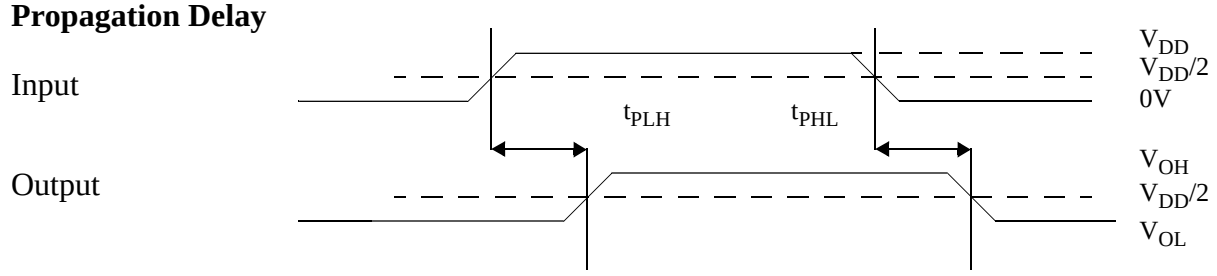
AC ELECTRICAL CHARACTERISTICS[1] (Port A = Port B, 3.3 Volt Operation)
(V_{DD1} = 3.00V to 3.6V; V_{DD2} = 3.00V to 3.6V, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	1	20	ns
t_{PHL}	Propagation delay Data to Bus	1	20	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	1	18	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	1	18	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	20	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	20	ns
t_{PZL}[2]	Output enable time DIRx to Bus	1	18	ns
t_{PZH}[2]	Output enable time DIRx to Bus	1	18	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	1	20	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance	1	20	ns

Notes:

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. OEx to bus times are tested.

Propagation Delay



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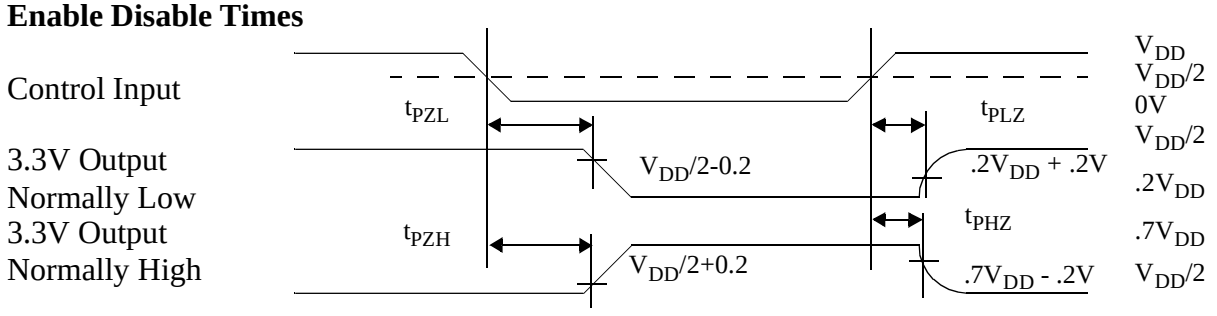
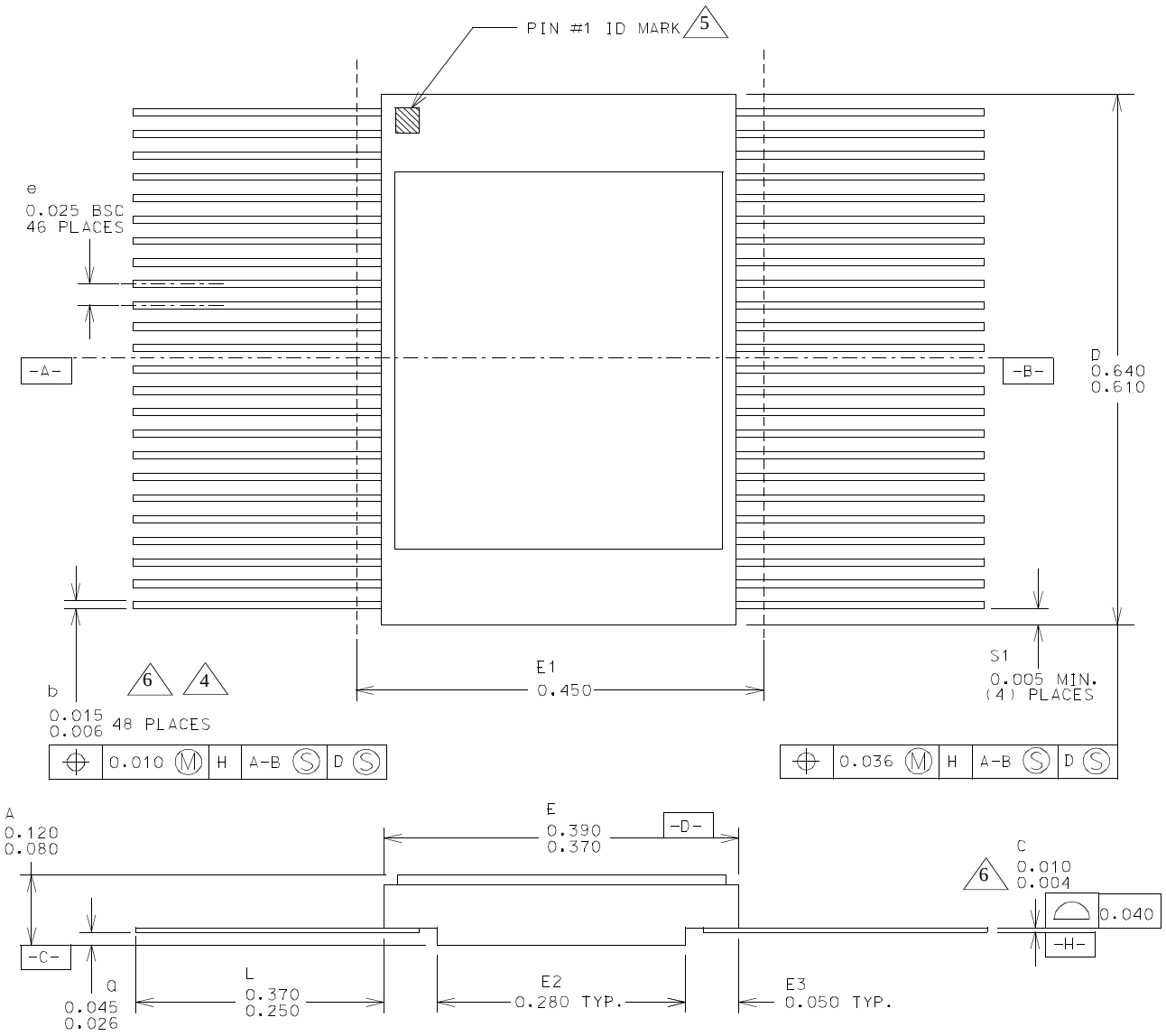


PACKAGE

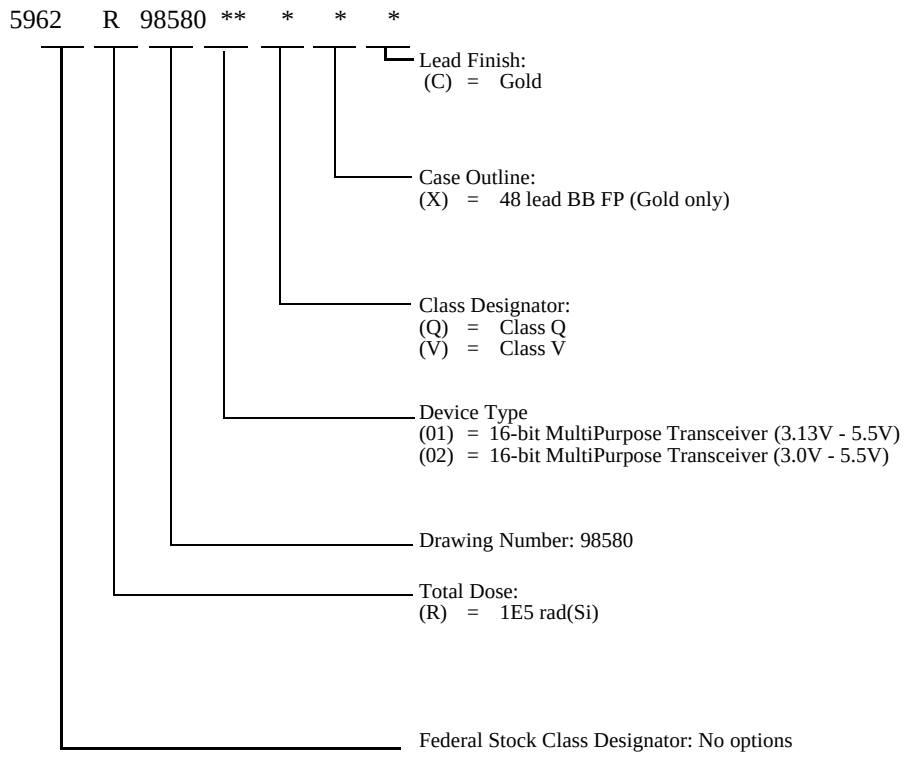


1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Lead position and colanarity are not measured.
5. ID mark symbol is vendor option.
6. With solder, increase maximum by 0.003.

Figure 1. 48-Lead Flatpack

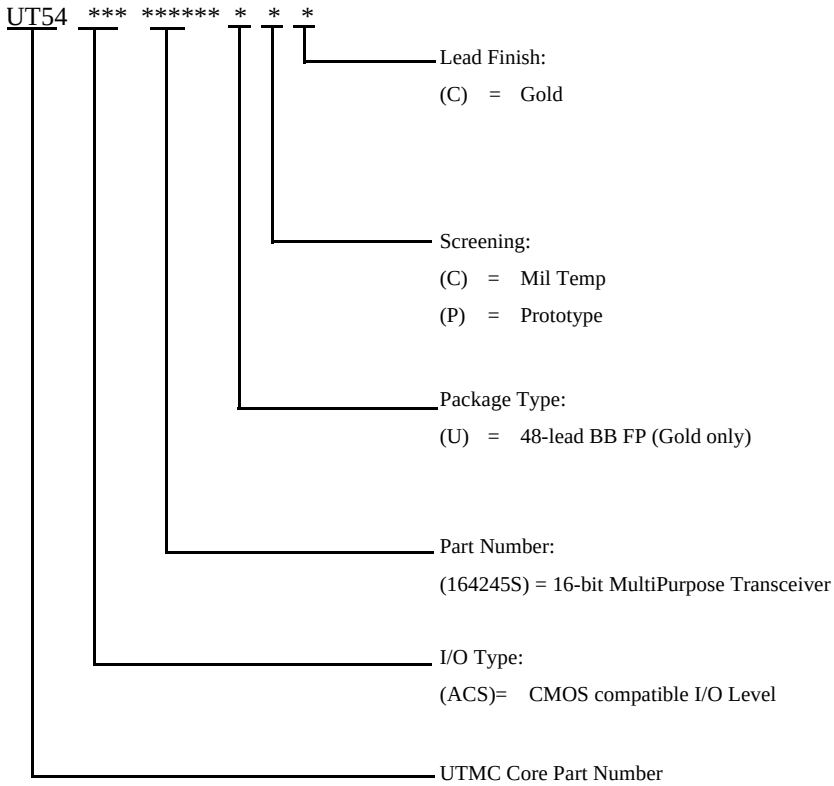
ORDERING INFORMATION

UT54ACS164245S: SMD



Notes:
1. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

UT54ACS164245S



Notes:
1. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested -55C, room temp, and 125C. Radiation neither tested nor guaranteed.
2. Prototype flow per UTMC Manufacturing Flows Document Tested at 25C only. Lead finish is gold only.