Dual D-type flip-flop

54F74

DESCRIPTION

The 54F74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs, and complimentary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

See 54F5074 for metastable immune version.

DESCRIPTION	ORDER CODE	PACKAGE DESCRIPTION*
14-Pin Ceramic DIP	54F74/BCA	GDIP1-T14
14-Pin Ceramic FlatPack	54F74/BDA	GDFP-T14
20-Pin Ceramic LLCC	54F74/B2A	CQCC2-N20

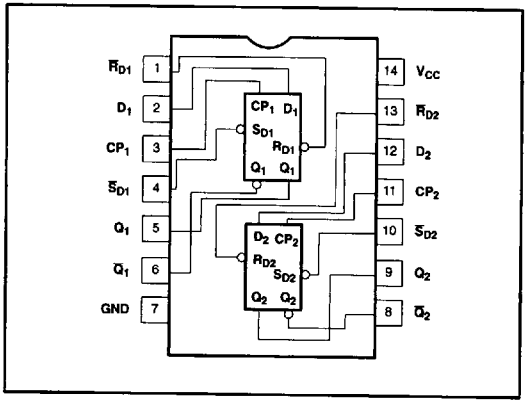
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

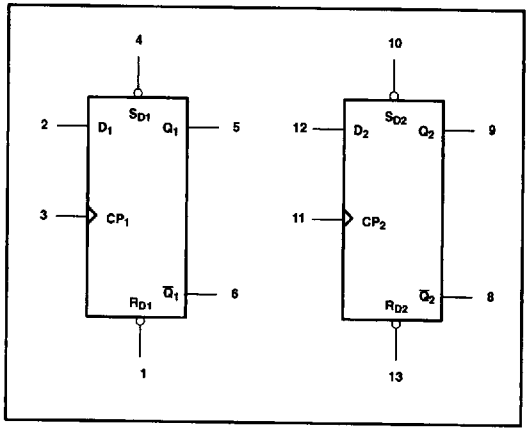
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_1, D_2	Data inputs	1.0/1.0	20µA/0.6mA
CP_1, CP_2	Clock pulse inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset inputs (active Low)	1.0/3.0	20µA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set inputs (active Low)	1.0/3.0	20µA/1.8mA
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) Fast Unit Load (U.I.) is Defined As: 20µA in the High state and 6.0mA in the Low state.

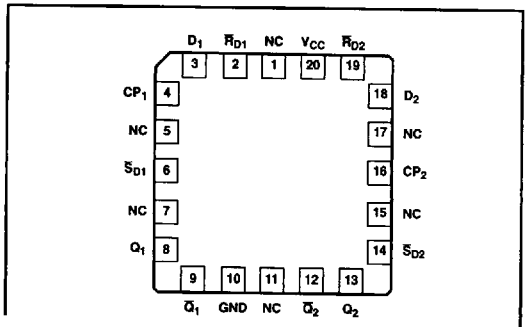
PIN CONFIGURATION



LOGIC SYMBOL



LLCC LEAD CONFIGURATION



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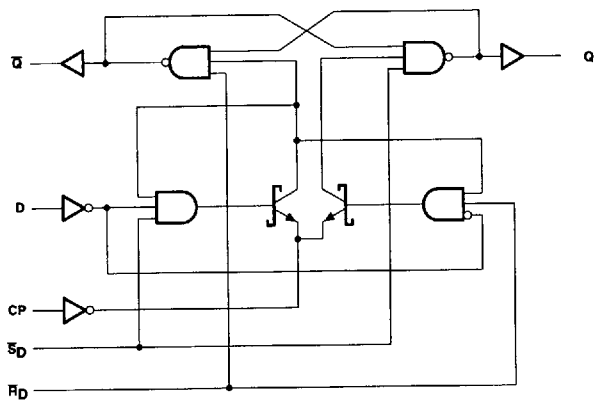
LOGIC DIAGRAM



MODE SELECT – FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined[1]	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

NOTE:
1. Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5 0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			5	100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	All inputs		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	D, CP inputs		-0.4	-0.6	mA
			$\overline{R}_D$, $\overline{S}_D$ inputs		-1.3	-1.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V		-60	-85	-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			11.5	16	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = 25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55 TO +125°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	6.8 8.0	3.5 3.7	8.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}_n$ or $\overline{RD}_n$ to Q_n, $\overline{Q}_n$	Waveform 2	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	8.0 11.5	ns ns

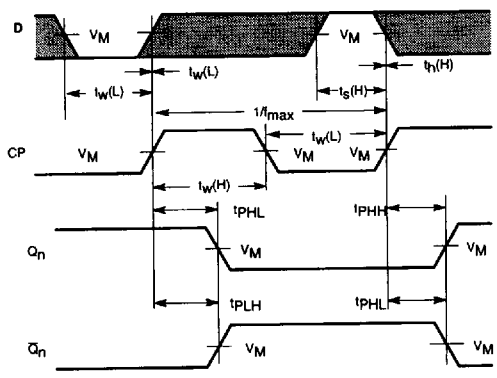
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V and T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not tested.

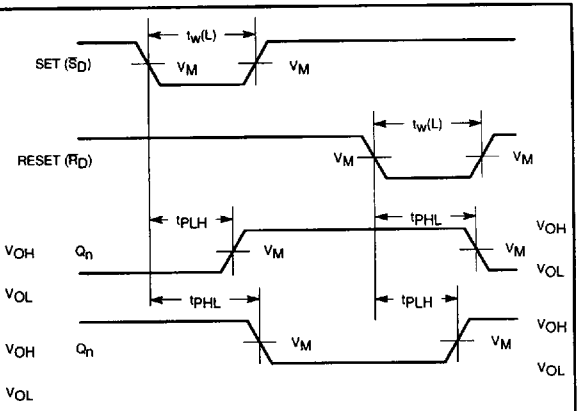
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = 25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = -55$ TO $+125°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup time High or Low D_n to CP	Waveform 1.	2.0 3.0			3.0 4.0		ns ns
$t_H(H)$ $t_H(L)$	Hold time High or Low D_n to CP	Waveform 4.	1.0 1.0			2.0 2.0		ns ns
$t_W(H)$ $t_W(L)$	Clock pulse width High or Low	Waveform 1.	4.0 5.0			4.0 6.0		ns ns
$t_W(L)$	$\overline{R}_D$ or $\overline{S}_D$ pulse width, Low	Waveform 2.	4.0			4.0		ns
t_{rec}	Recovery time, $\overline{R}_D$ or $\overline{S}_D$ to CP	Waveform 3.	2.0			3.0		ns

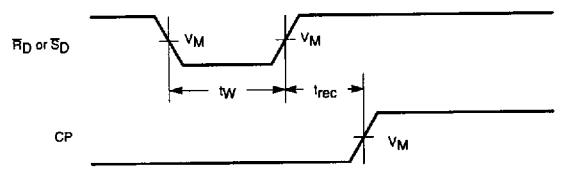
AC WAVEFORMS



Waveform 1.. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



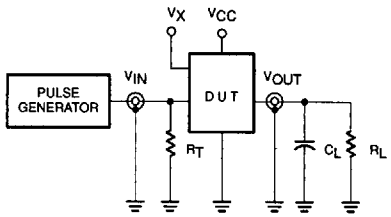
Waveform 2.. Set and Reset to Output Delays, Set and Reset Pulse Widths



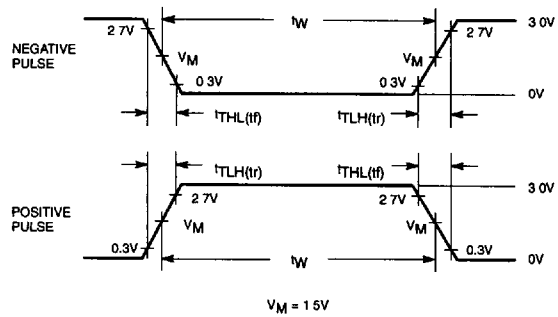
Waveform 3.. Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable performance

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns