

REVISIONS													
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED										

REV	1	2	3	4	5	6	7	8	9	10	11	12	13	14
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REV	1	2	3	4	5	6	7	8	9	10	11	12	13	14
SHEET														
REV STATUS OF SHEETS	REV													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13

PMIC N/A  <b>STANDARDIZED MILITARY DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	PREPARED BY <i>Jeffery J. Sinstall</i> CHECKED BY <i>[Signature]</i> APPROVED BY <i>[Signature]</i> DRAWING APPROVAL DATE 1 FEBRUARY 1989 REVISION LEVEL	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444  MICROCIRCUIT, DIGITAL, FAST CMOS 9-BIT NON-INVERTING BUS TRANSCEIVER, MONOLITHIC SILICON  <table style="width: 100%;"> <tr> <td style="width: 15%;">SIZE</td> <td style="width: 35%;">CAGE CODE</td> <td style="width: 50%;"></td> </tr> <tr> <td style="text-align: center;"><b>A</b></td> <td style="text-align: center;"><b>67268</b></td> <td style="text-align: center;"><b>5962-88661</b></td> </tr> <tr> <td style="text-align: center;">SHEET</td> <td style="text-align: center;">1</td> <td style="text-align: center;">OF 14</td> </tr> </table>	SIZE	CAGE CODE		<b>A</b>	<b>67268</b>	<b>5962-88661</b>	SHEET	1	OF 14
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<b>A</b>	<b>67268</b>	<b>5962-88661</b>									
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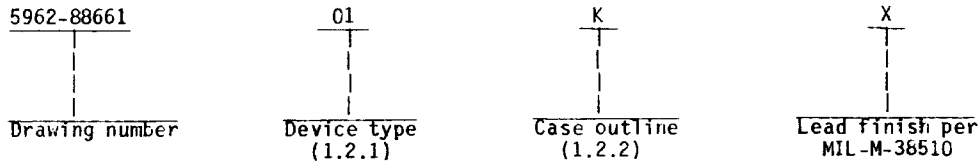
5962-E919

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT863A	9-bit non-inverting bus transceiver
02	54FCT863B	9-bit non-inverting bus transceiver

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage - - - - -	-0.5 V dc to +7.0 V dc
Input voltage range - - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
Output voltage range - - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC input diode current ( $I_{IK}$ ) - - - - -	-20 mA
DC output diode current ( $I_{OK}$ ) - - - - -	-50 mA
DC output current - - - - -	+100 mA
Maximum power dissipation ( $P_D$ ) 2/ - - - - -	500 mW
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) - - - - -	See MIL-M-38510, appendix C
Storage temperature range - - - - -	-65°C to +150°C
Junction temperature ( $T_J$ ) - - - - -	+175°C
Lead temperature (soldering, 10 seconds) - - - - -	+300°C

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ) - - - - -	+4.5 V dc to +5.5 V dc
Maximum low level input voltage ( $V_{IL}$ ) - - - - -	0.8 V dc
Minimum high level input voltage ( $V_{IH}$ ) - - - - -	2.0 V dc
Case operating temperature ( $T_C$ ) - - - - -	-55°C to +125°C

1/ All voltages referenced to GND.

2/ Must withstand the added  $P_D$  due to short circuit test; e.g.,  $I_{OS}$ .

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.0 V	I <sub>O</sub> = -300 μA	1, 2, 3	A11	4.3	V
			I <sub>O</sub> = -15 nA	1, 2, 3	A11	2.4	V
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 3.0 V, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.0 V	I <sub>O</sub> = 300 μA	1, 2, 3	A11		0.2 V
			I <sub>O</sub> = 32 mA	1, 2, 3	A11		0.5 V
Input clamp voltage	V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA	1	A11		-1.2	V
High level input current	I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V	O <sub>ERn</sub> , O <sub>ETn</sub>	1, 2, 3	A11		5 μA
			R <sub>n</sub> , T <sub>n</sub>	1, 2, 3	A11		15 μA
Low level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND	O <sub>ERn</sub> , O <sub>ETn</sub>	1, 2, 3	A11		-5 μA
			R <sub>n</sub> , T <sub>n</sub>	1, 2, 3	A11		-15 μA
High impedance output current	I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V	1, 2, 3	A11		10	μA
	I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND	1, 2, 3	A11		-10	μA
Short circuit output current	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V      1/	1, 2, 3	A11	-75		nA
Quiescent power supply current (CMOS inputs)	I <sub>CCQ</sub>	V <sub>IN</sub> < 0.2 V or V <sub>IN</sub> > 5.3 V, V <sub>CC</sub> = 5.5 V, f <sub>I</sub> = 0 MHz	1, 2, 3	A11		1.5	nA
Quiescent power supply current (TTL inputs)	ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V 2/	1, 2, 3	A11		2.0	nA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic power supply current	I <sub>CCD</sub>	V <sub>CC</sub> = 5.5 V, $\overline{OER} = \overline{OET} = \text{GND}$ , V <sub>IN</sub> > 5.3 V or V <sub>IN</sub> ≤ 0.2 V, Outputs open, One bit toggling - 50% duty cycle	3/	A11		0.25	mA/ MHz
Total power supply current <u>4/</u>	I <sub>CC</sub>	V <sub>IN</sub> > 5.3 V or V <sub>IN</sub> < 0.2 V, V <sub>CC</sub> = 5.5 V, f <sub>I</sub> = 10 MHz, Outputs open, One bit toggling - 50% duty cycle	1, 2, 3	A11		4.0	mA
		V <sub>IN</sub> = 3.4 V or V <sub>IN</sub> = GND, V <sub>CC</sub> = 5.5 V, f <sub>I</sub> = 10 MHz, Outputs open, One bit toggling - 50% duty cycle				5.0	mA
Functional tests		See 4.3. d	7, 8	A11			
Input capacitance	C <sub>IN</sub>	See 4.3.1c	4	A11		10	pF
Output capacitance	C <sub>OUT</sub>	See 4.3.1c	4	A11		12	μF
Propagation delay time, R <sub>n</sub> to T <sub>n</sub> or T <sub>n</sub> to R <sub>n</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	R <sub>L</sub> = 500Ω, See figure 3	C <sub>L</sub> = 50 pF	9,10,11	01	10	ns
					02	6.5	ns
			C <sub>L</sub> = 300 pF <u>5/</u>	9,10,11	01	17	ns
					02	14	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit		
						Min	Max			
Output enable time, OET <sub>n</sub> to T <sub>n</sub> or OER <sub>n</sub> to R <sub>n</sub>	tpZH, tpZL	R <sub>L</sub> = 500Ω, See figure 3	C <sub>L</sub> = 50 pF	9, 10, 11	01		17	ns		
						02		9.0	ns	
					01		5/	9, 10, 11		22
						02				16
Output disable time, OET <sub>n</sub> to T <sub>n</sub> or OER <sub>n</sub> to R <sub>n</sub>	tpZH, tpLZ	C <sub>L</sub> = 50 pF	9, 10, 11	01			10	ns		
					02		8.0	ns		
				01		5/	9, 10, 11		19	ns
					02				8.0	ns

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed 1 second.

2/ TTL driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

$$4/ I_{CC} = I_{CCQ} + (\Delta I_{CC} \times D_H \times N_T) + (I_{CCD} \times f_I \times N_I)$$

Where: D<sub>H</sub> = Duty cycle for TTL inputs high  
 N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>  
 f<sub>I</sub> = Input frequency in MHz  
 N<sub>I</sub> = Number of inputs at f<sub>I</sub>

5/ Parameter guaranteed, but not tested.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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Device types	All	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	$\overline{OER}_1$	NC
2	R <sub>0</sub>	$\overline{OER}_1$
3	R <sub>1</sub>	R <sub>0</sub>
4	R <sub>2</sub>	R <sub>1</sub>
5	R <sub>3</sub>	R <sub>2</sub>
6	R <sub>4</sub>	R <sub>3</sub>
7	R <sub>5</sub>	R <sub>4</sub>
8	R <sub>6</sub>	NC
9	R <sub>7</sub>	R <sub>5</sub>
10	R <sub>8</sub>	R <sub>6</sub>
11	$\overline{OER}_2$	R <sub>7</sub>
12	GND	R <sub>8</sub>
13	$\overline{DET}_1$	$\overline{OER}_2$
14	$\overline{DET}_2$	GND
15	T <sub>8</sub>	NC
16	T <sub>7</sub>	$\overline{DET}_1$
17	T <sub>6</sub>	$\overline{DET}_2$
18	T <sub>5</sub>	T <sub>8</sub>
19	T <sub>4</sub>	T <sub>7</sub>
20	T <sub>3</sub>	T <sub>6</sub>
21	T <sub>2</sub>	T <sub>5</sub>
22	T <sub>1</sub>	NC
23	T <sub>0</sub>	T <sub>4</sub>
24	V <sub>CC</sub>	T <sub>3</sub>
25	---	T <sub>2</sub>
26	---	T <sub>1</sub>
27	---	T <sub>0</sub>
28	---	V <sub>CC</sub>

FIGURE 1. Terminal connections.

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Inputs				Outputs		Function
OET <sub>n</sub>	OEF <sub>n</sub>	R <sub>n</sub>	T <sub>n</sub>	R <sub>n</sub>	T <sub>n</sub>	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High Z

H = High logic level  
 L = Low level logic  
 X = Don't care  
 Z = High impedance state  
 N/A = Not applicable

FIGURE 2. Truth table.

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Propagation delay

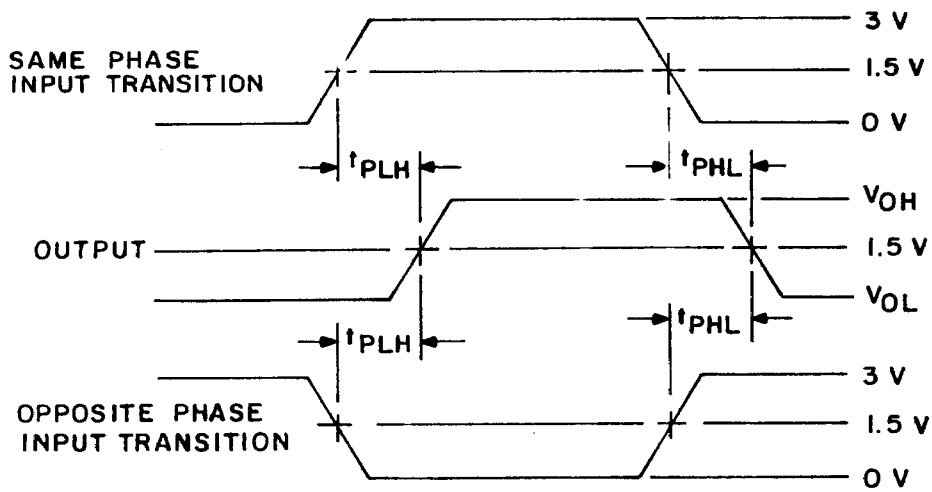


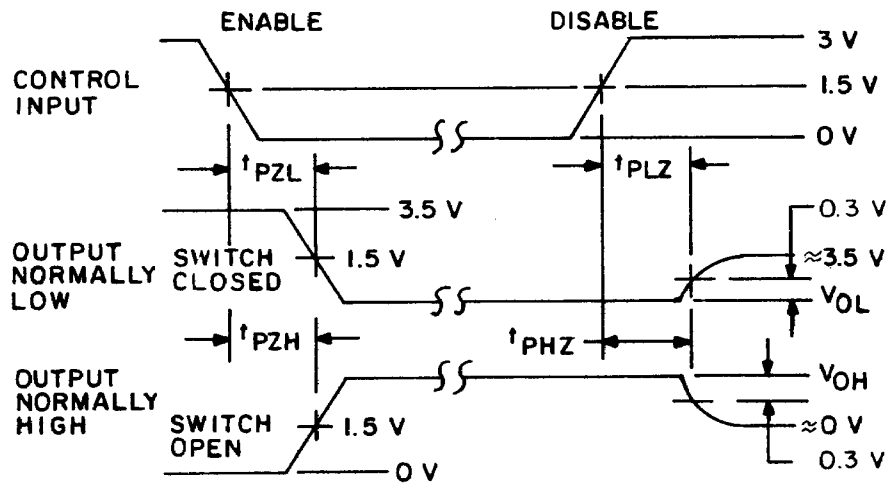
FIGURE 3. Switching waveforms and test circuit.

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Enable and disable times



NOTES:

1. Diagram shown for input control enable - low and input control disable - high.
2. Pulse generator for all pulses:  $t_f \leq 2.5$  ns,  $t_r \leq 2.5$  ns.

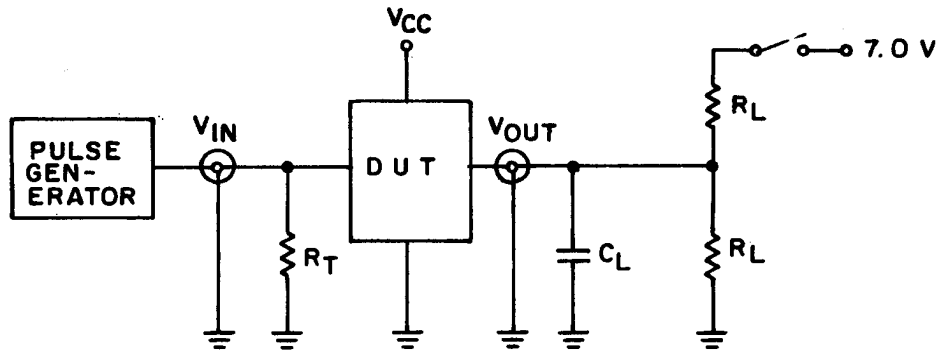
FIGURE 3. Switching waveforms and test circuit - Continued.

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Test circuits for three-state outputs



Switch position

Test	Switch
$t_{PLZ}$ $t_{PZL}$ All others	Closed Closed Open

Definitions:

- $R_L$  = Load resistor: See ac characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance:  
See ac characteristics for value.
- $R_T$  = Termination should be equal to  $Z_{OUT}$  of pulse generators.

FIGURE 3. Switching waveforms and test circuit - Continued.

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3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$  and  $C_{OUT}$  measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on five devices with zero failures.
- d. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test method 1005 of MIL-STD-883 conditions:
  - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,4,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

\* PDA applies to subgroup 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>	Replacement military specification part number
5962-8866101KX	61772	54FCT863AEB	---
5962-8866101LX	61772	54FCT863ADB	---
5962-88661013X	61772	54FCT863ALB	---
5962-8866102KX	61772	54FCT863BEB	---
5962-8866102LX	61772	54FCT863BDB	---
5962-88661023X	61772	54FCT863BLB	---

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

61772

Vendor name and address

Integrated Device Technology  
3236 Scott Boulevard  
Santa Clara, CA 95052

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