

16-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B
74ABTH16374B

FEATURES

- Two 8-bit positive edge triggered registers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State output buffers
- 74ABTH16373B incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16374B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16374B has two 8-bit, edge triggered registers, with each register coupled to eight 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (nOE) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable (nOE) controls all eight 3-State buffers for its register independent of the clock operation.

When nOE is Low, the stored data appears at the outputs for that register. When nOE is High, the outputs for that register are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

Two options are available, 74ABT16374B which does not have the bus-hold feature and 74ABTH16374B which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	2.6 2.2	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ} I_{CCL}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	μA
		Outputs Low; $V_{CC} = 5.5\text{V}$	8	mA

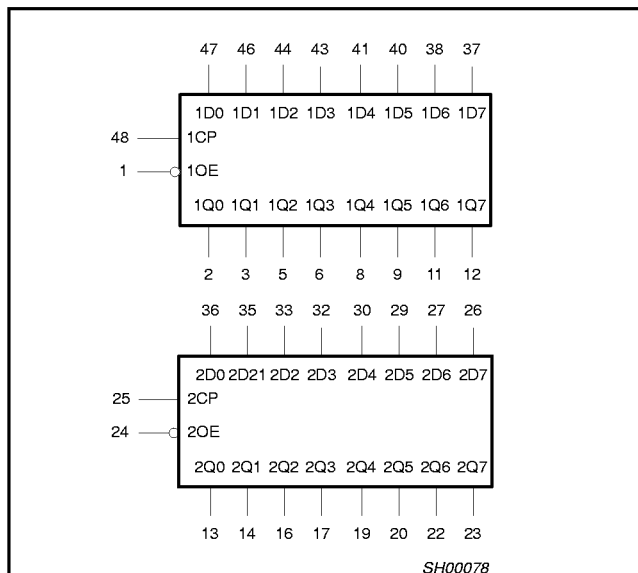
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ABT16374B DL	BT16374B DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABT16374B DGG	BT16374B DGG	SOT362-1
48-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ABTH16374B DL	BH16374B DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABTH16374B DGG	BH16374B DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	1OE, 2OE	Output enable inputs (active-Low)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

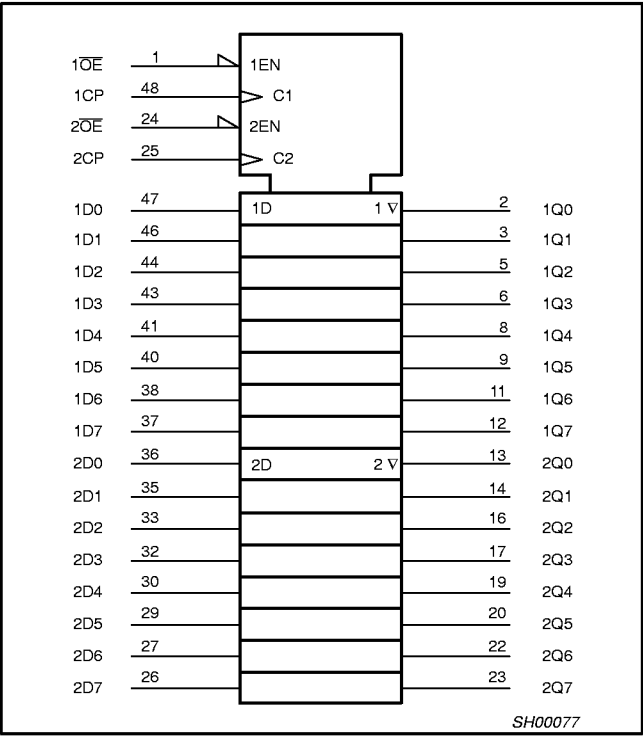
LOGIC SYMBOL



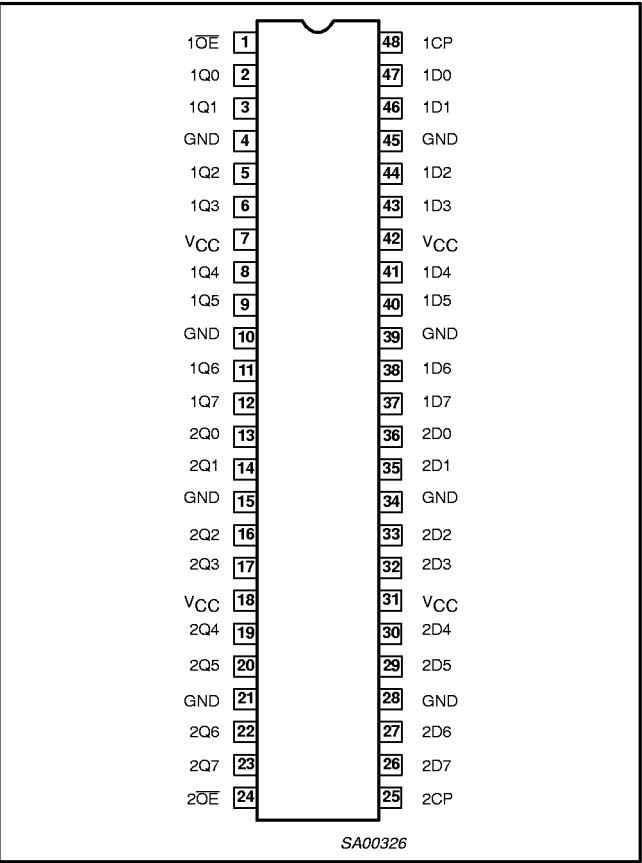
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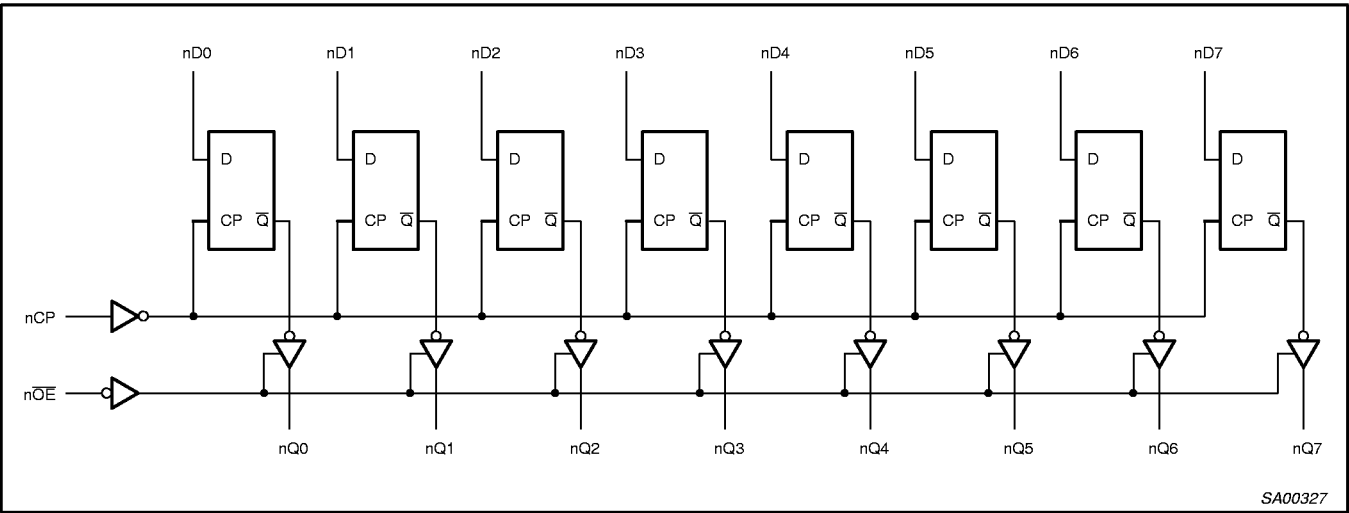
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



LOGIC DIAGRAM



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FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nCP	nDx		nQ0 – nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↑	X	NC	NC	Hold
H H	↑ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level

h = High voltage level one set-up time prior to the High-to-Low E transition

L = Low voltage level

l = Low voltage level one set-up time prior to the High-to-Low E transition

NC = No change

X = Don't care

Z = High impedance "off" state

↑ = Low-to-High clock transition

↑ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		–0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	–18	mA
V _I	DC input voltage ³		–1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	–50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	–0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	
T _{stg}	Storage temperature range		–65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level input voltage		0.8	V
I _{OH}	High-level output current		–32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	–40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = −18mA			−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}		2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}		3.0	3.4		3.0		
		V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}		2.0	2.4		2.0		
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}			0.42	0.55		0.55	V
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}			0.13	0.55		0.55	V
I _I	Input leakage current 74ABT16374B	V _{CC} = 5.5V; V _I = V _{CC} or GND			0.01	±1		±1	μA
I _I	Input leakage current 74ABTH16374B	V _{CC} = 5.5V; V _I = V _{CC} or GND	Control pins		±0.01	±1		±1	μA
		V _{CC} = 5.5V; V _I = V _{CC}	Data pins ⁵		0.01	1		1	
		V _{CC} = 5.5V; V _I = 0		−1	−3		−5		
I _{HOLD}	Bus Hold current inputs ⁶ 74ABTH16374B	V _{CC} = 4.5V; V _I = 0.8V		50			50		μA
		V _{CC} = 4.5V; V _I = 2.0V		−75			−75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V		±800					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V			±5.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = GND			±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}			0.5	10		10	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}			−0.5	−10		−10	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}			5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V		−50	−70	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}			0.5	2		2	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}			8	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}			0.5	2		2	mA
ΔI _{CC}	Additional supply current per input pin ² 74ABT16374B	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND			5	100		100	μA
ΔI _{CC}	Additional supply current per input pin ² 74ABTH16374B	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND			0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V .
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec . From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$ a transition time of up to $100\mu\text{sec}$ is permitted.
- Unused pins at V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	180	260				MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	1.7 1.4	2.6 2.2	4.0 3.4	1.7 1.4	4.7 3.9	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	3 4	1.3 1.3	2.4 2.3	3.7 3.4	1.3 1.3	4.7 4.6	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	3 4	1.9 1.7	3.1 2.6	4.6 4.0	1.9 1.7	5.5 4.4	ns

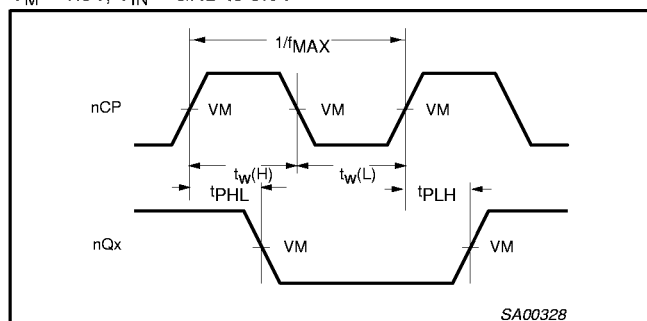
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

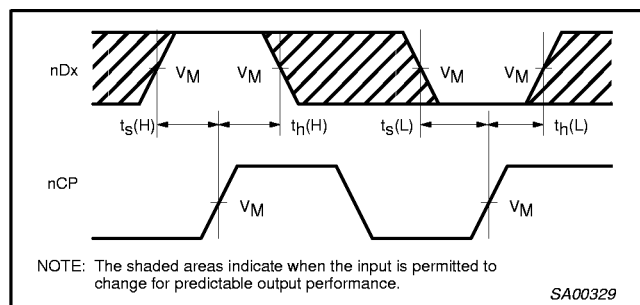
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time, High or Low nDx to nCP	2	1.0 1.0	0.3 0.1	1.0 1.0	ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold time, High or Low nDx to nCP	2	1.0 1.0	-0.1 -0.3	1.0 1.0	ns
$t_{\text{W}}(\text{H})$ $t_{\text{W}}(\text{L})$	nCP pulse width High or Low	1	2.8 2.8	1.2 1.5	2.8 2.8	ns

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



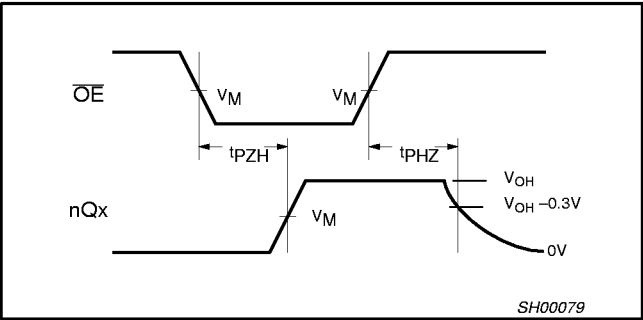
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



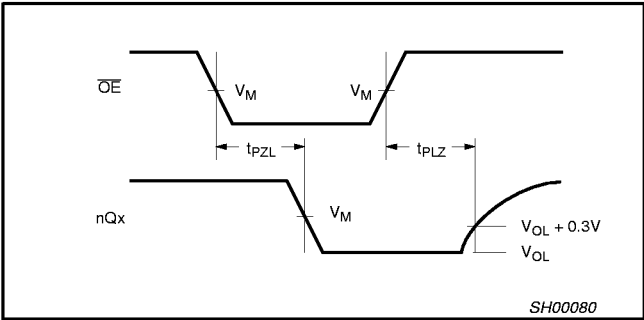
Waveform 2. Data Setup and Hold Times

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Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
tPLZ	closed
tpZL	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

$V_M = 1.5V$

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

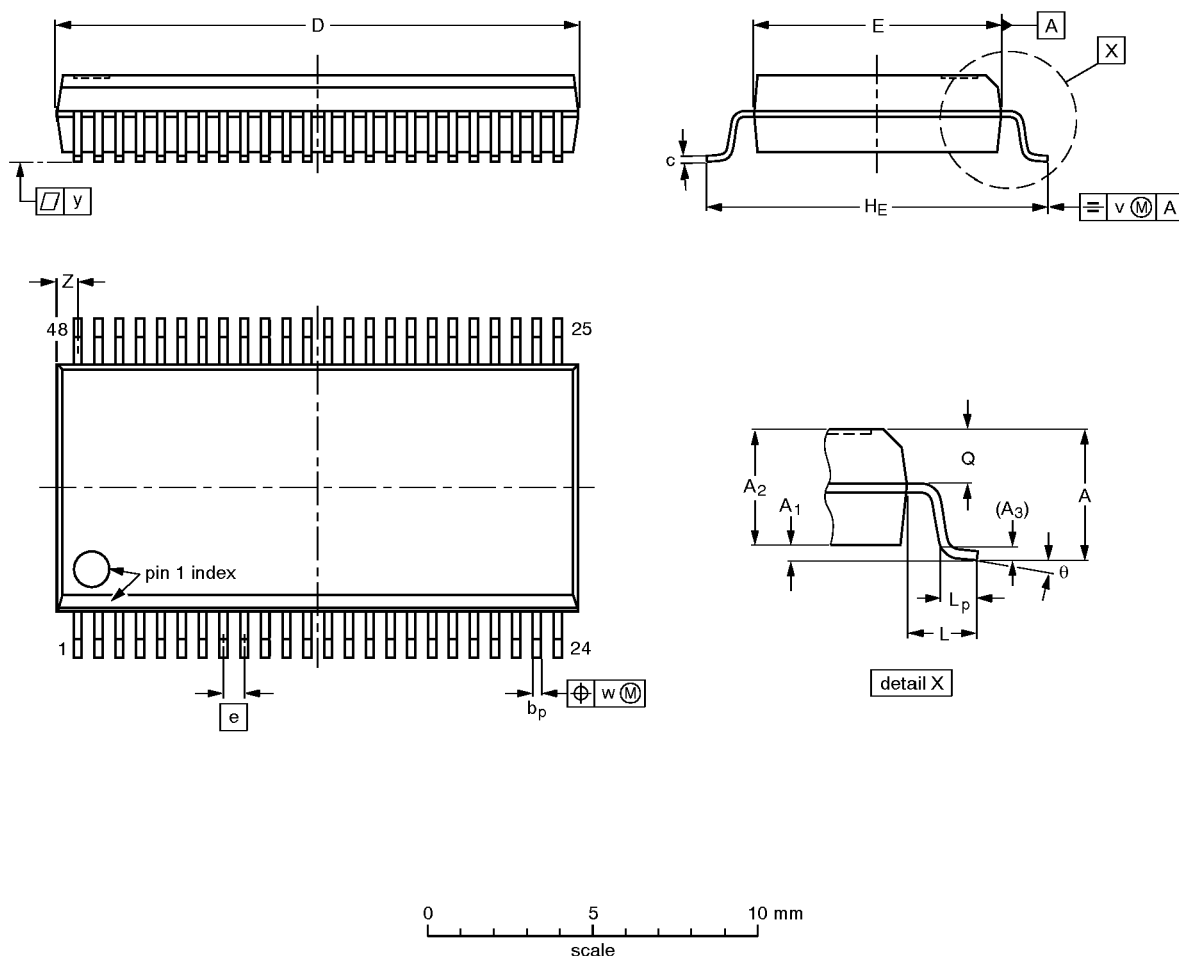
SA00018

Dual octal D-type flip-flop;
positive-edge trigger (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02 95-02-04

Dual octal D-type flip-flop;
positive-edge trigger (3-State)

74ABT16374B
74ABTH16374B

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1

