PRELIMINARY

T-46-23-37

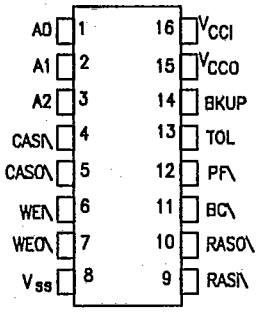
DALLAS SEMICONDUCTOR

DS1237
DRAM Nonvolatizer Chip

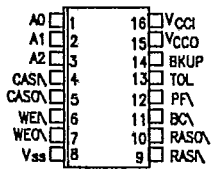
FEATURES
- Converts DRAM into nonvolatile RAM
- Controls any density of DRAM
- Wide backup supply voltage range
- Automatically refreshes when power fail detection occurs
- Power fail detection signal for hardwire interrupt
- Refresh is turned over to the processor after power-up under software control
- Space-saving 16-pin DIP and 16-pin SOIC for surface mounting
- Low-power CMOS
- Built-in backup condition circuit warns of impending backup supply failure
- Software-controlled backup supply disconnects switch for storage and shipment
- Software-controlled counter measures backup supply discharge time
- Optional refresh periods of 8 ms, 16 ms, 32 ms, and 64 ms are available to support extended refreshing at reduced power levels

DESCRIPTION
The DS1237 DRAM Nonvolatizer Chip is a CMOS circuit designed to control DRAMs such that information stored in memory is retained and protected during power failure. The DS1237 accomplishes this by monitoring the power supply for an out-of-tolerance condition. When such a condition occurs, DRAM is isolated from system control and the power supply for the DRAM is switched from V_{CC} to the backup supply. Refresh control is maintained by the DS1237 until the power is within specifications. At this time refresh is returned to the system after a highly structured serial sequence on address lines A0, A1, and A2. Other serial sequences are used to set switches which control a counter used to measure backup supply discharging and electrically connect or disconnect the backup supply.

PIN CONNECTIONS



DS1237 16-Pin DIP (300 Mil)



DS1237S16-Pin SOIC (300 Mil)

PIN NAMES (\ Indicates Condition Low)

BKUP	- Backup Supply
BC\	- Backup Condition
TOL	- V_{CCI} Trip Point Select
PF\	- Power Fail Output
A0-A2	- Address Inputs
Vss	- Ground
WEI\	- Write Enable Input
WEO\	- Write Enable Output
CASI\	- CAS\ Input from System
CASO\	- CAS\ Output to DRAM
RASI\	- RAS\ Input from System
RASO\	- RAS\ Output to DRAM
V_{CCO}	- V_{CC} Output to DRAM
V_{CCI}	- +5 Volt Input

OPERATION - NORMAL POWER CONDITIONS

Under normal operation system +5 volt power is supplied within the tolerance limits set by Pin 13 (TOL). If pin 13 is connected to V_{cco}, the DS1237 will operate in the normal mode down to 4.75 volts. When pin 13 is grounded, the DS1237 will operate in the normal mode down to 4.5 volts. During normal operation the RAS\, CAS\, and WE\ inputs are directly routed to the respective outputs with a maximum propagation delay of 15 ns. The backup supply input is normally connected to either a chargeable capacitor or battery; however, any backup supply with a voltage input between the limits of 6.0 volts and 10 volts is suitable. The power fail output (PF\) is at high level and address inputs A0, A1, and A2 are monitored for software-driven sequences. The backup condition output BC\ will be in an inactive (high) state provided that the backup input level is greater than 5.5 volts and the backup counter has not reached zero.

OPERATION - POWER LOSS AND DATA RETENTION

When the 5 volt V_{cc} power begins to drop, a precision band gap comparator senses this change. Depending on the level of the Tolerance Pin 13, a power fail signal will be generated as V_{cci} falls below 4.75 volts or 4.5 volts. The power fail output signal is driven low at this time and will stay low until V_{cci} is restored to normal conditions. When the data retention mode is turned on, the DS1237 isolates all control inputs and starts driving the RAS\, CAS\, and WE\ outputs. In addition, if RAS\ = 1, the DS1237 immediately takes control and issues the first refresh burst 62.5 uS later. If RAS\ = 0, the DS1237 will wait for RAS to go to a logic 1 level and then take control and issue the first refresh burst 62.5 uS later. If RAS\ = 0 and remains low for more than 10 uS after Power Fail Detect, the DS1237 will take control and drive RAS0\ = 1, then issue the first refresh burst 62.5 uS later. The V_{cci} input is disconnected from V_{cco} and the regulated backup supply is connected. A burst CAS\ before RAS\ refresh cycle is generated at a cycle time of 350 ns maximum. This burst refresh continues for 520 or 1032 consecutive cycles, depending on the dash number of the device (see Table 1). After the burst refresh is complete, subsequent burst refreshing continues at 8, 16, 32, or 64 ms intervals until V_{cci} returns to normal levels and the system signals the DS1237 that it is ready to assume refresh duties. The WE\ output is held at the high (inactive) level from the time power fail is detected until the system assumes refresh duties.

OPERATION - RETURN TO NORMAL POWER CONDITIONS

When the system +5 volt supply returns and exceeds the 4.5 volt BKUP supply voltage on pin 14, the V_{cci} input is immediately reconnected to the V_{cco} output pin while the regulated backup supply is internally disconnected from V_{cco}. Burst refreshing continues without interruption until the system signals that it is ready to assume the responsibility of refreshing the DRAMs. Refresh duties are shifted from the DS1237 to the system when a software controlled switch is set by sending a specific pattern on address lines A0, A1, and A2 for 24 consecutive cycles. This address pattern which sets the software switch is shown in Figure 1. The address pattern is clocked into the DS1237 on the falling edge of CAS\ provided that setup and hold times are met. When the 24th cycle is correctly entered, the DS1237 will issue a final refresh burst and then turn over control to the host system. At this point, the host system will be responsible for handling all refresh requirements. RAM read and write cycles can resume without restrictions after the software switch is correctly set.

ACTIVATION OF BACKUP SUPPLY

A software-controlled switch allows conservation of the backup supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. On the initial application of the battery, the battery backup switch will be off. The bit patterns shown in Figure 2 turn on or off this switch which connects or disconnects the backup supply.

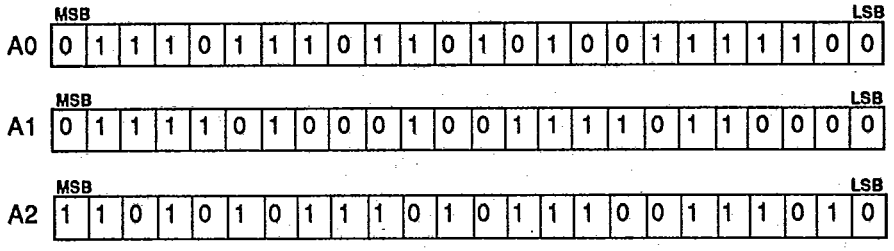
NOTE: On the initial connection of the battery, the battery backup switch will be off.

REFRESH INTERVALS Table 1

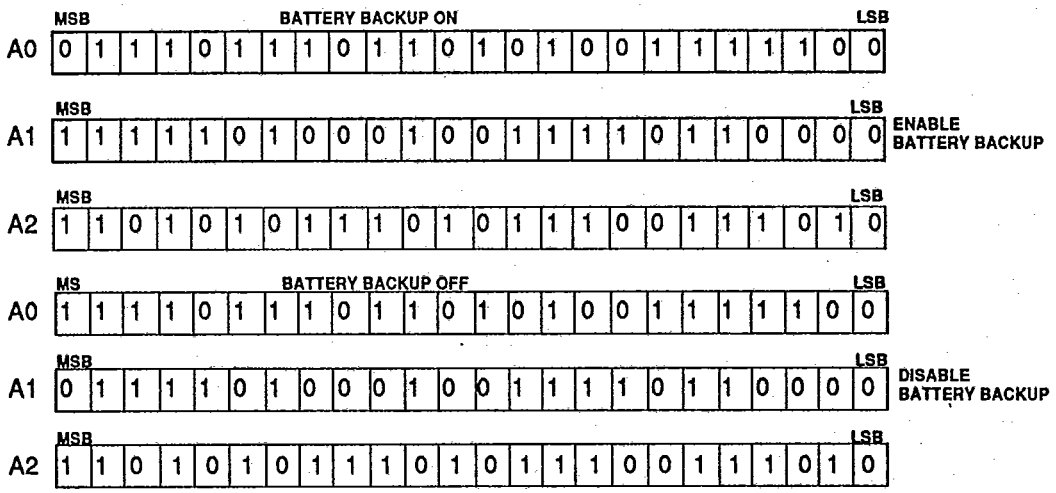
	REFRESH INTERVAL*			
NUMBER OF CYCLES	8	16	32	64
256K DRAM: 520	-1	-2	-3	-4
1 Meg DRAM: 1032	-5	-6	-7	-8

*Refresh intervals have a tolerance of +0/-12.5%.

SOFTWARE SWITCH FOR PROCESSOR CONTROL ON POWER-UP Figure 1



SOFTWARE CONTROLLED SWITCH FOR ACTIVATION OF BACKUP SUPPLY Figure 2



BATTERY CONDITION

The DS1237 has two features which provide information about the condition of the backup supply. First, the DS1237 monitors the backup supply input condition. If this input is below V_{cci}, the backup condition output pin (BC\) is driven to the active state (low) and will remain in this state until the backup supply voltage is restored to a level above V_{cci}. This feature is active only while V_{cc} is applied within nominal limits. Whenever the backup supply is supplying power, the BC\ pin remains at a logic zero state. The second feature for monitoring the condition of the backup supply is a counter which is decremented on one second intervals whenever the backup supply is supplying power. This counter is set with a number while V_{cc} is within nominal limits. The value of the counter is entered by sending a 24-bit sequence on address lines A0, A1, and A2 in the same manner as described for refresh control. This sequence is shown in Figure 3. After the 24-bit sequence is correctly entered, the next 24 bits will define the time count in seconds which will start decrementing down when the backup supply is supplying power. This count is 24 bits long and is entered LSB first on address line A0 when the CAS line goes low. The counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the BC\ pin will be low even though the V_{cc} supply is within nominal limits. The BC\ pin will remain low until a new value is entered into the counter. This time can be calculated by dividing the capacity in ampere hours of the backup supply by the average load current of the DRAMs and converting this value into seconds (see Figure 5). The value in the counter can be read at any time while V_{cc} is within nominal limits by sending the 24-bit sequence which is shown in Figure 4. This sequence is entered in the same manner as described for refresh control. After this sequence is correctly entered, the next 24 CAS\ cycles will cause the contents of the counter to be shifted out one bit at a time starting with the LSB on the BC\ pin. A logic zero on BC\ while CAS\ is low is a logic zero for that bit.

BACKUP CONDITION APPLICATIONS

The backup condition features of the DS1237 can supply the system valuable information about the backup supply. A simple application may only use the V_{cc} comparator to tell the system that a battery is weak and should be replaced. A more sophisticated system may use the backup condition counter to measure the time that a primary battery is used to supply power to DRAMs. By knowing the capacity of the battery and the requirements of the DRAM, the time for battery replacement can be predicted. In fact, if worst case primary supply outages can be estimated, the backup battery can be selected so that replacement can always occur prior to backup supply failure. If a rechargeable backup supply is used, such as a capacitor or a nicad battery, the backup condition counter can be used to measure both the charge and discharge time. Charge time can be measured by using a system time base and periodically adjusting the battery condition counter under software control to reflect the amount of time (amount of charge) that the system primary power is within nominal limits.

NOTE:

The DS1237 requires capacitive bypassing techniques between V_{cco} and GND for proper operation. A bypass capacitor between V_{cci} and BKUP is also essential for proper operation. While applications vary, a 10 uf capacitor value is typically required.

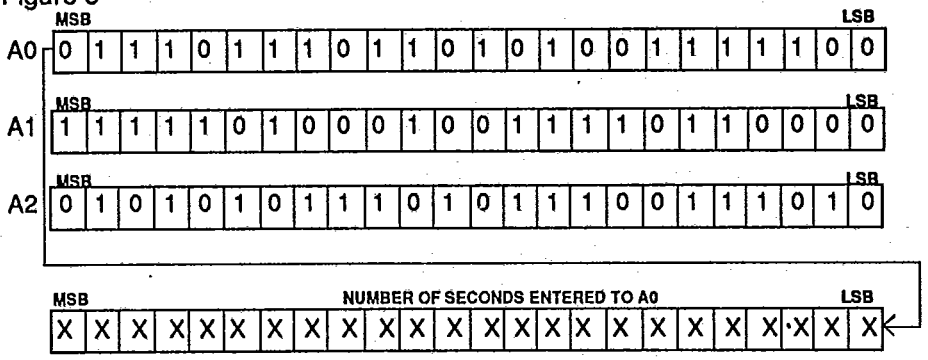
DATA RETENTION TIMES

The equations in Figure 5 are used to find the data retention time of DRAMs using the DS1237 DRAM Nonvolatizer Chip.

Calculating the actual current consumption of the DRAMs requires special attention since they are placed into the standby mode and then activated only when refreshing is required. This implies that the current draw of the DRAMs will be an average of the standby current and the active currents in direct proportion to the refresh cycle time and duration.

SOFTWARE SEQUENCE FOR SETTING THE BACKUP CONDITION COUNTER

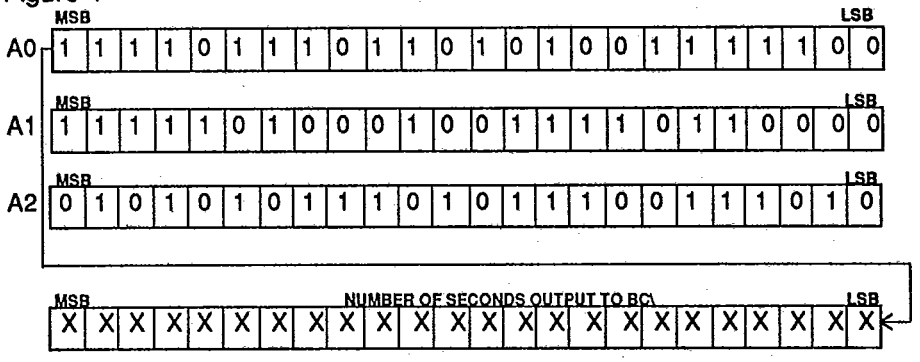
Figure 3



NOTE:
The binary count which is entered into the backup condition counter is a calculated value based on application and has a range of 2^{24} seconds with an accuracy of +/- 20%.

SOFTWARE SEQUENCE FOR READING THE BACKUP CONDITION COUNTER

Figure 4



DS1237 NONVOLATIZER DRAM DATA RETENTION TIMES Figure 5

$I_{datareten}$ = (# of DRAMs) x [(I_{act} + I_{std}) / $8e^{-3}$] + 4 mA

where,

I_{act} = 520 x $350e^{-9}$ x I_{active}
- 520 => number of refresh cycles (burst)
- $350e^{-9}$ => access cycle time of DRAM, and
- I_{active} => active current draw of DRAM

I_{std} = ($8e^{-3}$ - (520 x $350e^{-9}$)) x $I_{standby}$
- $8e^{-3}$ => refresh period
- 520 => number of refresh cycles (burst)
- $350e^{-9}$ => access cycle time of DRAM, and
- $I_{standby}$ => standby current draw of DRAM.

The forgoing equations can then be used to directly calculate the data retention time:

$t_{datareten} = Q_{bat} / I_{datareten}$

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ABSOLUTE MAXIMUM RATINGS *

Voltage on Battery Input Pins Relative To Ground	-0.3V to +12V
Voltage on any Other Pin Relative to Ground	-0.3V to +7V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	Volts	1
Voltage Input Logic 1	V_{IH}	2.0		V_{CC}+0.3V	Volts	1
Voltage Input Logic 0	V_{IL}	-0.3		+0.8	Volts	1
Backup Supply	BKUP	6.0V	8.0V	10.0	Volts	2,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.50V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-2.0			mA	1,5
Output Current @ 0.4 V	I_{OL}	+8.0			mA	1,5
Input Supply Current	I_{CCI}		3	7	mA	6
Output Supply Current $V_{CCO}=V_{CCI}$ -0.2 V	I_{CCO}			200	mA	4
PF\ Detect TOL = V_{CCO}	V_{TP}	4.5	4.62	4.75	V	7
PF\ Detect TOL = GND	V_{TP}	4.25	4.37	4.5	V	7
Output Supply Current $V_{CCI} < V_{TP}$	I_{CCOB}			30	mA	8
Backup Supply Leakage	I_{BKUP}			1	uA	9

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CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	COND.	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	7		pF	

AC ELECTRICAL CHARACTERISTICS - RAPID REFRESH

(0° to 70°C, $V_{CCI} < V_{TP}$)

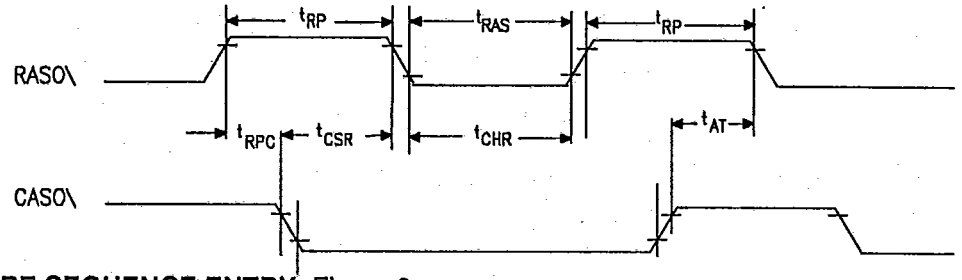
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RASO\ Precharge Time	t_{RP}	90			ns	
RASO\ Precharge to CASO\ Hold Time	t_{RPC}	60			ns	
CASO Setup Time	t_{CSR}	30			ns	
CASO\ Hold Time	t_{CHR}	60			ns	
RASO\ Pulse Width	t_{RAS}	0.120		10	us	
Elapsed Time Between Rapid Refresh Burst	t_{AT}	SEE TABLE 1			ns	

AC ELECTRICAL CHARACTERISTICS

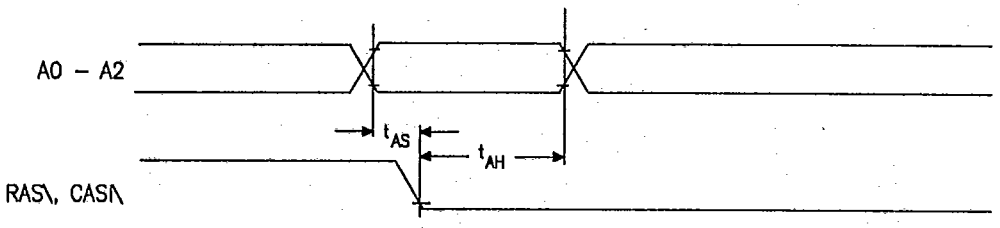
(0°C to 70°C, $V_{CCI} > V_{TP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	0			ns	
Address Hold Time	t_{AH}	20			ns	
Propagation Delay	t_{PD}		7	15	ns	

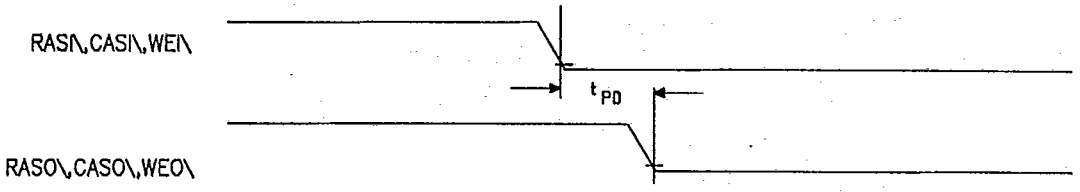
REFRESH CYCLE DURING BURST REFRESH RETENTION (WEO=V_{IH}) Figure 5



SOFTWARE SEQUENCE ENTRY Figure 6



PROPAGATION DELAY - NORMAL OPERATION Figure 7



NOTES

1. All voltages are referenced to ground.
2. The BC\ pin will be driven active whenever V_{CC} is within nominal limits and the backup supply is below V_{CC}.
3. Backup input voltage is internally regulated within the DS1237 such that V_{CCO} is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
4. I_{CCO} is the maximum current which the DS1237 can supply to RAM through the V_{CCO} pin with a voltage drop of less than 0.2 volts.
5. Load capacity is 300 pF.
6. Measured with all outputs open.
7. V_{TP} is the trip point where the internal switching circuits disconnect V_{CCI} and connect the internally regulated backup supply to V_{CCO}. Rapid refresh is also initiated at this time, and the PF\ output is driven active.
8. I_{CCOB} is the maximum current the DS1237 can supply to RAM through the V_{CCO} pin from the internally regulated supply while in the data retention mode.
9. Backup leakage is the internal current consumed by the DS1237 in the data retention mode, with battery backup disabled.

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APPLICATION NOTE: DIODE CONTROL OF BKUP INPUT

The fabrication of the DS1237 produces an N well for the BKUP input (pin 14) that must be considered by the user. Because of this it is imperative that the BKUP input does not go more negative from V_{CCI} input (pin 16) than the amount of one silicon diode.

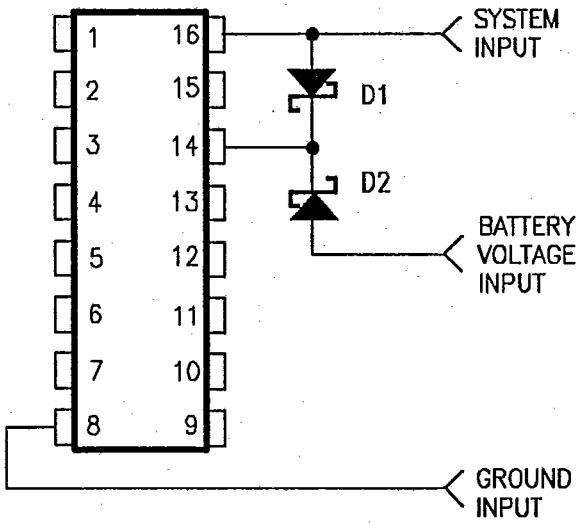
This requirement can be achieved by using a Schottky diode (D1) between the V_{CCI} input and BKUP input (see example below). This diode will limit the negative voltage level of BKUP input relative to the V_{CCI}.

A Shottky diode is required for D1.

Eventually the battery voltage that is applied to the BKUP input can decrease below the negative clamp voltage of D1. At this time, the battery should be disconnected from the circuit during the time that V_{CCI} input is present.

This can be achieved by using a diode (D2) between the battery positive supply lead and the BKUP input. Diode D2 will then disconnect the battery positive suply lead from the BKUP input when the battery output voltage has decreased.

A Shottky diode is suggested for D2.



NOTE: For circuits where the BKUP source is a primary battery, Underwriter Laboratories requires D2.