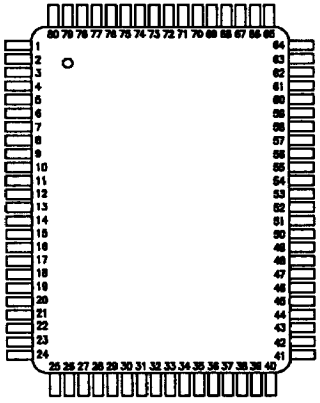
DALLAS SEMICONDUCTOR

DS53xx
Micro Softener Chips

FEATURES

- Chips provide softness for microprocessor or microcontroller-based systems
- Adapts to task-at-hand:
  - -Converts CMOS SRAM into lithium-backed NV program/data storage
  - -Freshness seal ensures maximum lithium life
  - -Serial bootstrap loading of software
  - -Code can be changed in end use
- Crashproof operation:
  - -NV storage for 10 years with no V_{CC}
  - -Orderly shutdown/ restart on power-up/down
  - -Inadvertent write protection
  - -Restart on errant software execution
- Provides enhanced 8-bit parallel I/O ports:
  - -One port generates 8 separate edge- or level-triggered interrupts
  - -Two ports support Dual Port Register file interface for PC-bus applications
- Processor-specific versions
  - -DS5340FP: Compatible with NEC V40; allows code development in PC native instruction set
  - -DS5303FP: Compatible with Hitachi HD6301/HD6303 Family
- FUTURE PRODUCTS:
  - DS5396FP: Compatible with Intel 80C196 Family
  - DS5311FP: Compatible with Motorola 68HC11 Family

PIN DESCRIPTION



80-Pin Quad Flat Pack

DESCRIPTION

The DS53xx Micro Softener Chips provide the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities for systems based on a variety of processor architectures.

Each version of the Micro Softener interfaces directly to a specific processor's address/data bus and control signals and can typically convert as much CMOS SRAM as can be addressed within the processor's memory map into lithium-backed nonvolatile read/write storage. This storage is initially bootstrap loaded via the serial port and can be changed at any time without the removal of components from the end system. In addition, the storage can be dynamically partitioned into separate program and data areas so that the program area is write-protected. Through proper selection of a lithium cell, the contents of the RAM can easily retain data in the absence of external power for over ten years.

The Micro Softener Chips provide crashproof operation when system power is momentarily disrupted or removed entirely. Early warning of a potential power failure is signalled by the Micro Softener so that the operational state of the system can be stored prior to a complete removal of system V_{CC}. The contents of the external nonvolatile SRAM and Micro Softener's configuration registers are automatically sustained at low current from an external lithium energy source for the entire time that V_{CC} is removed. When V_{CC} is applied once again, the Micro Softener automatically restarts the processor without the need for external circuitry. Regardless of whether the power merely fluctuates or is absent for years, upon its return the processor will have the ability to resume execution as if the power failure had not occurred at all.

Crashproof operation is provided in electrically noisy operating environments. A watchdog timer restores controlled software execution following a disruption in normal program execution, as might be caused by a transient condition. In addition, a timed access feature ensures controlled access to critical bits in the Micro Softener's configuration registers as well as to the write-protected portion of the nonvolatile SRAM.

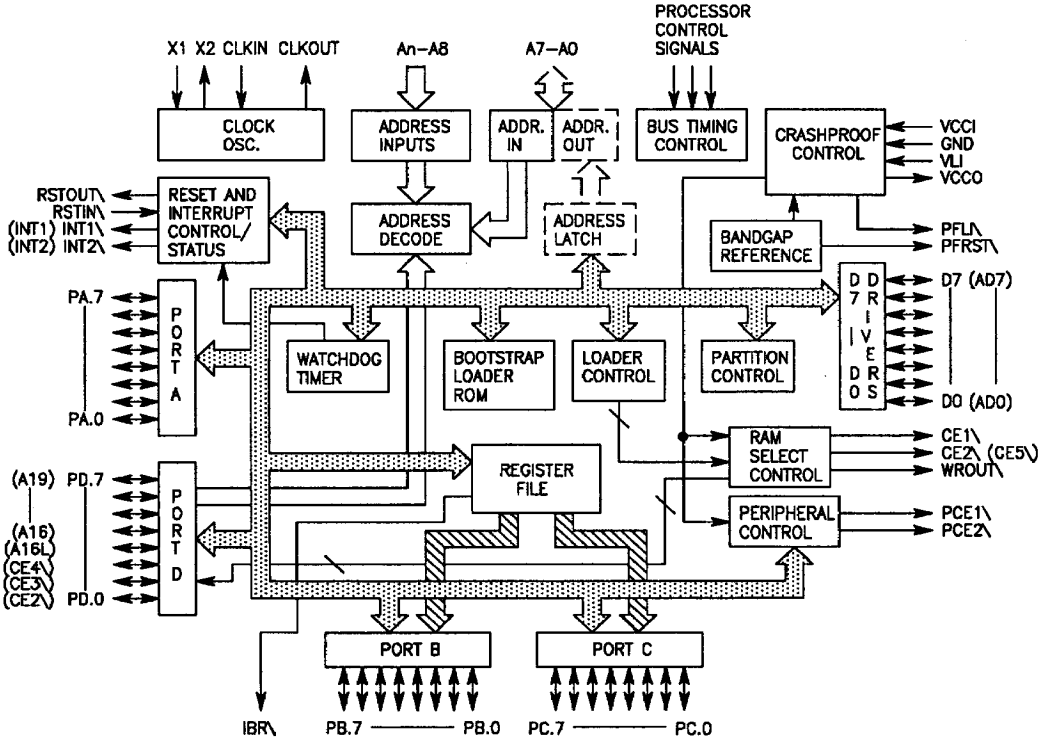
Depending on the specific version of the Micro Softener, up to four parallel I/O ports are provided which offer extended I/O capabilities. All versions incorporate one port which allows each pin to serve as an edge-triggered or level-sensitive interrupt input. In addition, all versions offer two ports that can be configured as an interface to the internal dual port register file. This software-invoked feature converts these two ports into a high-speed parallel bus interface to a host microprocessor. As a result, the Micro Softener-based system can act as an intelligent peripheral controller in a host system, such as a PC.

Finally, the Micro Softener allows interface to external peripheral devices with little or no external glue logic.

GENERIC FEATURES

Features which are generic to the entire family of Micro Softeners are described below. Detailed information for specific versions of Micro Softeners are given in individual device data sheets. Figure 1 is an internal block diagram of the generic Micro Softener.

GENERIC MICRO SOFTENER BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

V_{CCI}, GND - Power Supply Inputs
V_{CCI} is the +5V power supply voltage input; GND is tied to system ground.
V_{LI} - Lithium Supply Input
V_{LI} is tied to an external +3V lithium energy cell.
V_{CCO} - Power Supply Output
V_{CCO} is the power supply output used to power external nonvolatile CMOS SRAM and peripheral devices.
An-A8 - Address Bus Inputs
An-A8 are tied to the corresponding address output pins from the system processor.
D7-D0 - Data Bus; Bidirectional
(AD7-AD0) - Multiplexed Address/Data Bus; Bidirectional
These pins are used to interface to the system data bus. Processor-specific versions of the Micro Softener interface to either non-multiplexed data busses or multiplexed address/data busses.
A7-A0 - Address Bus Inputs (Address Bus Outputs)
For non-multiplexed data bus versions, A7-A0 are used to interface to the corresponding address output pins from the system processor. For multiplexed address/data bus systems, these pins output the demultiplexed lower 8 bits of address which are latched from the multiplexed address/data bus pins.
Processor Control Signals
Each processor-specific version of the Micro Softener provides a set of control inputs that connect directly to the processor's bus control signals. These pins signal read or write operations on the system bus to the Micro Softener.
CE1-2\ (CE3-5\); Chip Enable Outputs
One or more of these pins are typically tied to bytewide CMOS SRAMs that are maintained as nonvolatile program/data storage by the DS53xx. Each chip enable signal is assigned to a block of the processor's memory map during serial bootstrap loading of the system. One of these pins will be driven low when a memory cycle is decoded by the DS53xx as an access to a location within one of these blocks. These pins are held in their inactive high state by lithium backup in the absence of V_{CC}.
PCE1\, PCE2\ - Peripheral Chip Enable Outputs
PCE1\ and PCE2\ are software-selectable chip enable outputs to peripheral devices interfaced to the system address/data bus. A Peripheral Enable output pin will be driven low when the processor performs a read or write cycle to an address within the range assigned to that pin.
WROUT\ - Write Output
WROUT\ is driven low when a processor write cycle is being performed under the direction of the DS53xx.
X1, X2 - Crystal Inputs
X1 and X2 are used to tie a crystal to the internal clock oscillator circuit and set the operating frequency of the system. X1 is the input to the inverting oscillator amplifier and X2 is the output.
CLKOUT - Clock Output
CLKOUT is used to output a TTL/CMOS-compatible clock output from the internal oscillator circuitry within the DS53XX. Normally, this signal is used to clock the system processor and can be tied to other peripheral devices.

CLKIN - Clock Input
CLKIN is intended to be tied to the processor's CMOS-compatible clock output. The circuitry within the Micro Softener monitors this signal as an indication of activity within the processor for detection of low power standby operating modes and/or for synchronization purposes.
RSTOUT\ - Output; Active Low
The RSTOUT\ pin is provided to place the system processor in a reset condition in response to one of several conditions: When a power-on condition has occurred, when a power-off condition is about to occur, when a watchdog time-out has occurred, or when a reload condition is invoked.
RSTIN\ - Input; active low
This pin is used to monitor a system reset line. The Micro Softener's RSTOUT\ is driven to its active level in response to an active level applied on RSTIN\.
INT1\, INT2\ (INT1, INT2) - Interrupt Outputs; Active Low
INT1\ and INT2\ are used to signal the system processor of pending interrupt conditions within the Micro Softener.
PFRST\ - Power Fail Reset; Output, Active Low
PFRST\ indicates that V_{CC} voltage has dropped below the processor's minimum operating threshold, and for that reason the processor is being held in a reset state by the Micro Softener.
PFLI\ - Power Fail Lithium; Output, Active Low
PFLI\ is used to indicate that V_{CC} voltage has dropped below the lithium cell's voltage (nominally 3.0V) and that the Micro Softener's configuration registers, the external NV SRAM, and any peripheral circuit (such as a DS1283 Watchdog Timekeeper Chip) controlled by the lithium-backed PCE1\ pin are being supplied from the lithium cell tied to V_{LI}.
IBR\ - Input Buffer Ready; Output, Active Low
When the dual port register file interface has been enabled in place of Ports B and C, the Input Buffer Ready signal is used to indicate to the host processor that the selected input buffer registers are ready to accept data from the host processor.
PA7-PA0 - Port A; Bidirectional I/O
PA7-PA0 are the interface pins to the multiple-mode bidirectional I/O port designated as Port A. These pins can also be individually programmed as edge- or level-sensitive interrupt inputs.
PB7-PB0 - Port B; Bidirectional I/O
PB7-PB0 are the interface pins to the multiple-mode bidirectional I/O port designated as Port B. This port can also be programmed to provide address, control, and status signals for the internal Dual Port Register File in conjunction with Port C.
PC7-PC0 - Port C; Bidirectional I/O
PC7-PC0 are the interface pins to the multiple-mode bidirectional I/O port designated as Port C. This port may also be programmed to provide a bidirectional data bus interface for the internal Dual Port Register File in conjunction with Port B.
PD7-PD0 - Port D; Bidirectional I/O
PD7-PD0 are the interface pins to the multiple-mode bidirectional I/O port designated as Port D. On some versions of the Micro Softener, Port D is replaced with higher order address inputs and additional chip enable outputs.

ARCHITECTURAL DESCRIPTION

The following is a generic description of the internal architecture for the Micro Softener family. Figure 1 should be used for reference.

ADDRESS DECODE

During execution of processor read and write cycles, the Micro Softener accepts and decodes all of the incoming address lines from the system processor. For most designs, the Micro Softener defines the entire memory map for the system. It controls the selection of the external NV SRAM, on-chip registers, and external peripheral devices.

Each processor-specific version of the Micro Softener provides programmable chip enable outputs for control of external bytewide CMOS SRAM. Sufficient control is provided so that the majority of the processor's address space can be populated with NV SRAM under the control of the Micro Softener. The chip enable outputs are configured during serial bootstrap loading to decode blocks of memory corresponding to the density of the bytewide memory chips and/or SIMMs in the system. Depending on the processor-specific version, some combination of 8K x 8, 32K x 8, 128K x 8, or 512K x 8 blocks are decoded.

Address partition control bits within the Micro Softener allow the distinct program and data areas to be defined in the NV SRAM. The areas designated for program code cannot be overwritten via a normal processor write cycle. A multiple instruction Timed Access write sequence must be performed within a specified time window in order to modify the partition bits so that program code can be modified by the application software. The program code is thereby protected from inadvertent write operations in the event of errant software execution.

Locations in the external NV SRAM that are not accessible include those locations that are occupied by the internal registers of the processor and of the Micro Softener.

Two peripheral enable signals (PCE1\ and PCE2\) are provided to interface to chip enable inputs on peripheral devices. Each signal can be individually enabled or disabled by software during system operation. When it is enabled, the peripheral enable signal will pulse active low during a read or write cycle within a specified 256-byte block of memory. When disabled, locations within the external NV SRAM can be accessed instead of the peripheral device.

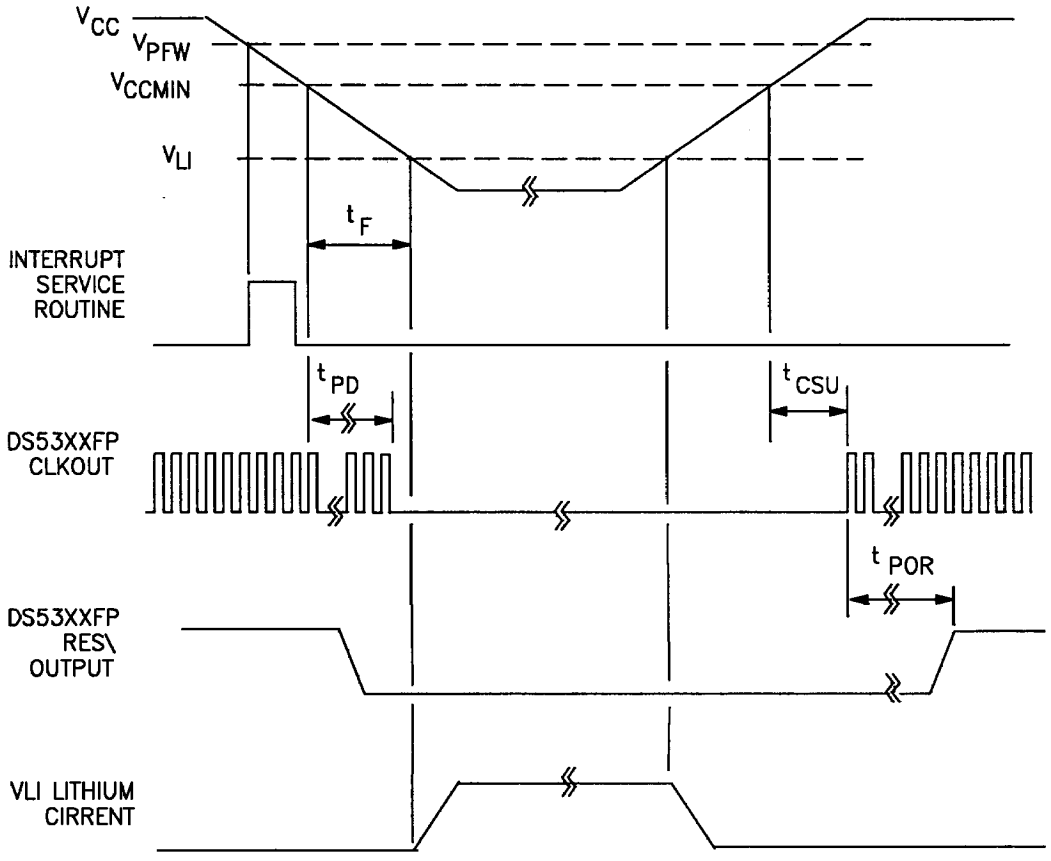
PCE1\ is designed to be a chip enable control signal for a peripheral device that is sustained from the lithium cell in the absence of V_{CC}. As a result, it remains at a logic high (inactive) level when system V_{CC} is removed. A common application for this feature would be to control the Dallas DS1283 Watchdog Timekeeper Chip, which can be permanently powered from the Micro Softener's V_{CCO} output. PCE2\ collapses to ground in the absence of V_{CC}.

LOW POWER STANDBY

The Micro Softener responds to software-initiated low-power standby modes in which the internal processor clock is halted. In some microprocessors, this is referred to as the Stop mode. In Stop mode, the processor draws a reduced amount of current from its V_{CC} line in order to retain the contents of its on-chip registers and/or RAM and thereby retain its operating state. The Micro Softener is capable of sensing such a mode of operation by the absence of a clock output signal from the processor on its CLKIN pin. In this event, the Micro Softener will disable the clock output (CLKOUT) from the processor and place itself in a low-power standby condition until a reset is issued, which is intended to resume processor operation. When such a signal is detected, the Micro Softener will once again supply a clock signal to the processor and will issue a reset signal to it.

IMAGE UNAVAILABLE

CRASHPROOF OPERATION TIMING Figure 2



input. Furthermore, each of these bits can be programmed to be level-sensitive or edge-sensitive. Each bit can also be programmed to interrupt on positive or negative signals. The processor is signalled by the DS53xx that such an interrupt has occurred via one of the processor's external interrupt lines. A register is provided within the Micro Softener which can then be polled by the processor to determine the source of the interrupt.

DUAL PORT REGISTER FILE

Ports B and C can also be software selected to serve an alternate function as an interface to an internal Dual Port Register File on the DS53xx. The Dual Port Register File interface allows the Micro Softener-based system to serve as a user-defined peripheral controller in a multiprocessor system. The host microprocessor can communicate over its data bus at high speed with the Micro Softener-based subsystem via the register file. In effect, the subsystem functions as a very sophisticated, user-reprogrammable peripheral device. The register file manages the transfer of data independent of the processor.

The register file function can be enabled or disabled from the application software. When it is enabled, the pins of Ports B and C are automatically redirected to serve the alternate functions as shown in Figure 3.

Within the Micro Softener, the register file consists of 8 input buffer registers, 8 output buffer registers, and a status register and interrupt control capability for both the host microprocessor and the subsystem's processor.

SERIAL BOOTSTRAP LOADER

The serial bootstrap loader is a firmware package contained within a special ROM area on the Micro Softener. It can be invoked either by external activation of the Reload pin, by the application software, or by detection of an error in the NV SRAM following a power-on or watchdog timer reset. When it is invoked, the processor is first internally reset and then executes code contained within the ROM. The firmware responds to commands from a host PC via the processor's asynchronous serial I/O port.

Initial loading of the application software and setting of the configuration registers within the Micro Softener is performed via the serial bootstrap loader. Once this information is loaded, it is sustained as nonvolatile information by the Micro Softener under power supplied by the lithium cell.

A variety of crystal frequencies and resulting baud rates are supported across a three-wire interface from the processor's serial I/O port.

When initialization is complete, the ROM is no longer present in the memory map of the processor, and the application software can be executed. The ROM is therefore transparent to the execution of application software.

The bootstrap serial loader implements an easy-to-use command line interface which facilitates communication from a PC. Functions that can be performed via the serial bootstrap loader include:

-Initialize memory range
-Load/dump application program into/from NV SRAM (absolute hex format)
- Verify application program in NV SRAM
- Fill memory range in NV SRAM
- Calculate, report, and store CRC value for requested NV SRAM range
-Initialize program/data partition
-Initialize freshness seal
-Select watchdog time-out value

DATA RETENTION AND FRESHNESS SEAL

Through proper memory and lithium selection, 10 years of data retention at room temperature can be achieved in the absence of V_{CC}. The Micro Softener draws no current from the lithium cell when V_{CC} is applied. Therefore, the 10 year figure is a cumulative amount of time for which lithium backup is required. Some capacity will be lost due to age of the lithium cell. However, lithium cells have an extremely long shelf-life when they are not supplying current, typically on the order of 30 to 40 years. As a result, such shelf-life considerations typically do not affect the data retention time for a given application.

The Micro Softener also incorporates a freshness seal feature that allows data retention to be disabled in the absence of V_{CC}. This feature is provided so that the lithium capacity can be preserved during times when the system is in storage and no data retention is required. The freshness seal is enabled during serial bootstrap loading by a special command. Upon the subsequent removal of V_{CC} following this operation, data retention will be disabled until the next time the system is powered up. After that time, data retention will again be enabled.

DEVICE DATA SHEETS

The user should consult the individual device data sheets for detailed information on a particular processor-specific version of the Micro Softener. Product previews are currently printed in the 1990-91 Dallas Semiconductor data book for the following versions:

DS5340 V40 Softener Chip
DS5303 6303 Softener Chip

In addition, product previews are printed in this data book for small, single-board soft Stik microcontroller systems based on these Micro Softeners:

DS2340 Soft V40 Flip Stik
DS2301 Soft 6301 Stik

Complete specifications on these products as well as information on future Micro Softener products is available on request from Dallas Semiconductor.

DUAL PORT REGISTER FILE PIN FUNCTIONS Figure 3