Logic Design Solutions

MESC-PM1

Enhanced Services Controller *MACRO*
Performance Monitor - 127 Connections

Data Sheet

Apr. 2000 – Ver. 3

Features

- Adjunct device to the Lucent ATM Port Controller (APC version 3) in ORCA 3T FPGA
- PM function carried out at the PM Sink only (destination of Forward PM cells)
- Extends the functionnality already available within the APC
- Directly connected to the Transmit ESI Interface of a single APC
- Maintain a different set of per VC statistics for up to 127 connections simultaneously
  - Ingress Received Cell Blocks (for convenience called - Stat 0)
  - Ingress Received CLP0+1 User Information Cells in a Block (for convenience called - Stat 1)
  - Ingress Severely Errored Cell Blocks (Bellcore GR1248 PM - Stat A)
  - Ingress CLP0+1 Errored Cells (Bellcore GR1248 PM - Stat B)
  - Ingress Lost CLP0+1 User Information Cells (Bellcore GR1248 PM - Stat C)
  - Ingress Misinserted CLP0+1 User Information Cells (Bellcore GR1248 PM - Stat E)
  - Ingress Total Transmitted CLP0+1 User Information Cells (Bellcore GR1248 PM - Stat F)
- Handle four Block size type per channel : 128, 256, 512 and 1024 cells
- Handle independant threshold for Lost, Misinserted and Errored statistics
- Simple CPU interface with Ready signal
- Available in VHDL source code format for ease of customization
- Can be customised by Logic Design Solutions

General Description

The MESC_PM1 function, implemented on a ORCA FPGA, is to extend the functionnality already available within the APC.
L.D.S. can integrate your decoding logic in the FPGA in addition to any other predesigned functions.

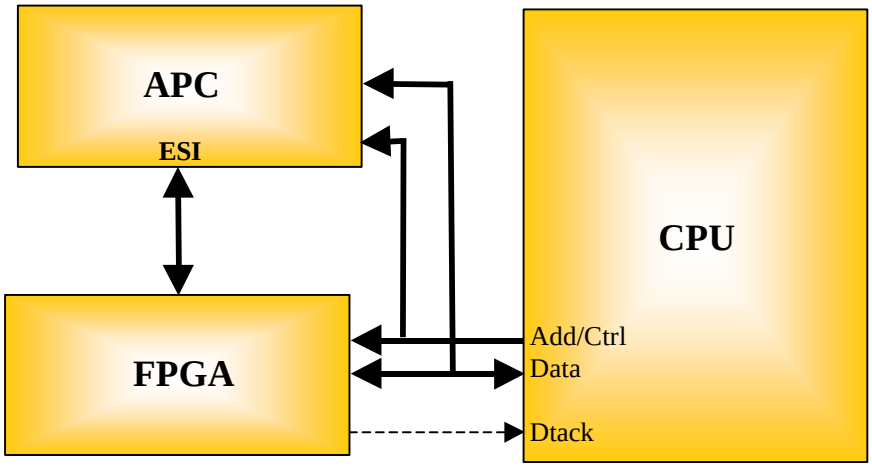
Design Package

Device Family	**ORCA 3T80-7-S208**	
PFUs	**411 – 85% used** *	
I/O	**64** **	
Package file options	**1**	**Bitstream + Data Sheet**
	2	**VHDL Source code** **VHDL Test Bench** for behavioural and gate level simulation. **Data Sheet** **Design Document :** features, architecture, interfaces and operation. **User's guide :** Simulation, Synthesis and Place and Route procedures. **Constraint Files :** « .prf » file
Design Tool Used	VHDL synthesis Leonardo Spectrum from Exemplar. VHDL ModelSim simulation tool from ModelTech. ORCA Foundry from Lucent Technologies.	
Support	Support provided by Logic Design Solutions 90 days e-mail and telephone support from Logic Design Solutions included in the Macro price. Support does not cover user Macro modifications. Maintenance Contracts available.	

* Synthesis option dependant (area/speed)
** Assuming all Macro signals are routed off chip.

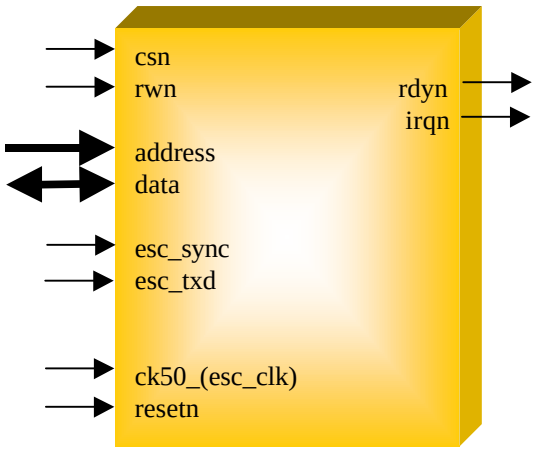
1. Description

1.1 Implementation example



1.2 Symbol

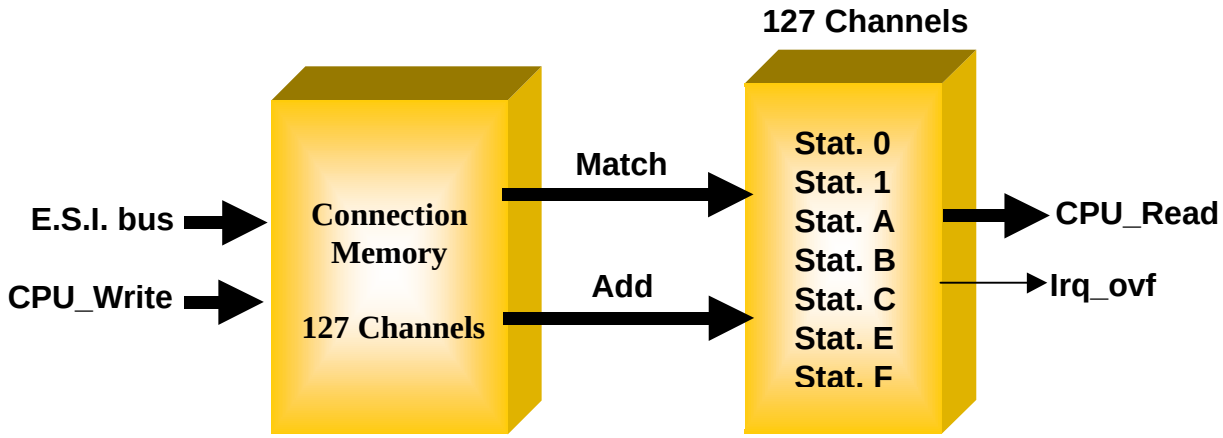
MESC_PM1 Controller MACRO



1.3 Pin Description

Signal	Direction	Activity	Description
CK50	Input	R edge	FPGA system clock. Must be connected to APC ESCLK signal.
RESETN	Input	Low	FPGA system asynchronous reset.
CSN	Input	Low	FPGA chip select.
RWN	Input	-	FPGA read write. 1 => Read. 0 => Write.
ADDRESS(10:0)	Input	High	FPGA address lines.
DATA(31:0)	Input/output	High	FPGA data lines. Active high.
RDYN	output	Low /ts	FPGA acknowledges write or read data. In three state when not active.
IRQN	output	Low	FPGA interruption in case of overflow. Active low during 80ns.
ESC_SYNC	Input	High	FPGA synchronisation pulse. Must be connected to APC ESSYNC signal.
ESC_TXD(15:0)	Input	High	FPGA ESC data. Must be connected to APC ESTXD signal.

1.4 Functionnal Description



The MESC_PM1 Controller is composed of two main functions.
The first function is a Connection Memory which contains the CPU programmed channel to be monitored. Up to 127 channels can be monitored among the 64k possible connections supported within the APC itself.
The second function contains seven statistic counters for up to 127 channels.
When one match happen between the E.S.I. bus and the Connection Memory on a particular channel, the seven statistic counters of this channel are updated according E.S.I. data.
If one statistic counter roll over, one interruption is generated and one status interrupt register is updated to inform the CPU.
When the CPU reads the statistic counters of a paricular channel, this will reset all the statistic counters associated to this channel (except for Stat.1 which has a specific reset mechanism).

1.5 E.S.I. interface

The MESC_PM1 is only connected to the E.S.I. 16-bits output data bus. The ESSYNC signals is also used to synchronise the frame received from the APC.
All the FPGA is synchronised on the APC ESCLK signals.

The ESI output is a repeating frame of length 34 cycles, which corresponds exactly to an APC internal timeslot. In each timeslot the APC can perform the enqueue of a single cell from the Utopia interface on Ingress. The MESC_PM1 will monitor events associated with this operation.

If the ESSYNC pulse is missing the associated cell will not be processed.

The fields which will be extracted, as a subset of the complete ESI frame, to support the statistics given earlier, are listed below. IE_ relates to Ingress Enqueue events. The position of each field within the frame is also given. Cycles within the ESI frame are numbered 0 to 33, with the high pulse on ESSYNC marking the position of Word 0.

Field	Word	Bits
IE_VCX[15:0]	7	15:0

This is the unique identifier for each enabled connection. A VCX of 0xFFFF is a NULL VCX, ie. no enqueue or dequeue event took place.

Field	Word	Bits
IE_S	4	5

This is the VP Switch flag. When S = 0 the connection is VC switched. When S = 1 the connection is VP switched. Only F5 level PM statistics can be maintained for VC switched connections. Only F4 level PM statistics can be maintained for VP switched connections.

Field	Word	Bits
IE_VPCT[2:0]	4	15:13
IE_VCCT[2:0]	4	12:10

This is the VP or VC cell type. Only user cells will be counted, ie. VPCT = 001 when S = 1, or VCCT = 001 when S = 0.

Field	Word	Bits
IE_OpCode[3:0]	24	15:12
IE_ErrCode[3:0]	24	11:8

This is the Ingress Enqueue Operation Code and Error Code. IE_OpCode = 0000 indicates a regular operation. IE_ErrCode = 0000 indicates a valid cell on a valid connection.

Field	Word	Bits
PM_PMX[6:0]	12	14:8
PM_BLER01[7:0]	12	7:0
PM_TUCD01[15:0]	13	15:0

These are the Performance Monitoring results. The PM_PMX is the index to one of 127 PM tasks within the APC. The PM_BLER01 is the Block Error Result for the CLP0+1 cell stream. The PM_TUCD01 is the Total User Cell Difference for the CLP0+1 cell stream.

Please refer to APC version 3 data sheet to get more detail.

1.6 Performance Monitor Register

1.6.1 Register Address Map

The state of the CSN, RWN, and ADDRESS(10:0) signals determines which internal register the microprocessor addresses.

All registers access are modulo 32-bits address, i.e. address bit 0 and bit 1 are not used in decoding logic.

CSN	RWN	ADD(10:0)	ACCESS	REGISTER
1	X	xxx\h	Read / Write	No access.
0	0	000\h	Write only	Connection Memory. 000\h => Unused 004\h => Channel 1 …. 1F8\h=> Channel 126 1FC\h=> Channel 127
0	0	200\h	Write only	Error Threshold Divider Register.
0	0	204\h	Write only	Lost Threshold Divider Register.
0	0	208\h	Write only	Misinserted Threshold Divider Register.
0	0	20C\h	Read / Write	Channel Counter read request.
0	1	400\h	Read only	Stat. 0 read register.
0	1	404\h	Read only	Stat. A read register.
0	1	408\h	Read only	Stat. B read register.
0	1	40C\h	Read only	Stat. C read register.
0	1	410\h	Read only	Stat. E read register.
0	1	414\h	Read only	Stat. F read register.
0	1	418\h	Read only	Status Interupt register.
0	1	41C\h	Read only	Stat. 1 read register.

1.6.2 Registers

1.6.2.1 Connection memory

Address = 004\h to 1FC\h.
Write only.

The Connection Memory enables the CPU to program which channel should be monitored. Up to 127 channels among 64k can be programmed. To each channel one block size is associated.

Channel 1 corresponds to address = 004\h,
Channel 127 corresponds to address = 1FC\h.
This correspondence has to be kept in mind when CPU reads channel counter.(See later)

BIT	DESCRIPTION
15..0	Channel number among 64k. FFFF\h => Channel is not activated.
17..16	Block size associated to the channel programmed : 00 : 128 cells 01 : 256 cells 10 : 512 cells 11 : 1024 cells
31:18	Not used.

1.6.2.2 Error Threshold Divider Register

Address = 200\h.
Write only.

The Error Threshold divider register is a 3-bits value which helps with the Block Size value to generate the Error Threshold.

BIT	DESCRIPTION
2..0	Error Threshold divider. 000 : Disable Threshold 001 : Block size / 2 010 : Block size / 4 011 : Block size / 8 100 : Block size / 16 101 : Block size / 32 110 : Block size / 64 111 : Block size / 128
31:3	Not used.

The possible Error Threshold value are :

BLOCK SIZE	Possible Error Threshold Value
00 : 128 cells	1, 2, 4 …….64 or disabled
01 : 256 cells	2, 4, 8 …….128 or disabled
10 : 512 cells	4, 8, 16 … 256 or disabled
11 : 1024 cells	8, 16, 32 ….512 or disabled

If the Error Threshold divider is programmed to 000 it means the comparison with the Error Threshold Value is inhibited. Hence the Ingress CLP0+1 Errored Cells counter (Stat. B) is always incremented when a block is received with errored cells. Conversely, the Ingress Severely Errored Cell Blocks counter (Stat. A) is not incremented regardless of the number of Cells Errored in a given block.

1.6.2.3 Lost Threshold Divider Register

Address = 204\h.
Write only.

The Lost Threshold divider register is a 3-bits value which helps with the Block Size value to generate the Lost Threshold.

BIT	DESCRIPTION
2..0	Lost Threshold divider. 000 : Disable Threshold 001 : Block size / 2 010 : Block size / 4 011 : Block size / 8 100 : Block size / 16 101 : Block size / 32 110 : Block size / 64 111 : Block size / 128
31:3	Not used.

The possible Lost Threshold value are :

BLOCK SIZE	Possible Lost Threshold Value
00 : 128 cells	1, 2, 4 …….64 or disabled
01 : 256 cells	2, 4, 8 …….128 or disabled
10 : 512 cells	4, 8, 16 … 256 or disabled
11 : 1024 cells	8, 16, 32 ….512 or disabled

If the Lost Threshold divider is programmed to 000 it means the comparison with the Lost Threshold Value is inhibited. Hence the Ingress Lost CLP0+1 User Information Cells (Stat. C) is always incremented when a block is received with lost cells. Conversely, the Ingress Severely Errored Cell Blocks counter (Stat. A) is not incremented regardless of the number of Cells Lost in a given block.

1.6.2.4 Misinserted Threshold Divider Register

Address = 208\h.
Write only.

The Misinserted Threshold divider register is a 3-bits value which helps with the Block Size value to generate the Misinserted Threshold.

BIT	DESCRIPTION
2..0	Misinserted Threshold divider. 000 : Disable Threshold 001 : Block size / 2 010 : Block size / 4 011 : Block size / 8 100 : Block size / 16 101 : Block size / 32 110 : Block size / 64 111 : Block size / 128
31:3	Not used.

The possible Misinserted Threshold value are :

BLOCK SIZE	Possible Misinserted Threshold Value
00 : 128 cells	1, 2, 4 …….64 or disabled
01 : 256 cells	2, 4, 8 …….128 or disabled
10 : 512 cells	4, 8, 16 … 256 or disabled
11 : 1024 cells	8, 16, 32 ….512 or disabled

If the Misinserted Threshold divider is programmed to 000 it means the comparison with the Misinserted Threshold Value is inhibited. Hence the Ingress Misinserted CLP0+1 User Information Cells (Stat. E) is always incremented when a block is received with misinserted cells. Conversely, the Ingress Severely Errored Cell Blocks counter (Stat. A) is not incremented regardless of the number of Cells Misinserted in a given block.

1.6.2.5 Channel Counter Read Request Register

Address = 20C\h.
Read Write.

To read the counters (Stat.0, A, B, C, E, F) of a particular channel, the CPU has to set one Read and Reset Request bit 0 to one and write also in the same time the particular channel number. When the Read and Reset Request bit 0 is reset by the FPGA, then the CPU can read the counter values associated with the channel number programmed.

The channel number corresponds to the Connection Memory Address, i.e. channel 1 corresponds to Connection Memory address 004\h.

BIT	DESCRIPTION
6..0	Channel Number : 00\h : Unused 01\h : Channel 1 … 7E\h : Channel 126 7F\h : Channel 127
7	Read and Reset Request Bit 0 (Stat.0, A, B, C, E, F)
8	Read and Reset Request Bit 1 (Stat.1)
9	Mask Interruption bit. 0 => masked / 1 => not masked.
31:10	Not used.

The Statistic 1 is the Ingress Cells Received in Block count. This statistic is required internally to the MESC_PM1 for synchronising the Total Transmitted Cell Counts (Stat.F) to the other PM parameters.
The Total Transmitted Cell Counts (Stat.F) is updated at the end of a PM block.

The Read and Reset Request Bit 1 enables the CPU to read and reset Ingress Cells Received in Block count for a particular channel. This has to be done typically when deactivating a Channel in the connection memory (writing FFFF\h). The possibility to read the Ingress Cells Received in Block count value (Stat.1) is only for debug purpose.

Both Read and Reset Request Bit 1 and 0 can be written in same time.

1.6.2.6 Stat. 1 read register.

Address = 400\h.
Read only.
24-bits Counter.

Ingress Received Cell Blocks (for convenience called - Stat 0)

This counter counts the number of blocks received since the last CPU read.
One CPU read will reset this counter.

BIT	DESCRIPTION
23..0	Stat. 0 read register
31:24	Not used.

1.6.2.7 Stat. A read register.

Address = 404\h.
Read only.
16-bits Counter.

Ingress Severely Errored Cell Blocks. This statistic is listed in Bellcore GR1248-CORE 11/98 Section 7.1.3.2.1, called Stat A.

One CPU read will reset this counter.

BIT	DESCRIPTION
15..0	Stat. A read register
31:16	Not used.

1.6.2.8 Stat. B read register.

Address = 408\h.
Read only.
16-bits Counter.

Ingress CLP0+1 Errored Cells. This statistic is listed in Bellcore GR1248-CORE 11/98 Section 7.1.3.2.1, called Stat B.

One CPU read will reset this counter.

BIT	DESCRIPTION
15..0	Stat. B read register
31:16	Not used.

1.6.2.9 Stat. C read register.

Address = 40C\h.
Read only.
16-bits Counter.

Ingress Lost CLP0+1 User Information Cells. This statistic is listed in Bellcore GR1248-CORE 11/98 Section 7.1.3.2.1, called Stat C.

One CPU read will reset this counter.

BIT	DESCRIPTION
15..0	Stat. C read register
31:16	Not used.

1.6.2.10 Stat. E read register.

Address = 410\h.
Read only.
16-bits Counter.

Ingress Misinserted CLP0+1 User Information Cells. This statistic is listed in Bellcore GR1248-CORE 11/98 Section 7.1.3.2.1, called Stat E.

One CPU read will reset this counter.

BIT	DESCRIPTION
15..0	Stat. E read register
31:16	Not used.

1.6.2.11 Stat. F read register.

Address = 414\h.
Read only.
32-bits Counter.

Ingress Total Transmitted CLP0+1 User Information Cells. This statistic is listed in Bellcore GR1248-CORE 11/98 Section 7.1.3.2.1, called Stat F.

One CPU read will reset this counter.

BIT	DESCRIPTION
31..0	Stat. F read register

1.6.2.12 Status Interupt register.

Address = 418\h.
Read only.

When one interruption is generated, this register identifies which Channel counter has rolled over.
One CPU read will reset the register.

BIT	DESCRIPTION
6..0	0 : Stat. 0 Counter 1 : Stat. 1 Counter 2 : Stat. A Counter 3 : Stat. B Counter 4 : Stat. C Counter 5 : Stat. E Counter 6 : Stat. F Counter
13:7	Channel number .
31:14	Not used.

1.6.2.13 Stat. 0 read register.

Address = 41C\h.
Read only.
12-bits Counter.

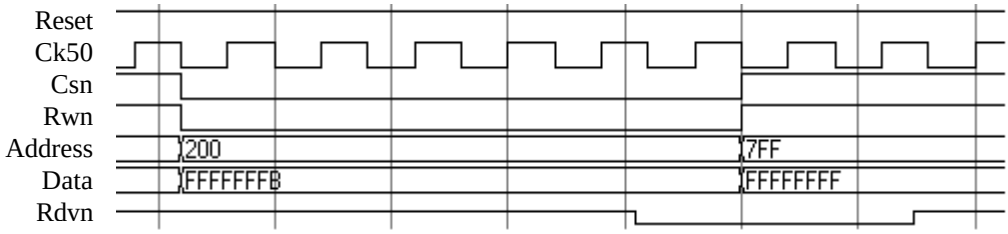
Ingress CLP0+1 Cells Received in current Block (for convenience called - Stat 0)

One CPU read will reset this counter.

BIT	DESCRIPTION
11..0	Stat. 0 read register
31:12	Not used.

1.7 Write cycle

The following chronogram describes the write cycle :

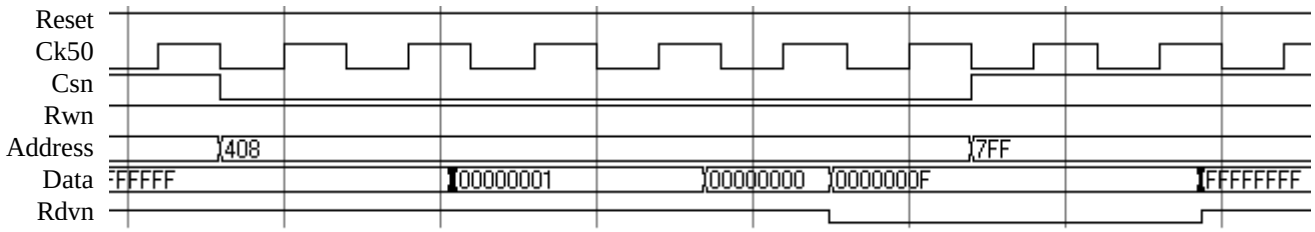


All the Cpu signals are re-synchronised with the Ck50 (APC esclk signal clock) clock signal.

The Rwn, Data and Address signals are only valid when the Csn signal is active low. The Csn, Rwn, Data and Address signals
should stay stable until the Rdyn signal goes low.
When the Rdyn signal goes low, it means the data has been written in the FPGA.
The Rdyn signal stays low until the Csn signal goes high again.
The Rdyn signal is in thee-state by default.

1.8 Read cycle

The following chronogram describes the read cycle :



All the Cpu signals are re-synchronised with the Ck50 (APC esclk signal clock) clock signal.

The Rwn, Data and Address signals are only valid when the Csn signal is active low. The Csn, Rwn, Data and Address signals should stay stable until the Rdyn signal goes low.
When the Rdyn signal goes low, it means the data can be sampled by the CPU.
The Rdyn signal stays low and the data stay valid until the Csn signal goes high again.
The Rdyn signal is in thee-state by default.

1.9 FPGA Timing

The ORCA 3T80-7-S208 respect the following timing :

- FPGA Clock_to_Out = 8 ns (refer to external clock).
- FPGA Input setup time = 8 ns (refer to external clock).
- FPGA Hold time = 1 ns (refer to external clock).
- External Frequency = 50MHz (20ns period).

2. Tool version used

The Macro has been done with a P.C. on Windows N.T. 4 and with the following version tool :

- Synthesis tool : Leonardo Spectrum level 2 V1999.1h from Exemplar.
- Place and Route tool : Orca Foundry V9.4 production, from Lucent technologies.
- VHDL Simulation tool : ModelSim PE V5.3b

Every tool has been used with its GUI.

3. Recommended Design Experience

Designers should be familiar with APC device, VHDL, synthesis tools, ORCA Foundry data flow and VHDL simulation software. Experience with microprocessor is recommended. The macro can easily be integrated into hierarchical VHDL designs.

4. Available Support Products

Support products available from Logic Design Solutions.

5. Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers macro integration and design services on FPGA.
Logic Design Solutions macros are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

6. Related Information

Lucent Programmable Logic

For information on Lucent programmable logic or development system software, please contact your local Lucent sales office.
WEB: http://www.lucent.com/micro

Logic Design Solutions

48 Allée des Coteaux B2 – 93340 Le Raincy – France.
Phone : +33 (0) 1 43 01 42 44
Fax : +33 (0) 1 43 81 20 21
E-mail : info@logic-design-solutions.com
WEB: http://www.logic-design-solutions.com