National Semiconductor

MM54HCT138/MM74HCT138
3-to-8 Line Decoder

General Description

This decoder utilizes advanced silicon-gate CMOS technology, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM54HCT138/MM74HCT138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, G2A and G2B) are provided to ease the cascading decoders.

The decoders' output can drive 10 low power Schottky TTL equivalent loads and are functionally and pin equivalent to

the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features
- TTL input compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
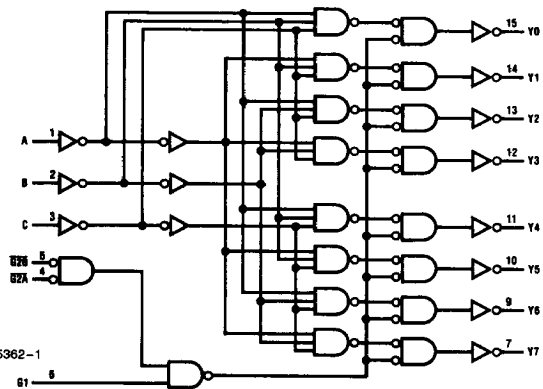- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

SELECT   ENABLE   OUTPUT

TOP VIEW
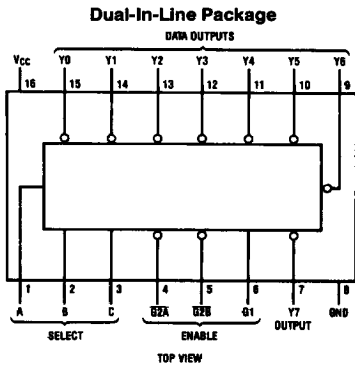
Order Number MM54HCT138*
or MM74HCT138*

*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram

TL/F/5362-1

TL/F/5362-2

Truth Table

Inputs				Outputs							
Enable		Select									
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$ H = high level L = low level X = don't care

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to $+7.0$V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC}+1.5$V
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC}+0.5$V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	-40	$+85$	°C
MM54HCT	-55	$+125$	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC}=5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$|I_{OUT}|=20\,\mu A$	V_{CC}	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$	V
		$|I_{OUT}|=4.0$ mA, $V_{CC}=4.5$V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|=4.8$ mA, $V_{CC}=5.5$V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$|I_{OUT}|=20\,\mu A$	0	0.1	0.1	0.1	V
		$|I_{OUT}|=4.0$ mA, $V_{CC}=4.5$V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|=4.8$ mA, $V_{CC}=5.5$V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\,\mu A$		8.0	80	160	μA
		$V_{IN}=2.4$V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input pin. All other inputs are held at V_{CC} or ground.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, A, B, or C to Output		20	35	ns
t_{PLH}	Maximum Propagation Delay, A, B, or C to Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, G1 to Y Output		14	25	ns
t_{PLH}	Maximum Propagation Delay, G1 to Y Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		17	30	ns
t_{PLH}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		13	25	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25°C$ Typ	74HCT $T_A = -40$ to 85°C	54HCT $T = -55$ to 125°C	Units
				Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay A, B, or C to Output		24	40	50	60	ns
t_{PLH}	Maximum Propagation Delay A, B, or C to Output		18	30	38	45	ns
t_{PHL}	Maximum Propagation Delay G1 to Y Output		17	30	38	45	ns
t_{PLH}	Maximum Propagation Delay G1 to Y Output		20	30	38	45	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		23	35	43	52	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		18	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{IN}	Input Capacitance			5	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)	55				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

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