S6B0723

132 SEG / 65 COM DRIVER & CONTROLLER FOR STN LCD

June. 2000.

Ver. 0.9

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S6B0723 Specification Revision History		
Version	**Content**	**Date**
0.0	Initial version	1998
0.1	1. V_{DD} level changed(1.8V ~ 3.6V → 2.4V ~ 5.5V) 2. Power save mode changed (compound instruction) 3. Oscillator ON command deleted 4. Vref voltage changed (1.4V → 2.1 V) 5. Internal resistor (Ra / Rb) ratio changed 6. n-line inversion deleted	Mar.1999
0.2	1. PAD name changed (VSS → TEST4)	Mar.1999
0.3	1. Eq2. changed (page 32)	Mar.1999
0.4	1. figure 10. figure 11. changed	Mar.1999
0.5	1. Set static indicator register changed (page 46)	Apr.1999
0.6	1. Modify following sections Introduction, Features, Pad Configuration, Pin Description, Power Supply Circuits, Reference Circuit Examples, DC/AC Characteristics, Connection Between S6B0723 and LCD Panel	Apr.1999
0.7	1. S6B0723 Application circuit is changed(page 65~67)	Aug.1999
0.8	1. Operating VDD range is changed	Oct.1999
0.9	1. READ timing is changed(Figure 5)	Jun.2000

CONTENTS

INTRODUCTION

The S6B0723 is a single-chip driver & controller LSI for graphic dot-matrix liquid crystal display systems. This chip can be connected directly to a microprocessor, accepts serial or 8-bit parallel display data from the microprocessor, stores the display data in an on-chip display data RAM of 65 x 132 bits and generates a liquid crystal display drive signal independent of the microprocessor. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. It contains 65 common driver circuits and 132 segment driver circuits, so that a single chip can drive a 65 x 132 dot display. And the capacity of the display can be increased through the use of master/slave multi-chip structures. This chip is able to minimize power consumption because it performs display data RAM read/write operation with no external operation clock. In addition, because it contains power supply circuits necessary to drive liquid crystal, which is a display clock oscillator circuit, high performance voltage converter circuit, high-accuracy voltage regulator circuit, low power consumption voltage divider resistors and OP-Amp for liquid crystal driver power voltage, it is possible to make the lowest power consumption display system with the fewest components for high performance portable systems.

FEATURES

Display Driver Output Circuits

– 65 common outputs / 132 segment outputs

On-chip Display Data RAM

– Capacity: 65 x 132 = 8,580 bits
– RAM bit data "1": a dot of display is illuminated.
– RAM bit data "0": a dot of display is not illuminated.

Applicable Duty Ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/65	1/7 or 1/9	65 × 132
1/55	1/6 or 1/8	55 × 132
1/49	1/6 or 1/8	49 × 132
1/33	1/5 or 1/6	33 × 132

Microprocessor Interface

– High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface (only write operation) available

Various Function Set

– Display ON / OFF, set initial display line, set page address, set column address, read status, write / read display data, select segment driver output, reverse display ON / OFF, entire display ON / OFF, select LCD bias, set/reset modify-read, select common driver output, control display power circuit, select internal regulator resistor ratio for V0 voltage regulation, electronic volume, set static indicator state.
– H/W and S/W reset available
– Static drive circuit equipped internally for indicators with 4 flashing modes

Built-in Analog Circuit

- On-chip oscillator circuit for display clock (external clock can also be used)
- High performance voltage converter (with booster ratios of x2, x3, x4 and x5, where the step-up reference voltage can be used externally)
- High accuracy voltage regulator (temperature coefficient: -0.05%/°C or external input)
- Electronic contrast control function (64 steps)
- Vref = 2.1V ± 3% (V0 voltage adjustment voltage)
- High performance voltage follower (V1 to V4 voltage divider resistors and OP-Amp for increasing drive capacity)

Operating Voltage Range

- Supply voltage (V_{DD}): 2.4 to 3.6V
- LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.5 to 15.0V

Low Power Consumption

- Operating power: 40μA typical (conditions: V_{DD} = 3V, x 4 boosting (VCI = V_{DD}), V0 = 11V, Internal power supply ON, display OFF and normal mode is selected)
- Standby power: 10 μA maximum (during power save[standby] mode)

Operating Temperatures

- Wide range of operating temperatures : -40 to 85°C

CMOS Process

Package Type

- TCP

BLOCK DIAGRAM

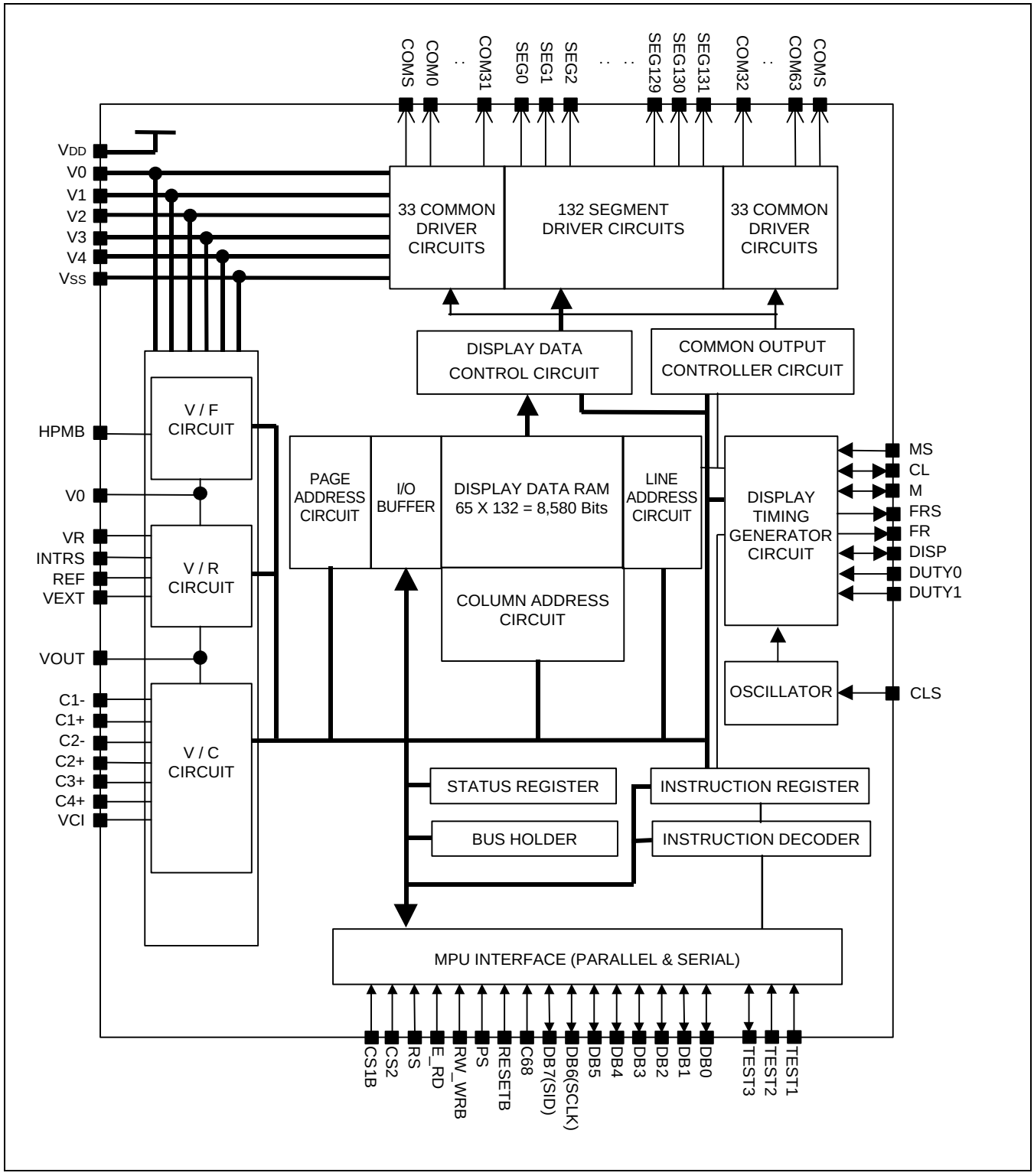


Figure 1. Block Diagram

PAD CONFIGURATION

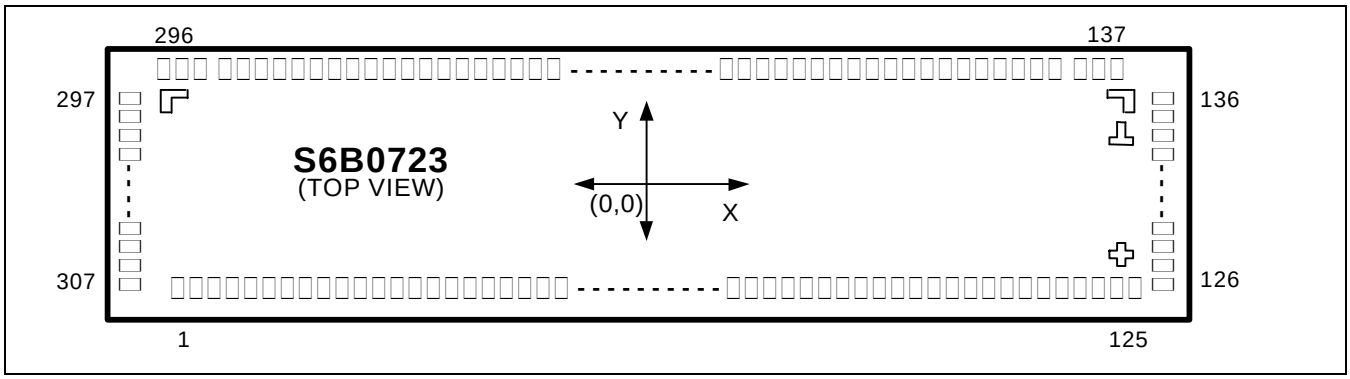
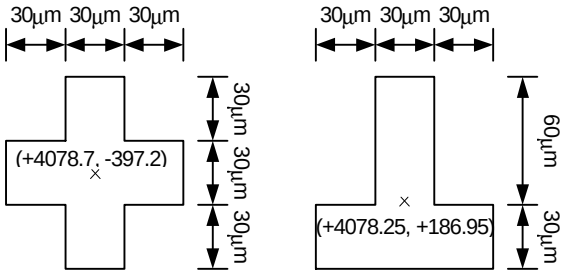


Figure 2. S6B0723 Chip Configuration

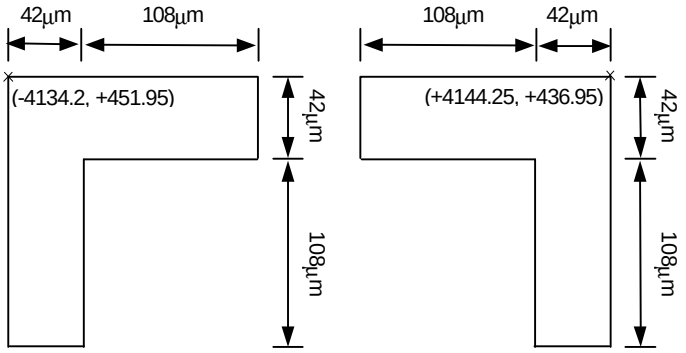
Table 1. S6B0723 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	8850	1980	µm
Pad pitch	151 to 282	52		
	2 to 21, 105 to 124 138 to 150, 283 to 295	55		
	22 to 104	70		
	150 to 151, 282 to 283	75		
	1 to 2, 124 to 125 137 to 138, 295 to 296	80		
	126 to 136, 297 to 307	150		
	21 to 22, 104 to 105	226		
Bumped pad size (Bottom)	1, 125, 137, 296	62	70	
	2 to 21, 105 to 124 138 to 150, 283 to 295	34	70	
	151 to 282	34	70	
	22 to 104	52	70	
	126 to 136, 297 to 307	38	70	
Bumped pad height	All pad	14 (Typ.)		

COG Align Key Coordinate



ILB Align Key Coordinate



SAMSUNG ELECTRONICS

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	DUMMY	-4221	-865	51	DUTY0	-840	-865	101	HPMB	2660	-865
2	COM45	-4141	-865	52	DUTY1	-770	-865	102	VSS	2730	-865
3	COM46	-4086	-865	53	VSS	-700	-865	103	INTRS	2800	-865
4	COM47	-4031	-865	54	VDD	-630	-865	104	VDD	2870	-865
5	COM48	-3976	-865	55	VDD	-560	-865	105	COM31	3096	-865
6	COM49	-3921	-865	56	VDD	-490	-865	106	COM30	3151	-865
7	COM50	-3866	-865	57	VCI	-420	-865	107	COM29	3206	-865
8	COM51	-3811	-865	58	VCI	-350	-865	108	COM28	3261	-865
9	COM52	-3756	-865	59	VSS	-280	-865	109	COM27	3316	-865
10	COM53	-3701	-865	60	VSS	-210	-865	110	COM26	3371	-865
11	COM54	-3646	-865	61	VSS	-140	-865	111	COM25	3426	-865
12	COM55	-3591	-865	62	VOUT	-70	-865	112	COM24	3481	-865
13	COM56	-3536	-865	63	VOUT	0	-865	113	COM23	3536	-865
14	COM57	-3481	-865	64	C4+	70	-865	114	COM22	3591	-865
15	COM58	-3426	-865	65	C4+	140	-865	115	COM21	3646	-865
16	COM59	-3371	-865	66	C3+	210	-865	116	COM20	3701	-865
17	COM60	-3316	-865	67	C3+	280	-865	117	COM19	3756	-865
18	COM61	-3261	-865	68	C1-	350	-865	118	COM18	3811	-865
19	COM62	-3206	-865	69	C1-	420	-865	119	COM17	3866	-865
20	COM63	-3151	-865	70	C1+	490	-865	120	COM16	3921	-865
21	COMS	-3096	-865	71	C1+	560	-865	121	COM15	3976	-865
22	FRS	-2870	-865	72	C2+	630	-865	122	COM14	4031	-865
23	FR	-2800	-865	73	C2+	700	-865	123	COM13	4086	-865
24	TEST1	-2730	-865	74	C2-	770	-865	124	COM12	4141	-865
25	TEST2	-2660	-865	75	C2-	840	-865	125	DUMMY	4221	-865
26	TEST3	-2590	-865	76	VDD	910	-865	126	DUMMY	4345	-750
27	M	-2520	-865	77	VEXT	980	-865	127	DUMMY	4345	-600
28	CL	-2450	-865	78	REF	1050	-865	128	DUMMY	4345	-450
29	DISP	-2380	-865	79	VSS	1120	-865	129	DUMMY	4345	-300
30	TEST4	-2310	-865	80	V1	1190	-865	130	DUMMY	4345	-150
31	VSS	-2240	-865	81	V1	1260	-865	131	DUMMY	4345	0
32	CS1B	-2170	-865	82	V2	1330	-865	132	DUMMY	4345	150
33	CS2	-2100	-865	83	V2	1400	-865	133	DUMMY	4345	300
34	VDD	-2030	-865	84	V3	1470	-865	134	DUMMY	4345	450
35	RESETB	-1960	-865	85	V3	1540	-865	135	DUMMY	4345	600
36	RS	-1890	-865	86	V4	1610	-865	136	DUMMY	4345	750
37	VSS	-1820	-865	87	V4	1680	-865	137	DUMMY	4221	865
38	RW_WRB	-1750	-865	88	V0	1750	-865	138	COM11	4141	865
39	E_RDB	-1680	-865	89	V0	1820	-865	139	COM10	4086	865
40	VDD	-1610	-865	90	VR	1890	-865	140	COM9	4031	865
41	DB0	-1540	-865	91	VR	1960	-865	141	COM8	3976	865
42	DB1	-1470	-865	92	VSS	2030	-865	142	COM7	3921	865
43	DB2	-1400	-865	93	VSS	2100	-865	143	COM6	3866	865
44	DB3	-1330	-865	94	VDD	2170	-865	144	COM5	3811	865
45	DB4	-1260	-865	95	MS	2240	-865	145	COM4	3756	865
46	DB5	-1190	-865	96	CLS	2310	-865	146	COM3	3701	865
47	DB6	-1120	-865	97	VSS	2380	-865	147	COM2	3646	865
48	DB7	-1050	-865	98	C68	2450	-865	148	COM1	3591	865
49	VSS	-980	-865	99	PS	2520	-865	149	COM0	3536	865
50	VDD	-910	-865	100	VDD	2590	-865	150	COMS	3481	865

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
151	SEG0	3406	865	201	SEG50	806	865	251	SEG100	-1794	865
152	SEG1	3354	865	202	SEG51	754	865	252	SEG101	-1846	865
153	SEG2	3302	865	203	SEG52	702	865	253	SEG102	-1898	865
154	SEG3	3250	865	204	SEG53	650	865	254	SEG103	-1950	865
155	SEG4	3198	865	205	SEG54	598	865	255	SEG104	-2002	865
156	SEG5	3146	865	206	SEG55	546	865	256	SEG105	-2054	865
157	SEG6	3094	865	207	SEG56	494	865	257	SEG106	-2106	865
158	SEG7	3042	865	208	SEG57	442	865	258	SEG107	-2158	865
159	SEG8	2990	865	209	SEG58	390	865	259	SEG108	-2210	865
160	SEG9	2938	865	210	SEG59	338	865	260	SEG109	-2262	865
161	SEG10	2886	865	211	SEG60	286	865	261	SEG110	2314	865
162	SEG11	2834	865	212	SEG61	234	865	262	SEG111	-2366	865
163	SEG12	2782	865	213	SEG62	182	865	263	SEG112	-2418	865
164	SEG13	2730	865	214	SEG63	130	865	264	SEG113	-2470	865
165	SEG14	2678	865	215	SEG64	78	865	265	SEG114	-2522	865
166	SEG15	2626	865	216	SEG65	26	865	266	SEG115	-2574	865
167	SEG16	2574	865	217	SEG66	-26	865	267	SEG116	-2626	865
168	SEG17	2522	865	218	SEG67	-78	865	268	SEG117	-2678	865
169	SEG18	2470	865	219	SEG68	-130	865	269	SEG118	-2730	865
170	SEG19	2418	865	220	SEG69	-182	865	270	SEG119	-2782	865
171	SEG20	2366	865	221	SEG70	-234	865	271	SEG120	-2834	865
172	SEG21	2314	865	222	SEG71	-286	865	272	SEG121	-2886	865
173	SEG22	2262	865	223	SEG72	-338	865	273	SEG122	-2938	865
174	SEG23	2210	865	224	SEG73	-390	865	274	SEG123	-2990	865
175	SEG24	2158	865	225	SEG74	-442	865	275	SEG124	-3042	865
176	SEG25	2106	865	226	SEG75	-494	865	276	SEG125	-3094	865
177	SEG26	2054	865	227	SEG76	-546	865	277	SEG126	-3146	865
178	SEG27	2002	865	228	SEG77	-598	865	278	SEG127	-3198	865
179	SEG28	1950	865	229	SEG78	-650	865	279	SEG128	-3250	865
180	SEG29	1898	865	230	SEG79	-702	865	280	SEG129	-3302	865
181	SEG30	1846	865	231	SEG80	-754	865	281	SEG130	-3354	865
182	SEG31	1794	865	232	SEG81	-806	865	282	SEG131	-3406	865
183	SEG32	1742	865	233	SEG82	-858	865	283	COM32	-3481	865
184	SEG33	1690	865	234	SEG83	-910	865	284	COM33	-3536	865
185	SEG34	1638	865	235	SEG84	-962	865	285	COM34	-3591	865
186	SEG35	1586	865	236	SEG85	-1014	865	286	COM35	-3646	865
187	SEG36	1534	865	237	SEG86	-1066	865	287	COM36	-3701	865
188	SEG37	1482	865	238	SEG87	-1118	865	288	COM37	-3756	865
189	SEG38	1430	865	239	SEG88	-1170	865	289	COM38	-3811	865
190	SEG39	1378	865	240	SEG89	-1222	865	290	COM39	-3866	865
191	SEG40	1326	865	241	SEG90	-1274	865	291	COM40	-3921	865
192	SEG41	1274	865	242	SEG91	-1326	865	292	COM41	-3976	865
193	SEG42	1222	865	243	SEG92	-1378	865	293	COM42	-4031	865
194	SEG43	1170	865	244	SEG93	-1430	865	294	COM43	-4086	865
195	SEG44	1118	865	245	SEG94	-1482	865	295	COM44	-4141	865
196	SEG45	1066	865	246	SEG95	-1534	865	296	DUMMY	-4221	865
197	SEG46	1014	865	247	SEG96	–1586	865	297	DUMMY	-4345	750
198	SEG47	962	865	248	SEG97	-1638	865	298	DUMMY	-4345	600
199	SEG48	910	865	249	SEG98	-1690	865	299	DUMMY	-4345	450
200	SEG49	858	865	250	SEG99	-1742	865	300	DUMMY	-4345	300

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
301	DUMMY	-4345	150								
302	DUMMY	-4345	0								
303	DUMMY	-4345	-150								
304	DUMMY	-4345	-300								
305	DUMMY	-4345	-450								
306	DUMMY	-4345	-600								
307	DUMMY	-4345	-750								

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/9 bias</td><td>(8/9) x V0</td><td>(7/9) x V0</td><td>(2/9) x V0</td><td>(1/9) x V0</td></tr>
<tr><td>1/8 bias</td><td>(7/8) x V0</td><td>(6/8) x V0</td><td>(2/8) x V0</td><td>(1/8) x V0</td></tr>
<tr><td>1/7 bias</td><td>(6/7) x V0</td><td>(5/7) x V0</td><td>(2/7) x V0</td><td>(1/7) x V0</td></tr>
<tr><td>1/6 bias</td><td>(5/6) x V0</td><td>(4/6) x V0</td><td>(2/6) x V0</td><td>(1/6) x V0</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table></td></tr>
</table>

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pins Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
C4+	O	Capacitor 4 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input/output pin Connect this pin to V_{SS} through capacitor.
VR	I	V0 voltage adjustment pin It is valid only when internal voltage regulator resistors are not used (INTRS = "L").
VCI	I	This is the reference voltage for the voltage converter circuit for the LCD driving. Whether internal voltage converter use or not use, this pin should be fixed. The voltage should have the following range: 2.4V ≤ VCI ≤ 3.6V
VEXT	I	This is the external-input reference voltage (V_{REF}) for the internal voltage regulator. It is valid only when external V_{REF} is used (REF = "L"). When using internal V_{REF}, this pin is Open
REF	I	Select the external V_{REF} voltage via VEXT pin – REF = "L": using the external V_{REF} – REF = "H": using the internal V_{REF}

SYSTEM CONTROL

Table 5. System Control Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MS</td><td>I</td><td>Master / slave mode select input
Master makes some signals for display, and slave gets them. This is for display synchronization.
– MS = "H": master mode
– MS = "L": slave mode
The following table depends on the MS status.
<table>
<tr><th>MS</th><th>CLS</th><th>OSC circuit</th><th>Power supply circuit</th><th>CL</th><th>M</th><th>FR</th><th>DISP</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>-</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin
– CLS = “H”: enable
– CLS = “L”: disable (external display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin
When the S6B0723 is used in master/slave mode (multi-chip), the CL pins must be connected each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC Signal input / output pin
When the S6B0723 is used in master/slave mode (multi-chip), the M pins must be connected each other.
– MS = “H”: output
– MS = “L”: input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin
This pin is used together with the FR pin.</td></tr>
<tr><td>FR</td><td>O</td><td>Static driver common output pin
This pin is used together with the FRS pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input / output
When S6B0723 is used in master/slave mode (multi-chip), the DISP pins must be connected each other.
– MS = “H”: output
– MS = “L”: input</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistor select pin
This pin selects the resistors for adjusting V0 voltage level and is valid only in master operation.
– INTRS = "H": use the internal resistors.
– INTRS = "L": use the external resistors.
V0 voltage is controlled by VR pin and external resistive divider.</td></tr>
</table>

Table 5. System Control Pins Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td rowspan="8">DUTY0
DUTY1</td><td rowspan="8">I</td><td colspan="3">The LCD driver duty ratio depends on the following table.</td></tr>
<tr><td>DUTY1</td><td>DUTY0</td><td>Duty ratio</td></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L</td><td>1/55</td></tr>
<tr><td>H</td><td>H</td><td>1/65</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td>HPMB</td><td>I</td><td colspan="3">Power control pin of the power supply circuits for LCD driver.
– HPMB = "H": normal mode
– HPMB = "L": high power mode
This pin is valid only in master operation.</td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is "L", initialization is executed.</td></tr>
<tr><td rowspan="5">PS</td><td rowspan="5">I</td><td>Parallel / Serial data input select input
<table>
<tr><td>PS</td><td>Interface mode</td><td>Chip select</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RDB
RW_WRB</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
</table>
</td></tr>
<tr><td>*NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RDB and RW_WRB must be fixed to either "H" or "L".</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor interface select input pin in parallel mode
– C68 = "H": 6800-series MPU interface
– C68 = "L": 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CS1B is "L" and CS2 is "H". When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="4">RW_WRB</td><td rowspan="4">I</td><td>Read / Write execution control pin
<table>
<tr><td>C68</td><td>MPU Type</td><td>RW_WRB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
– RW = "H": read
– RW = "L": write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WRB</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.</td></tr>
</table>
</td></tr>
<tr><td></td></tr>
</table>

Table 6. Microprocessor Interface Pins Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RDB</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU Type</td><td>E_RDB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
– RW = "H": When E is "H", DB0 to DB7 are in an output status.
– RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RDB</td><td>Read enable clock input pin
When /RDB is "L", DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>TEST1
to
TEST4</td><td>I/O</td><td colspan="4">These are pins for IC chip testing
They are set to Open.</td></tr>
</table>

NOTE: **DUMMY – These pins should be opened (floated).**

LCD DRIVER OUTPUTS

Table 7. LCD Driver Output Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG131</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">FR</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM63</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>FR</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">Vss</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS</td><td>O</td><td colspan="4">Common output for the icons
The output signals of two pins are same. When not used, these pins should be left Open. In multi-chip (master / slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B0723 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E_RDB, and RW_WRB inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

S6B0723 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 8**.**

Table 8. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*×: Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in table 9. The type of data transfer is determined by signals at RS, E_RDB and RW_WRB as shown in table 10.

Table 9. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RDB	RW_WRB	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RDB	/WRB	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RDB (E)	RW_WRB (RW)	E_RDB (/RDB)	RW_WRB (/WRB)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (PS = "L")

When the S6B0723 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

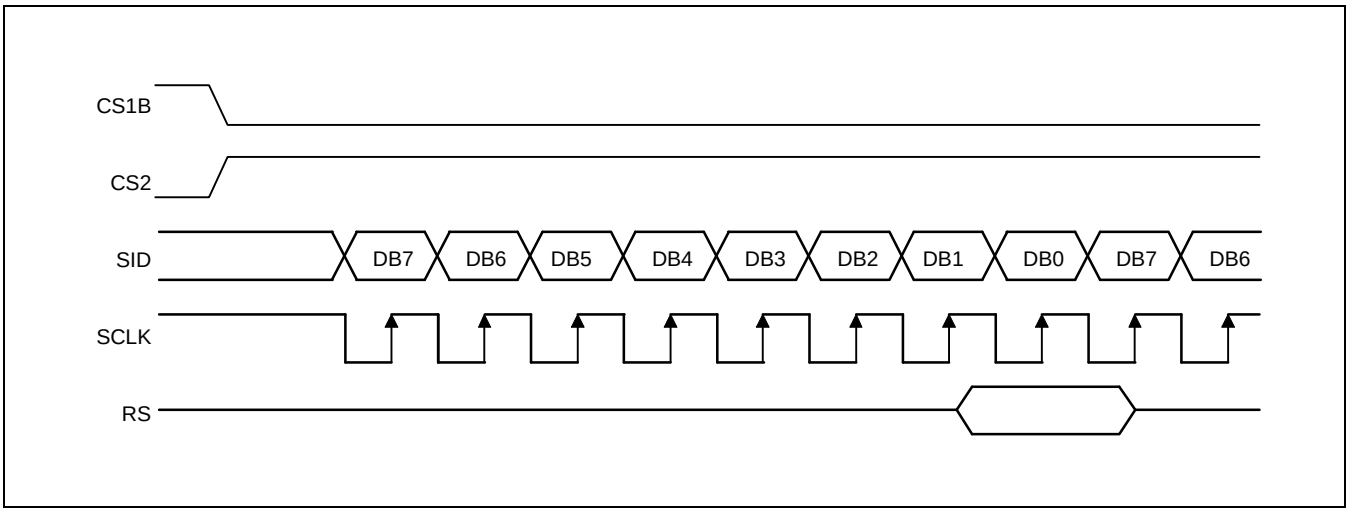


Figure 3. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the S6B0723 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0723 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

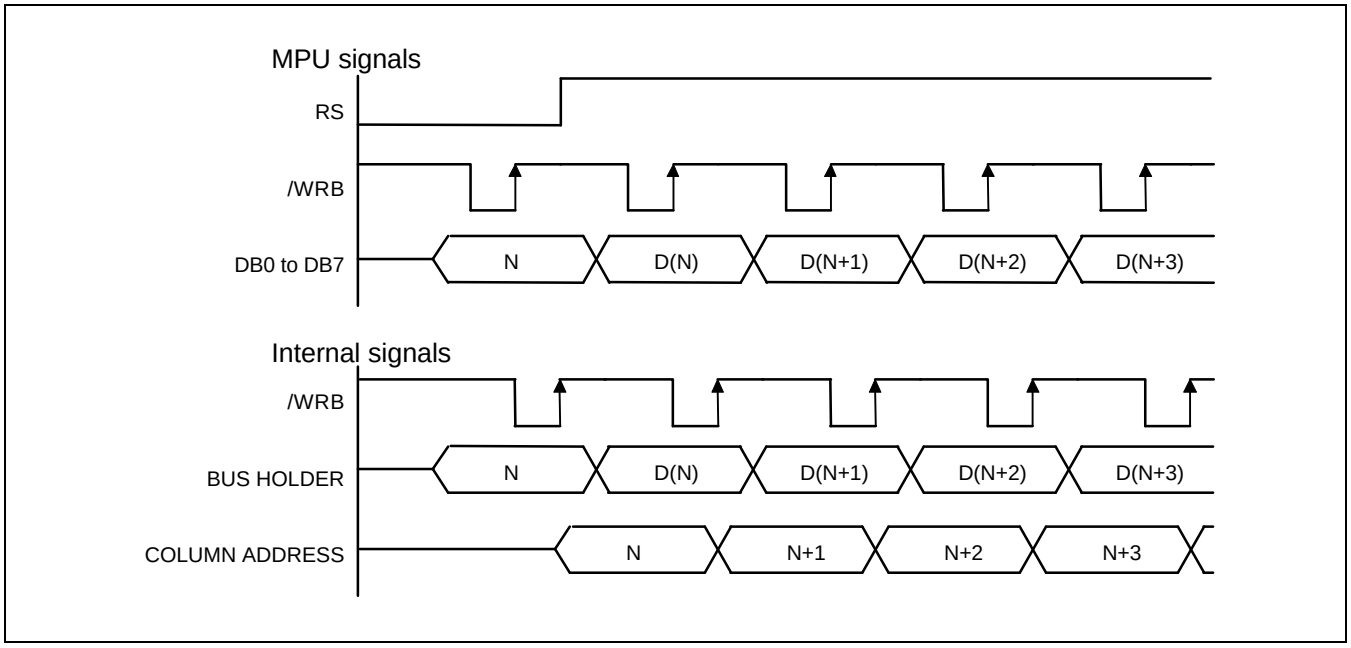


Figure 4. Write Timing

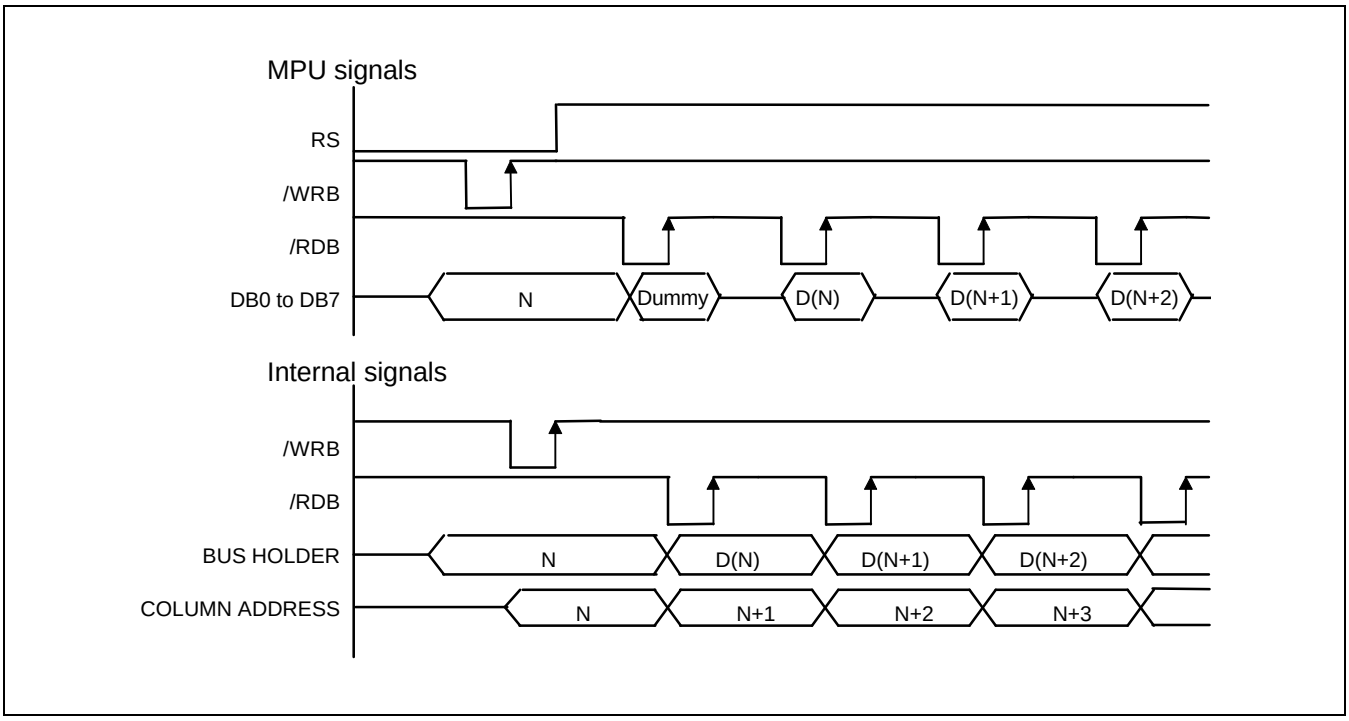


Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

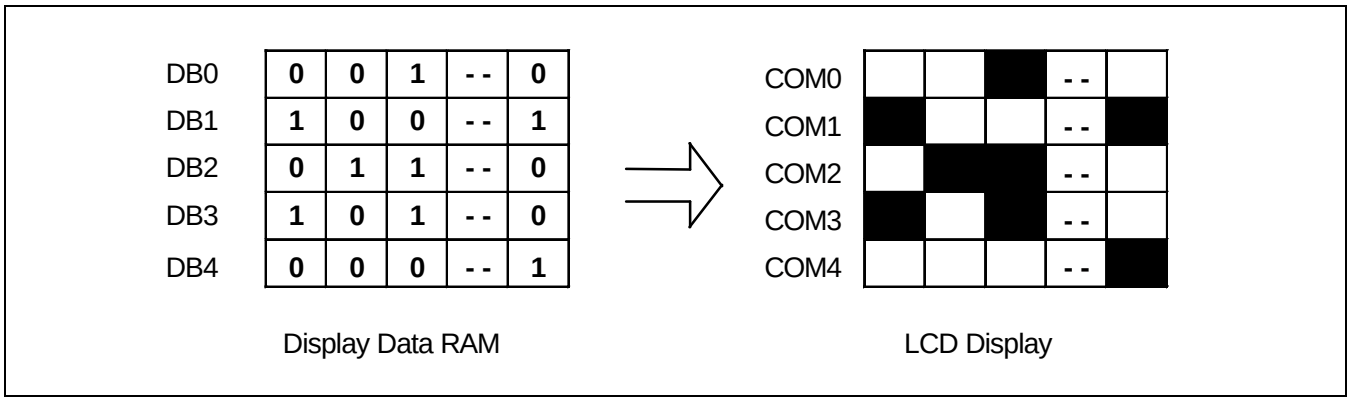


Figure 6. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 8 (DB3 is "H", but DB2, DB1 and DB0 are "L") is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 8. It incorporates 6-bit line address register changed by only the initial display line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column Address circuit has an 8-bit preset counter that provides column address to the Display Data RAM as shown in figure 8. When Set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 7.

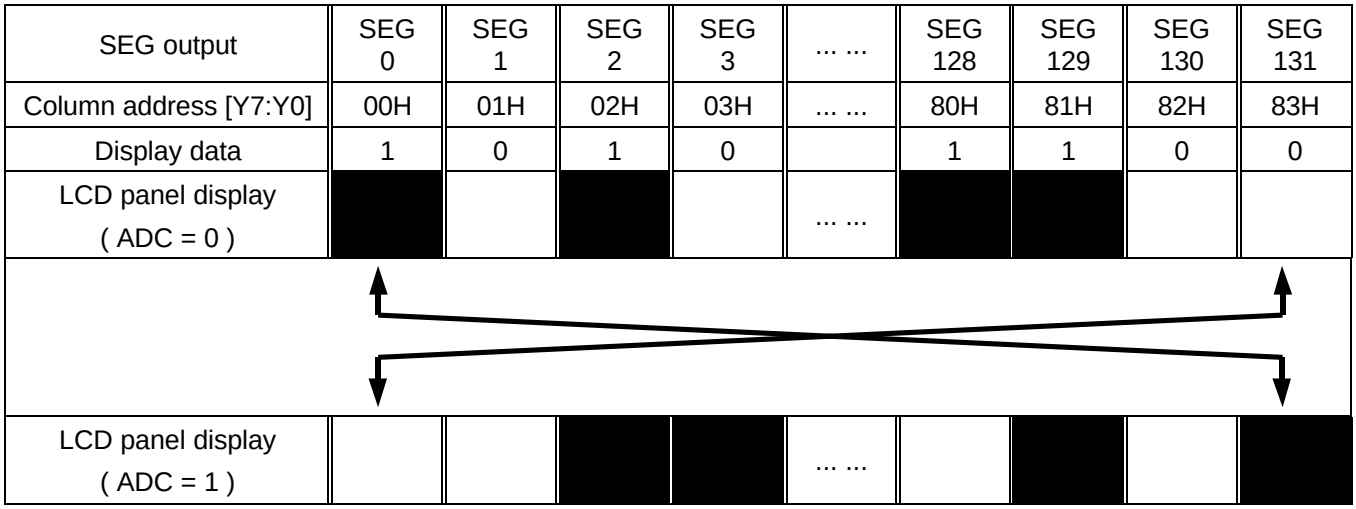
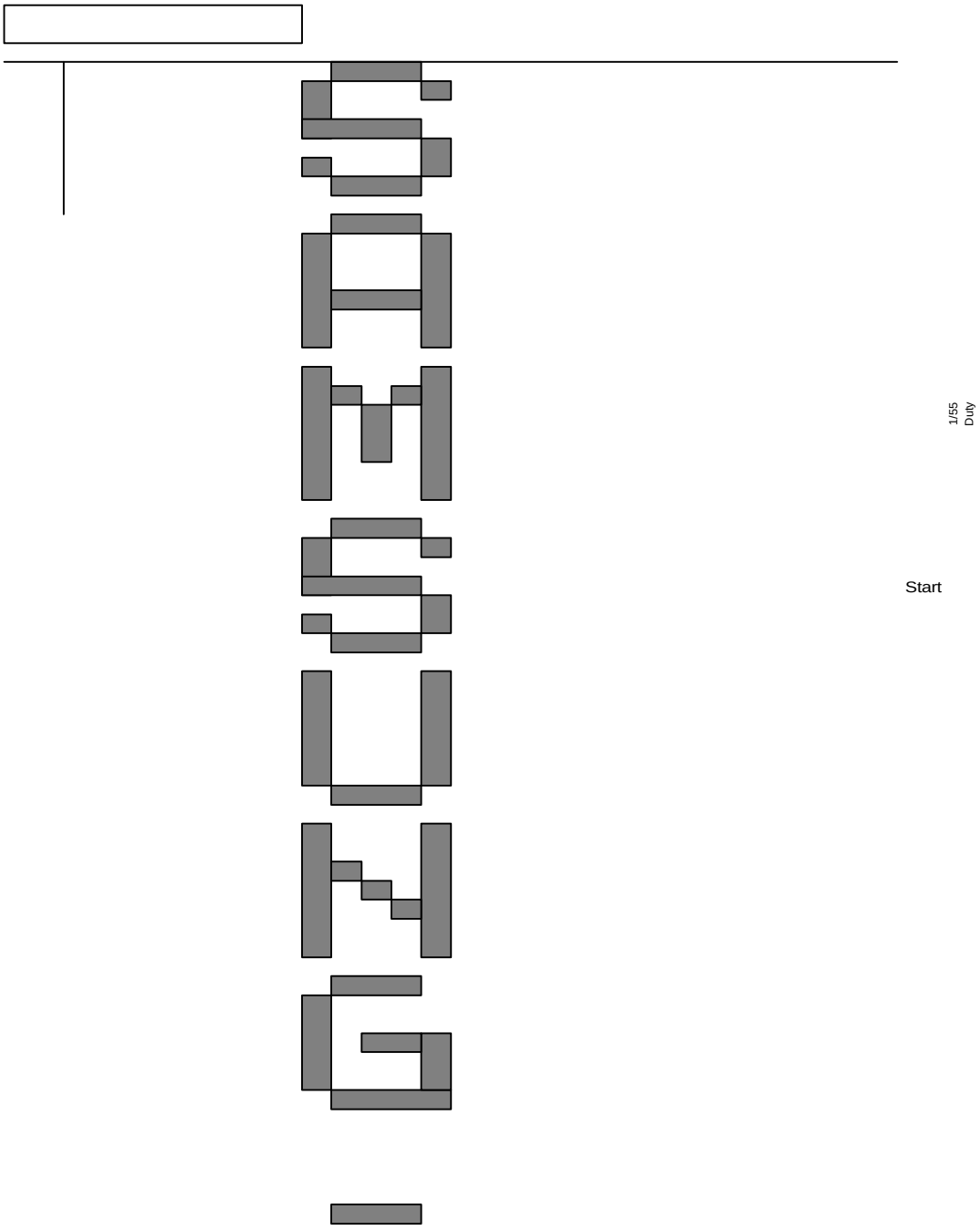


Figure 7. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.


1/55
Duty
Start

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit. The oscillator circuit is only enabled when MS = "H" and CLS = "H". When on-chip oscillator is not used, CLS pin must be "L" condition. In this time, external clock must be input from CL pin.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL generated by oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 132-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The LCD AC signal, M is generated from the display clock. 2-frame AC driver waveforms with internal timing signal are shown in figure 9.

In a multiple chip configuration, the slave chip requires the M, CL and DISP signals from the master. Table 11 shows the M, SYNC, CL, and DISP status.

Table 11. Master and Slave Timing Signal Status

Operation mode	Oscillator	M	CL	DISP
Master	ON (internal clock used)	Output	Output	Output
	OFF (external clock used)	Output	Input	Output
Slave	-	Input	Input	Input

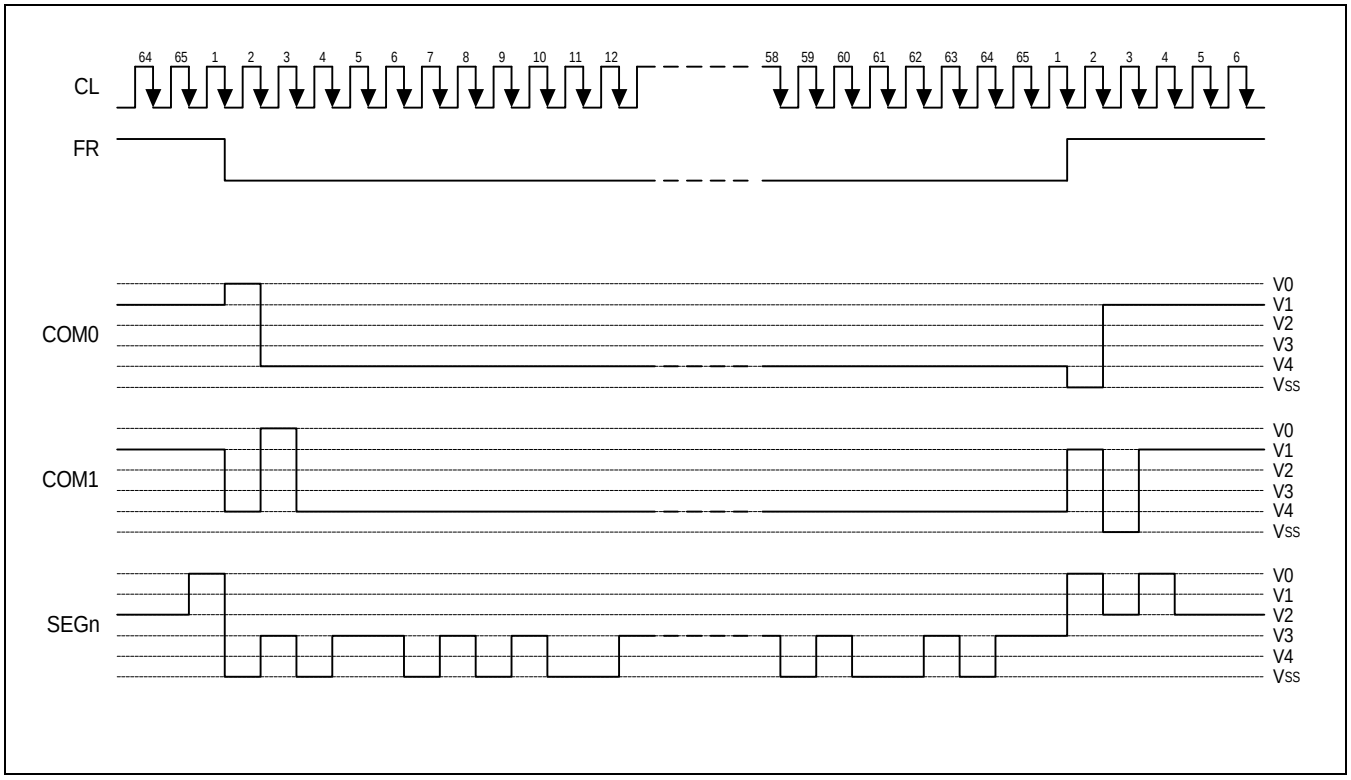


Figure 9. 2-frame AC Driving Waveform (Duty Ratio = 1/65)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL select instruction specifies the scanning direction of the common output pins.

Table 12. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common output pins							
		COM [0:15]	COM [16:23]	COM [24:26]	COM [27:36]	COM [37:39]	COM [40:47]	COM [48:63]	COMS
1/33	0	COM[0:15]	*NC					COM[16:31]	COMS
	1	COM[31:16]	*NC					COM[15:0]	
1/49	0	COM[0:23]		*NC			COM[24:47]		COMS
	1	COM[47:24]		*NC			COM[23:0]		
1/55	0	COM[0:26]			*NC	COM[27:53]			COMS
	1	COM[53:27]			*NC	COM[26:0]			
1/65	0	COM[0:63]							COMS
	1	COM[63:0]							

*NC: No Connection

LCD DRIVER CIRCUITS

This driver circuit is configured by 66-channel (including 2 COMS channels) common driver and 132-channel segment driver. This LCD panel driver voltage depends on the combination of display data and FR signal.

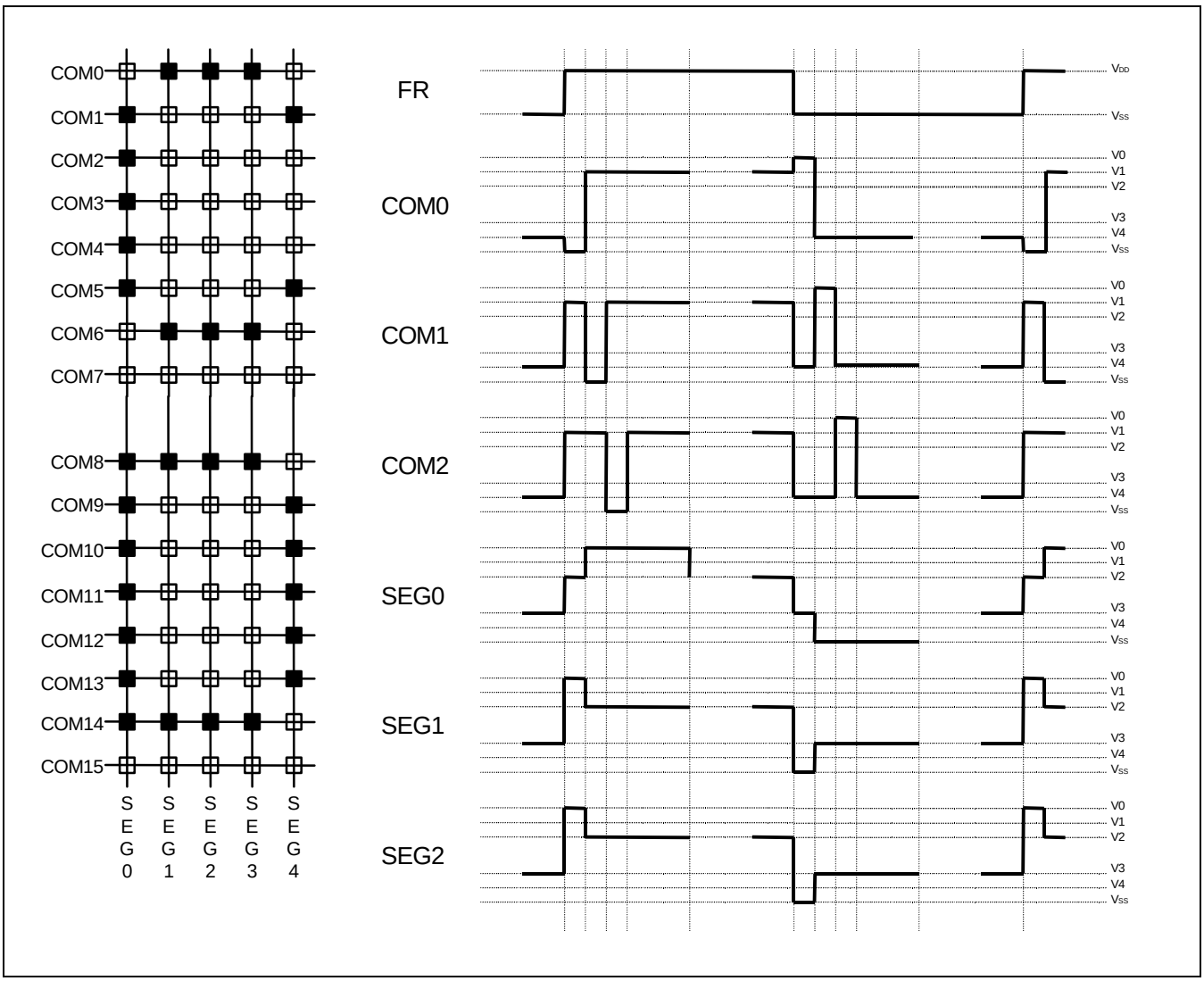


Figure 10. Segment and Common Timing

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 13 shows the referenced combinations in using Power Supply circuits.

Table 13. Recommended Power Supply Combinations

User Setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and VSS to 2, 3, 4, or 5 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7 µF]

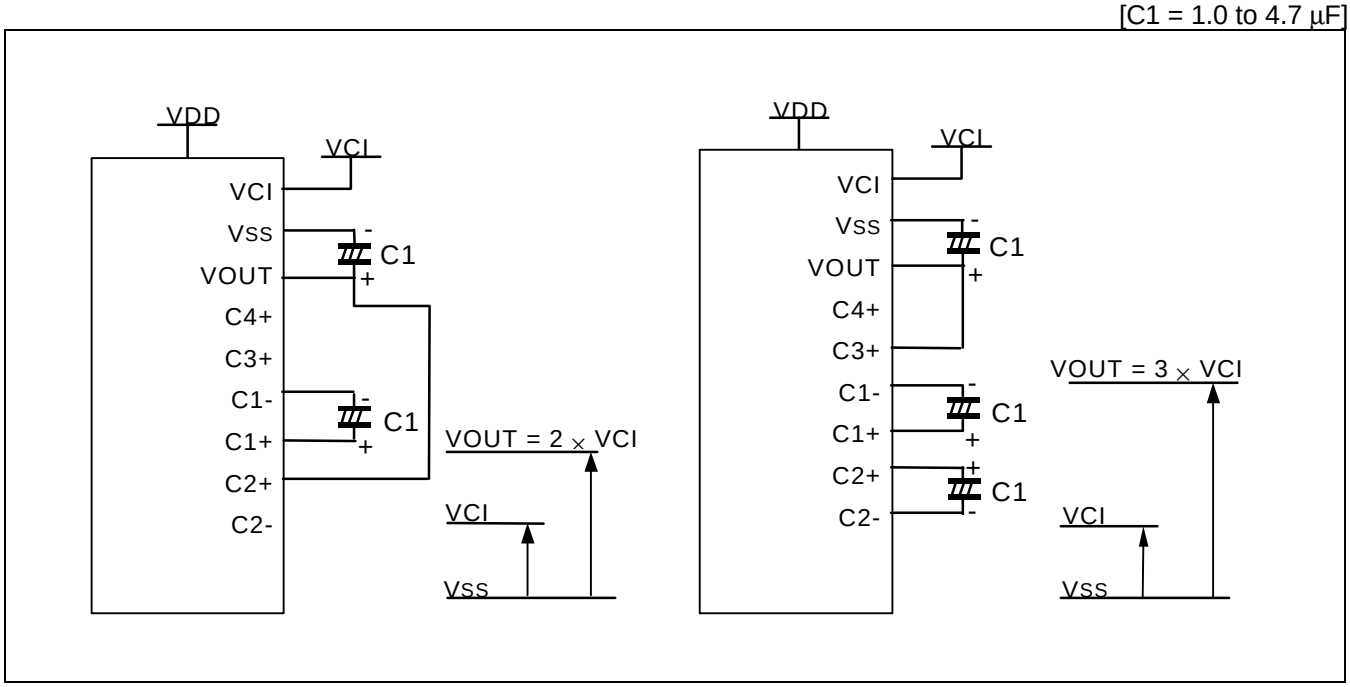


Figure 11. Two Times Boosting Circuit

Figure 12. Three Times Boosting Circuit

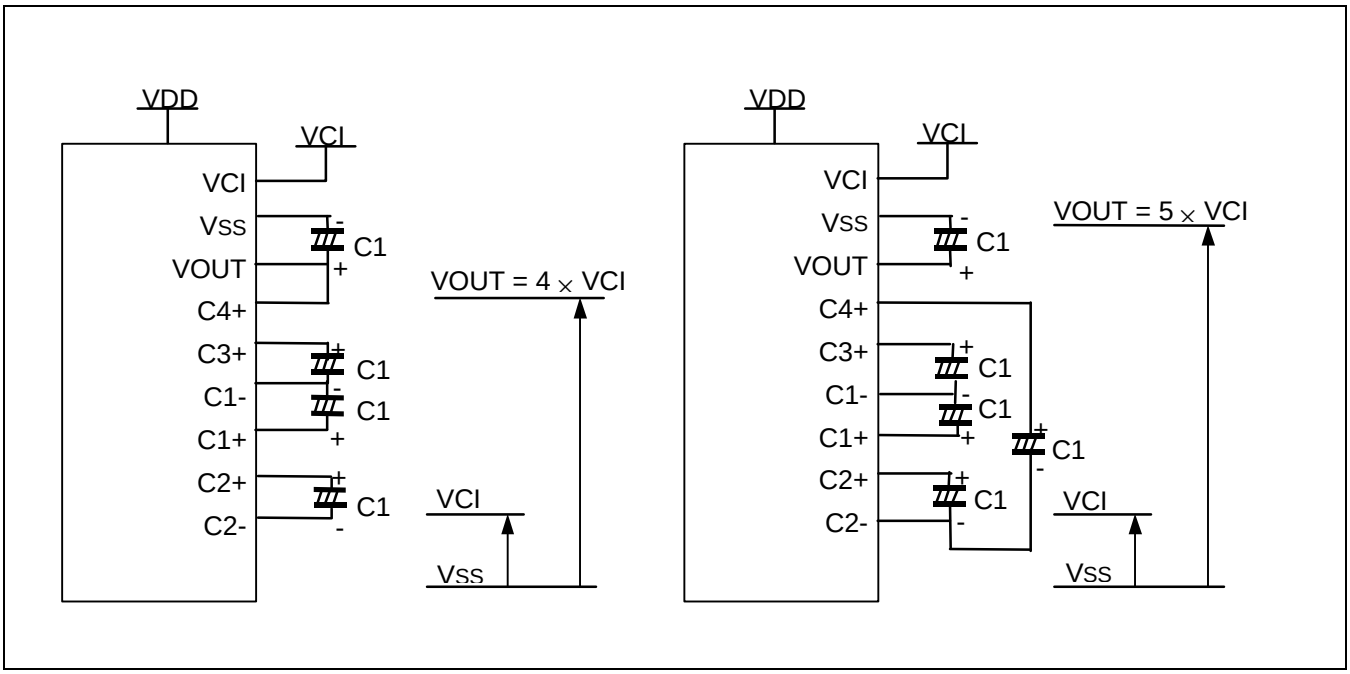


Figure 13. Four Times Boosting Circuit

Figure 14. Five Times Boosting Circuit

* The VCI voltage range must be set so that the VOUT voltage does not exceed the absolute maximum rated value

SAMSUNG ELECTRONICS

Voltage Regulator Circuits

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure 15, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in table 14-1.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{162}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 14-1. V_{REF} Voltage at Ta = 25 °C

REF	Temp. coefficient	V_{REF} [V]
H	-0.05% / °C	2.1
L	External input	VEXT

Table 14-2. Electronic Contrast Control Register (64 Steps)

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62		
1	1	1	1	1	1	63	Maximum	High

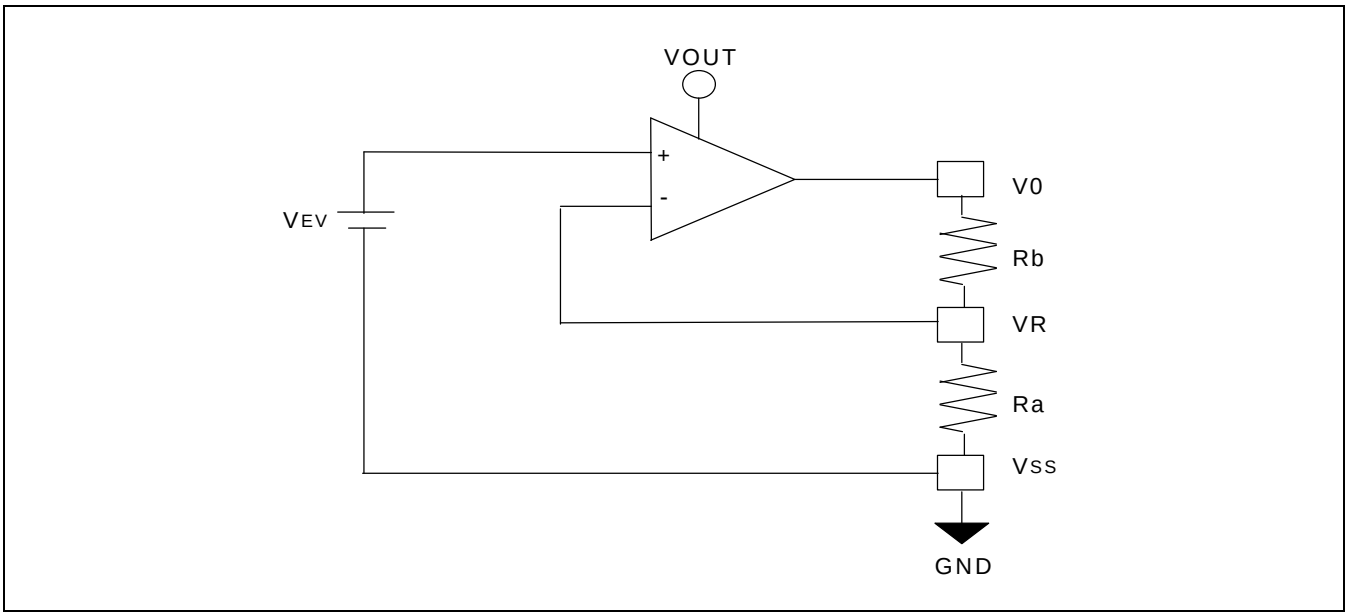


Figure 15. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 15. Internal Rb / Ra ratio depending on 3-bit data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.4

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

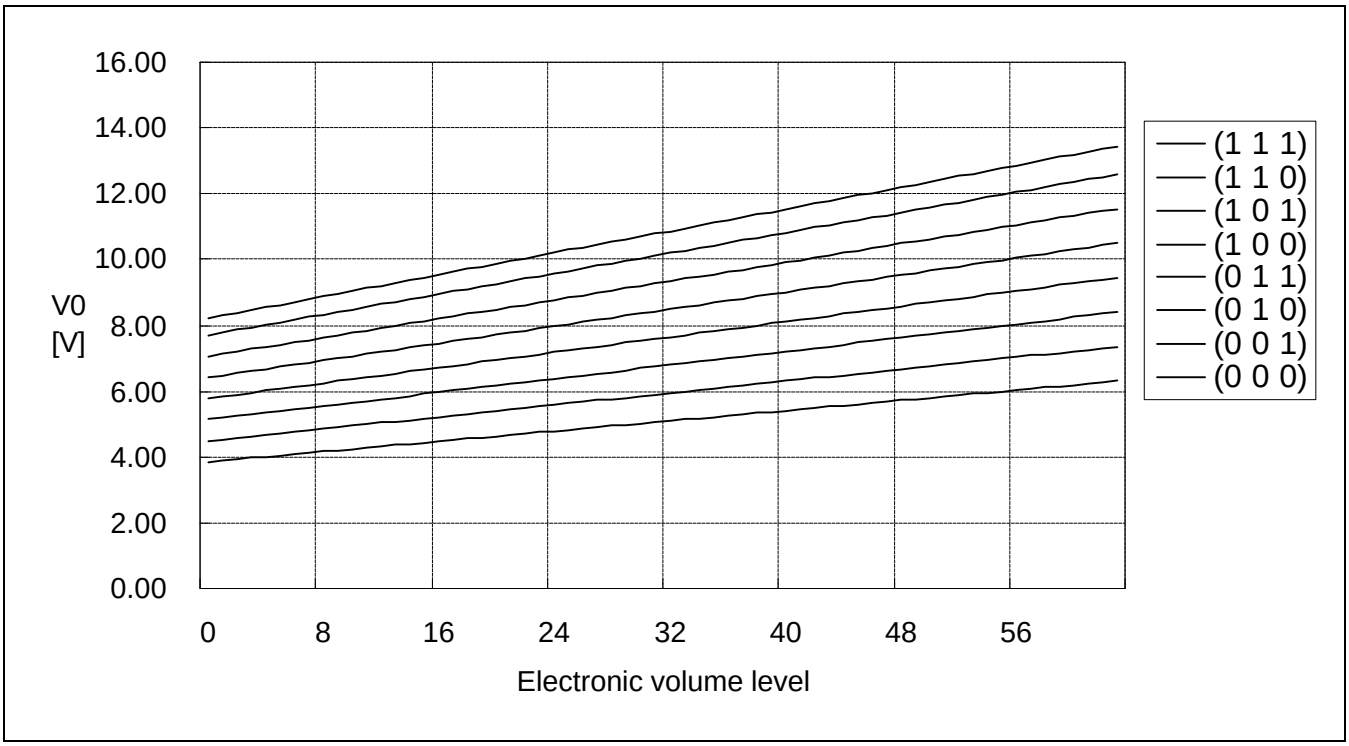


Figure 16. Electronic Volume Level

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(63 - 32)}{162}\right) \times 2.1 \cong 1.698 \quad [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \text{ [uA]} \quad \text{------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5
Ra ≅ 1.69 [MΩ]
Rb ≅ 8.31 [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 16. V0 Depending on Electronic Volume Level

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	7.57	.....	10.00	.....	12.43

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 17. The Relationship between V1 to V4 Level and Duty Ratio

Duty ratio	DUTY1	DUTY0	LCD bias	V1	V2	V3	V4
1/33	L	L	1/5	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0
			1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
1/49	L	H	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/55	H	L	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/65	H	H	1/7	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
			1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0

High Power Mode

The power supply circuit equipped in the S6B0723 for LCD drive has very low power consumption (in normal mode: HPMB = “H”). If use for LCD panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the HPMB pin to “L”(high power mode) can improve the quality of the display. Moreover, if the quality of display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally (Vout or V0 or V1 / V2 / V3 / V4).

REFERENCE CIRCUIT EXAMPLES

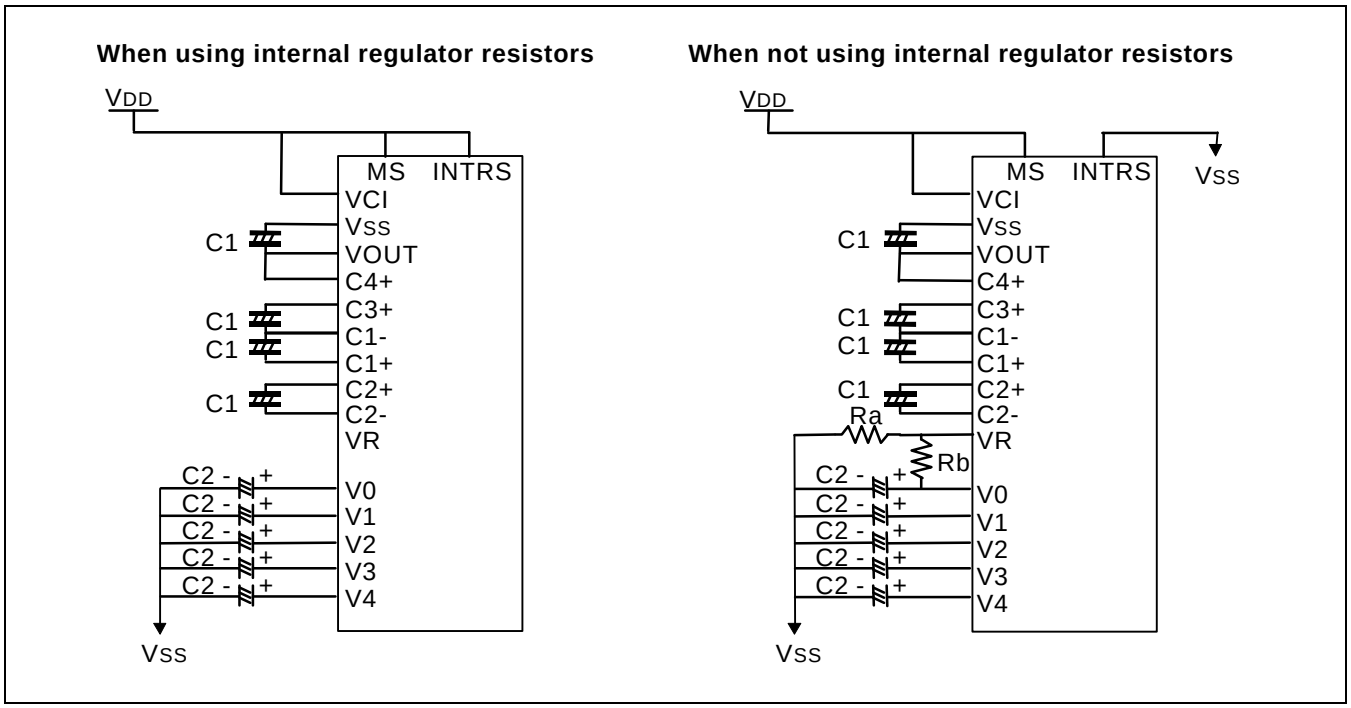


Figure 17. When Using all Internal LCD Power Circuits (VCI = VDD, 4-time V/C: ON, V/R: ON, V/F: ON)

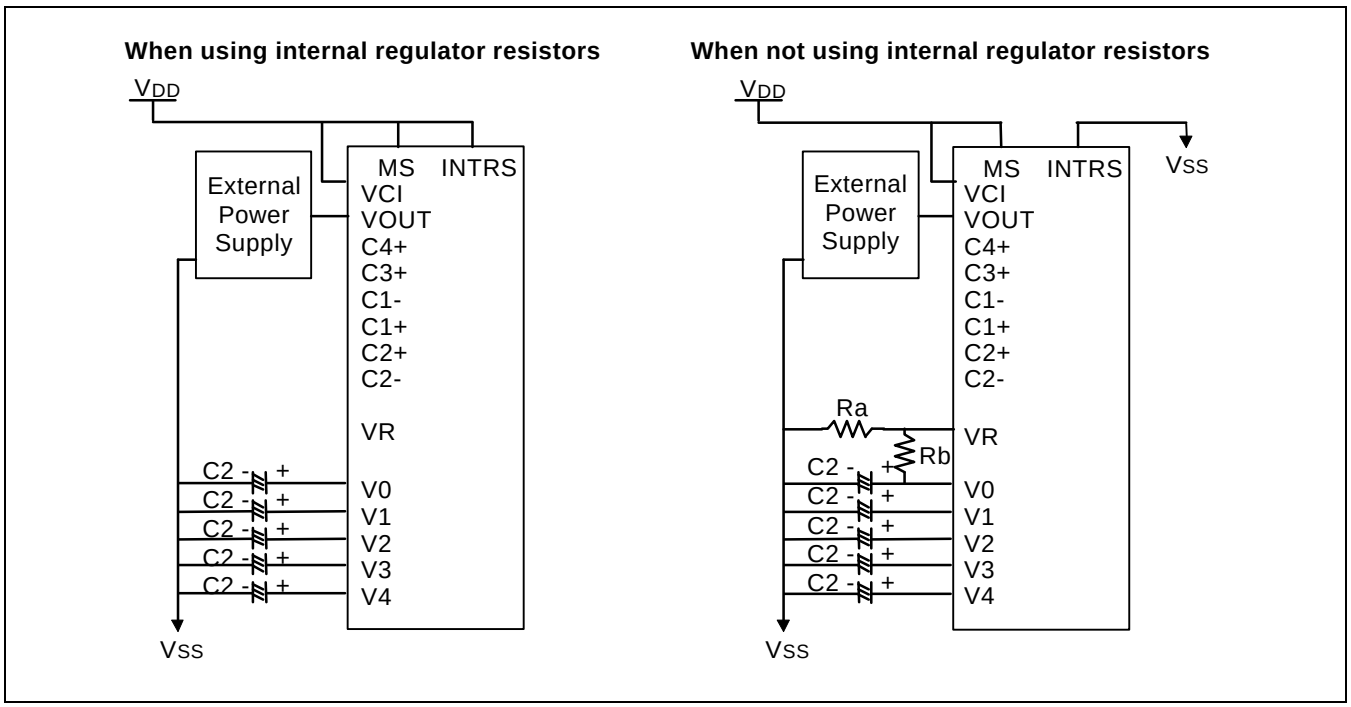


Figure 18. When Using some Internal LCD Power Circuits (VCI = VDD, V/C: OFF, V/R: ON, V/F: ON)

SAMSUNG ELECTRONICS

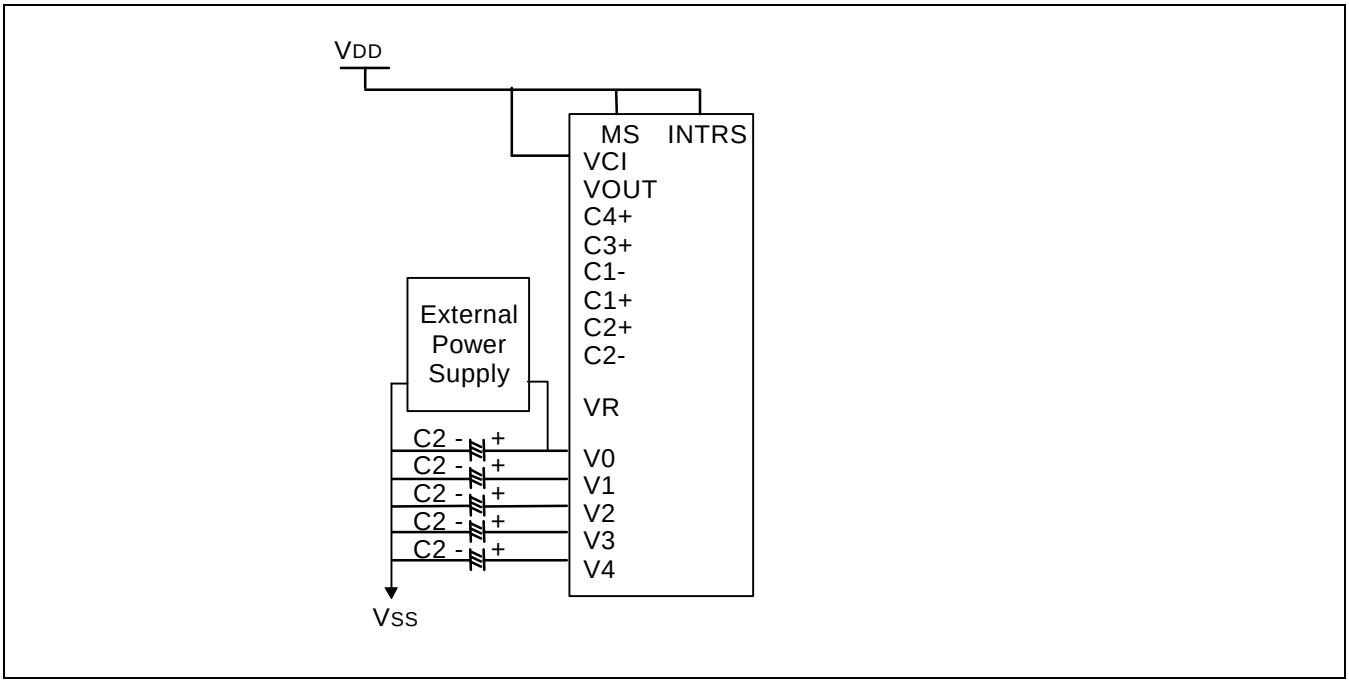
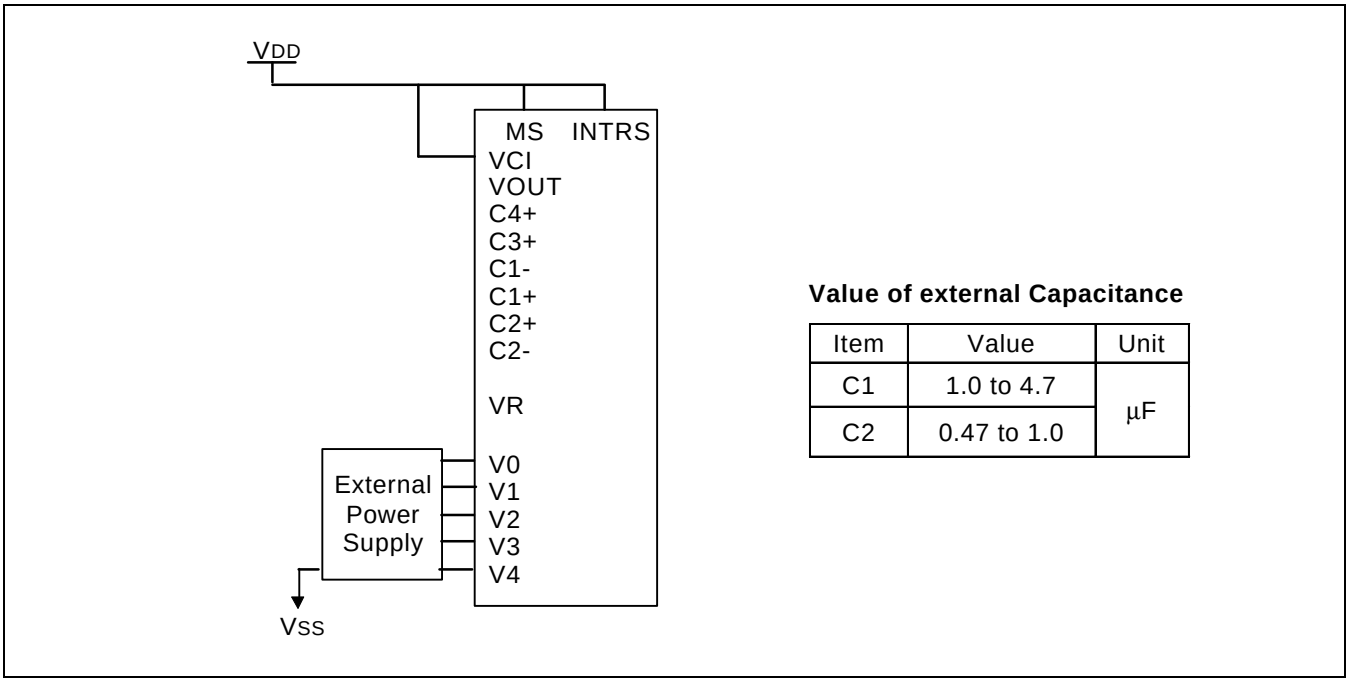


Figure 19. When Using some Internal LCD Power Circuits (VCI = VDD, V/C: OFF, V/R: OFF, V/F: ON)



Value of external Capacitance

Item	Value	Unit
C1	1.0 to 4.7	µF
C2	0.47 to 1.0	

Figure 20. When not Using any Internal LCD Power Supply Circuits (VCI = VDD, V/C: OFF, V/R: OFF, V/F: OFF)

* C1 and C2 are determined by the size of the LCD being driven.
Select a value that will stabilize the liquid crystal drive voltage.

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", following procedure is occurred.

Display ON / OFF: OFF
Entire display ON / OFF: OFF (normal)
ADC select: OFF (normal)
Reverse display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
Serial interface internal register data clear
LCD bias ratio: 1/9 (1/65 duty), 1/8 (1/55 duty), 1/8 (1/49 duty), 1/6 (1/33 duty)
On-chip oscillator OFF
Power save release
Read-modify-write: OFF
SHL select: OFF (normal)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

When RESET instruction is issued, following procedure is occurred.

Read-modify-write: OFF
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
SHL select: 0
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

While RESETB is "L" or Reset instruction is executed, no instruction except read status could be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 18. Instruction Table

×: Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON / OFF LCD panel When DON = 0: display OFF When DON = 1: display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into DDRAM
Read display data	1	1	Read data								Read data from DDRAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0: normal direction (SEG0→SEG131) When ADC = 1: reverse direction (SEG131→SEG0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal/ entire display ON When EON = 0: normal display. When EON = 1: entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0: normal direction (COM0→COM63) When SHL = 1: reverse direction (COM63→COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound Instruction of display OFF and entire display ON

Table 18. Instruction Table (Continued)

×: Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
NOP	0	0	1	1	1	0	0	0	1	1	*Non-Operation command*
Test Iistruction_1	0	0	1	1	1	1	×	×	×	×	*Don' t use this instruction*
Test instruction_2	0	0	1	0	0	1	×	×	×	×	*Don' t use this instruction*

Display ON / OFF

Turns the Display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Initial Display Line

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM63 when SHL = H) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the page address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

Read Status

Indicates the internal status of the S6B0723

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	RESETB	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG131 → SEG0), 1: normal direction (SEG0 → SEG131)
ON / OFF	Indicates display ON / OFF status. 0: display ON, 1: display OFF
RESETB	Indicates the initialization is in progress by RESETB signal. 0: chip is active, 1: chip is being reset

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

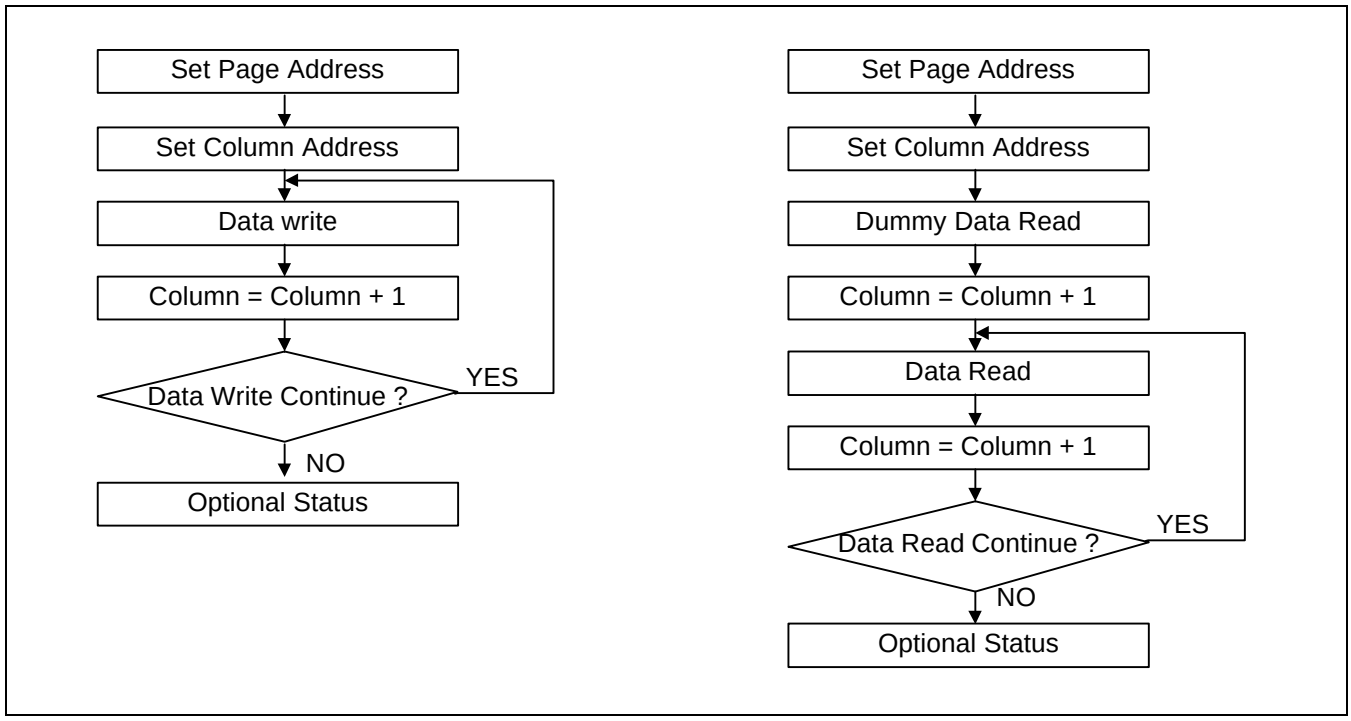


Figure 21. Sequence for Writing Display Data **Figure 22. Sequence for Reading Display Data**

Read Display Data

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

ADC Select (Segment Driver Direction Select)

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG131)
ADC = 1: reverse direction (SEG131 → SEG0)

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display On/Off instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display
EON = 1: entire display ON

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DUTY1	DUTY0	LCD bias	
			Bias = 0	Bias = 1
1/33	0	0	1/6	1/5
1/49	0	1	1/8	1/6
1/55	1	0	1/8	1/6
1/65	1	1	1/9	1/7

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

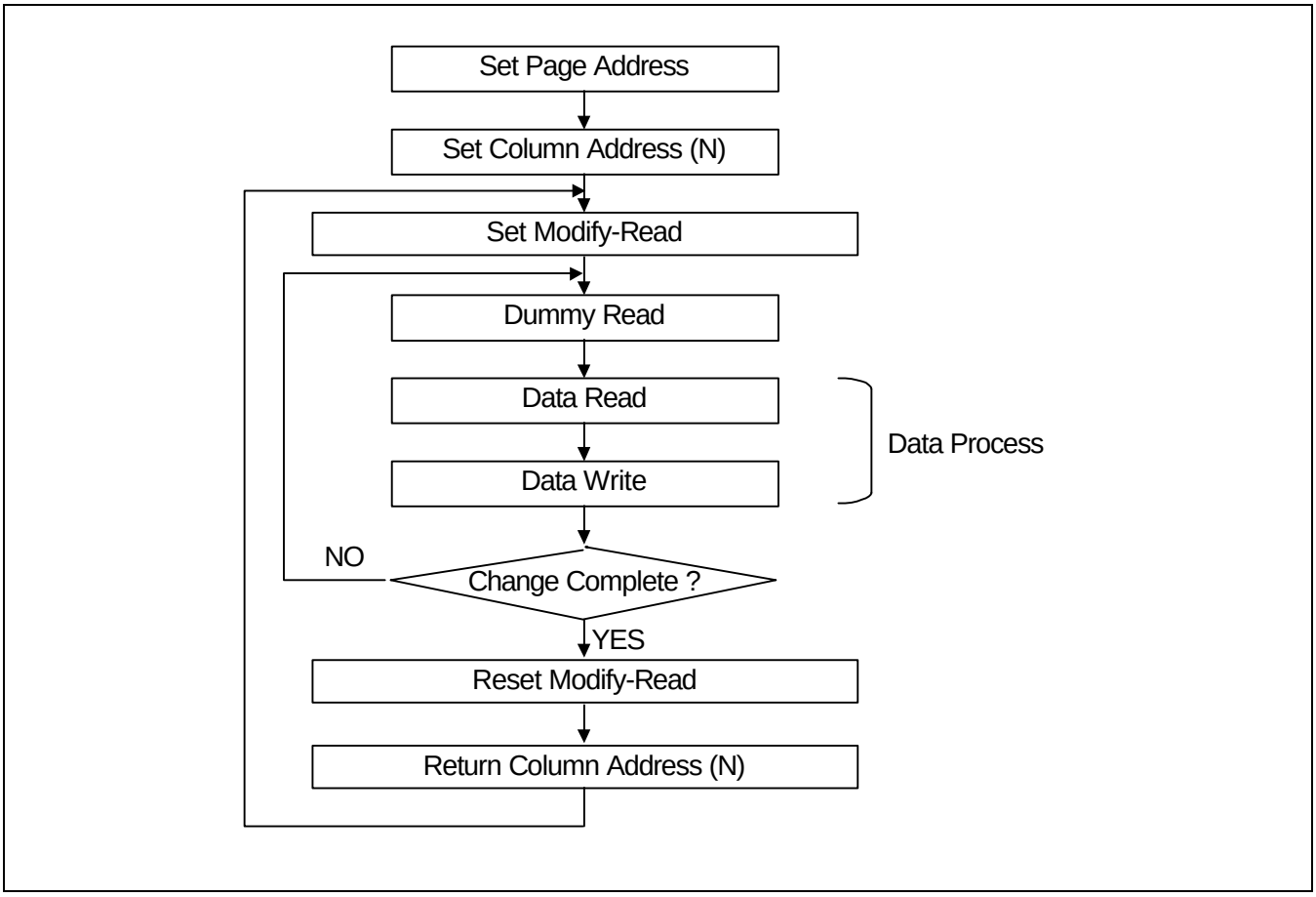


Figure 23. Sequence for Cursor Display

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SHL Select (Common Output Mode Select)

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

× : Don' t care

SHL = 0: normal direction (COM0 → COM63)
SHL = 1: reverse direction (COM63 → COM0)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	(1 + Rb / Ra) ratio
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0 (default)
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4

Reference Voltage Select

Consists of 2-byte instruction. The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62		
1	1	1	1	1	1	63	Maximum	High

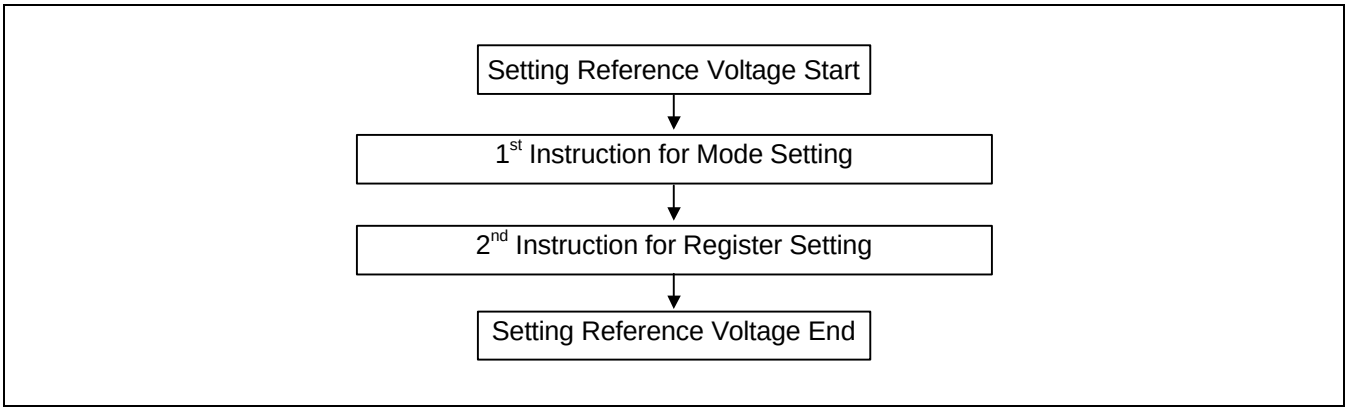


Figure 24. Sequence for Setting the Reference Voltage

Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator Mode) enables the second byte instruction (set Static Indicator Register) to be valid. The first byte sets the static indicator ON / OFF. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this Static Indicator state is released after setting the data of indicator register.

The 1st Instruction: Set Static Indicator Mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The 2nd Instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

NOP

Non Operation Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction (Test Instruction_1 & Test Instruction_2)

These are the instruction for IC chip testing. Please do not use it. If the test instruction is used by accident, it can be cleared by applying "0" signal to the RESETB input pin or the reset instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×
0	0	1	0	0	1	×	×	×	×

Power Save (Compound Instruction)

If the entire display ON / OFF instruction is issued during the display OFF state, S6B0723 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one mode of sleep and standby mode. When Static Indicator mode is ON, standby mode is issued. When OFF, sleep mode is issued. Power save mode is released by the entire display OFF instruction.

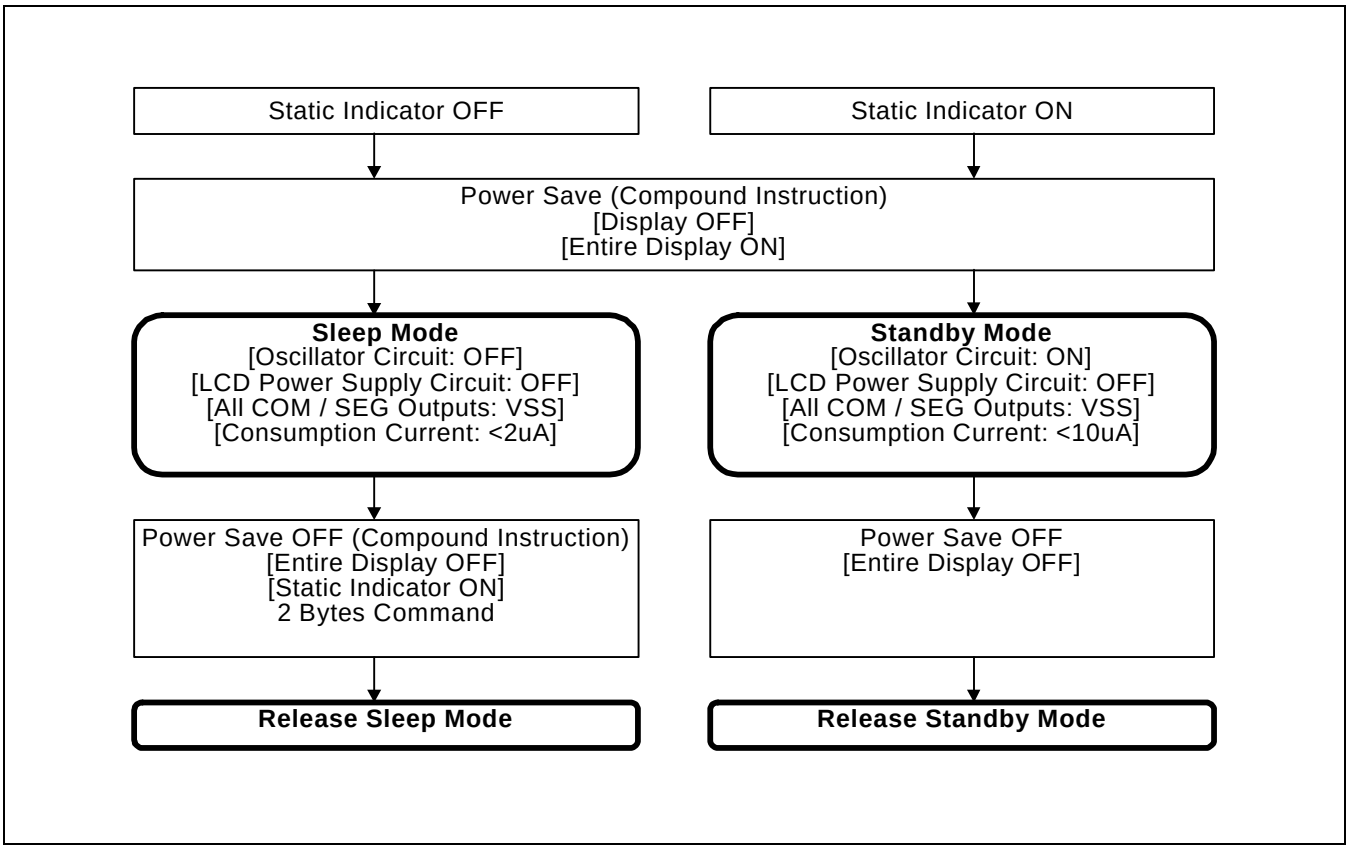


Figure 25. Power Save (Compound Instruction)

– Sleep Mode

This stops all operations in the LCD display system, and as long as there are no access from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

a. The oscillator circuit and the LCD power supply circuit are halted.
b. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a Vss level.

– Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive.
The internal modes are in the following states during standby mode.

a. The LCD power supply circuits are halted. The oscillator circuit continues to operate.
b. The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs a Vss level. The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.

Referential Instruction Setup Flow (1)

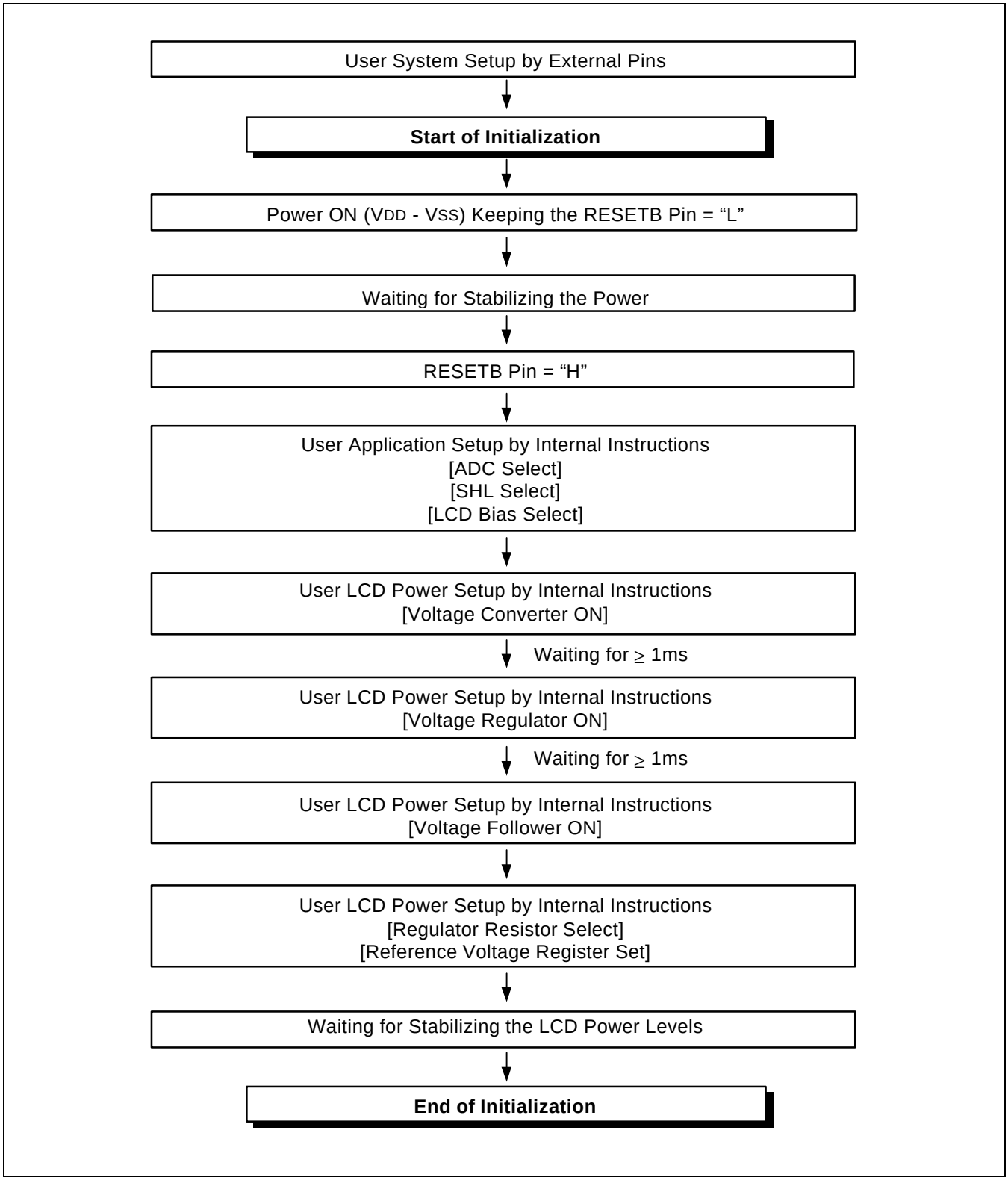


Figure 26. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow (2)

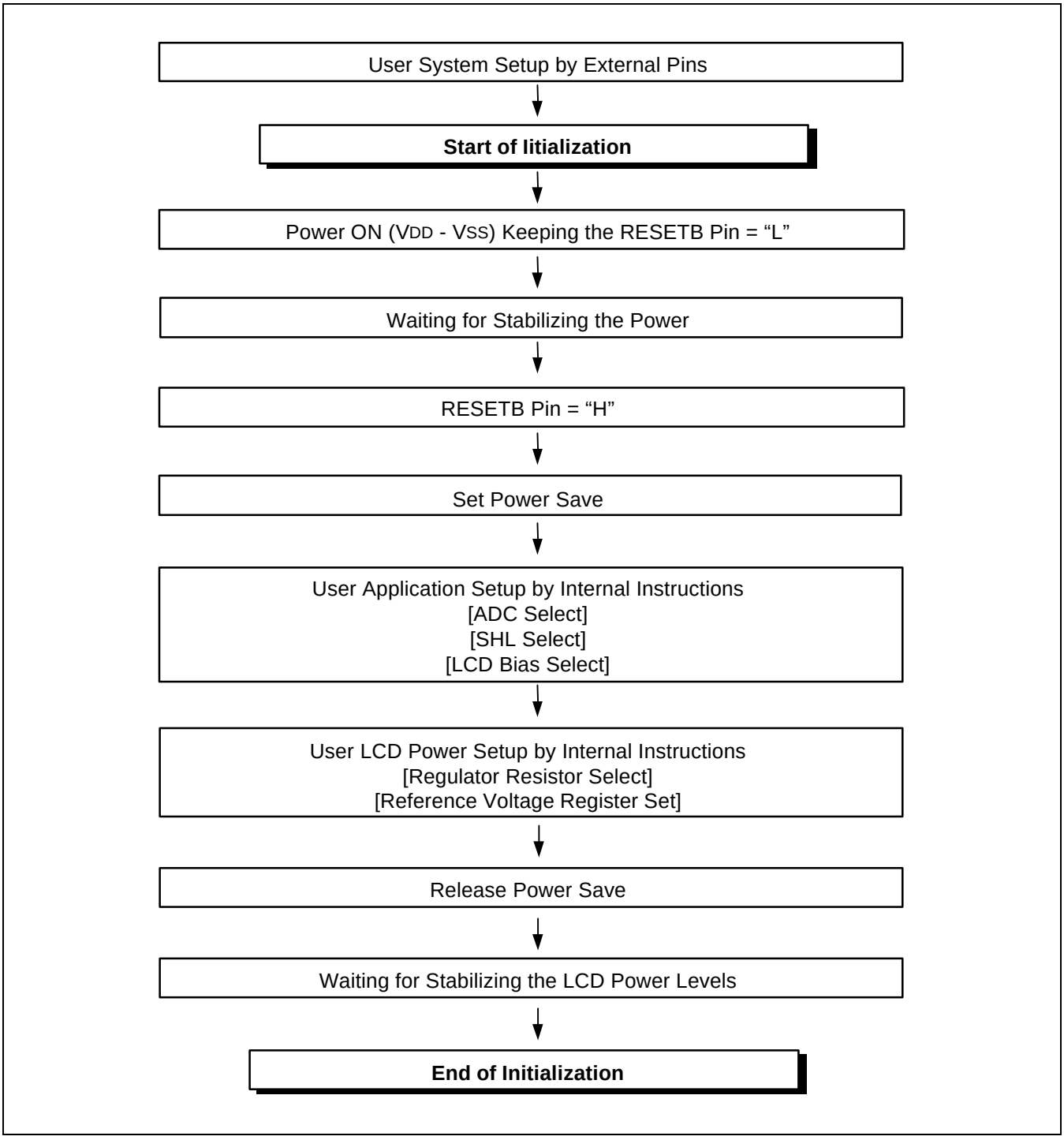


Figure 27. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow (3)

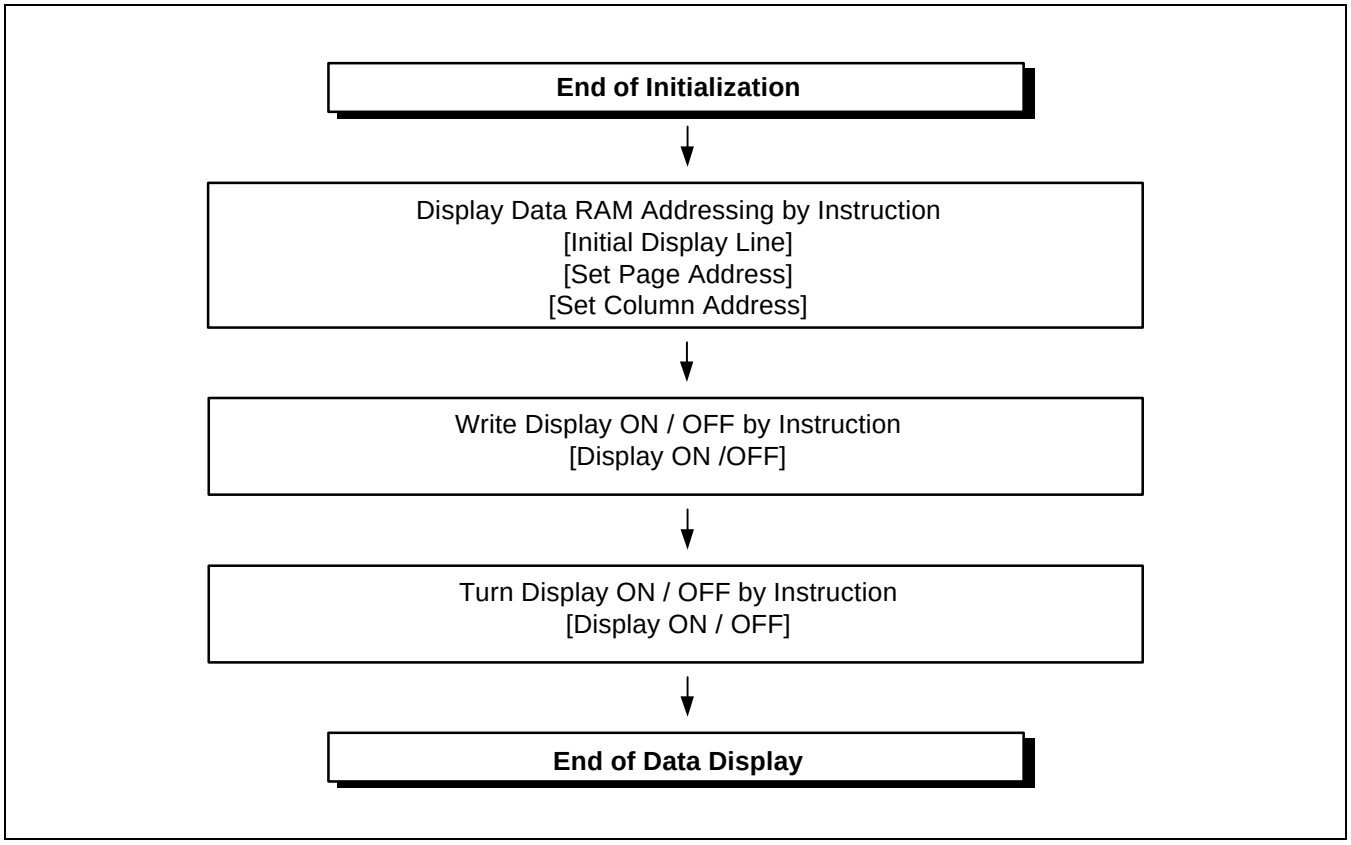


Figure 28. Data Displaying

Referential Instruction Setup Flow (4)

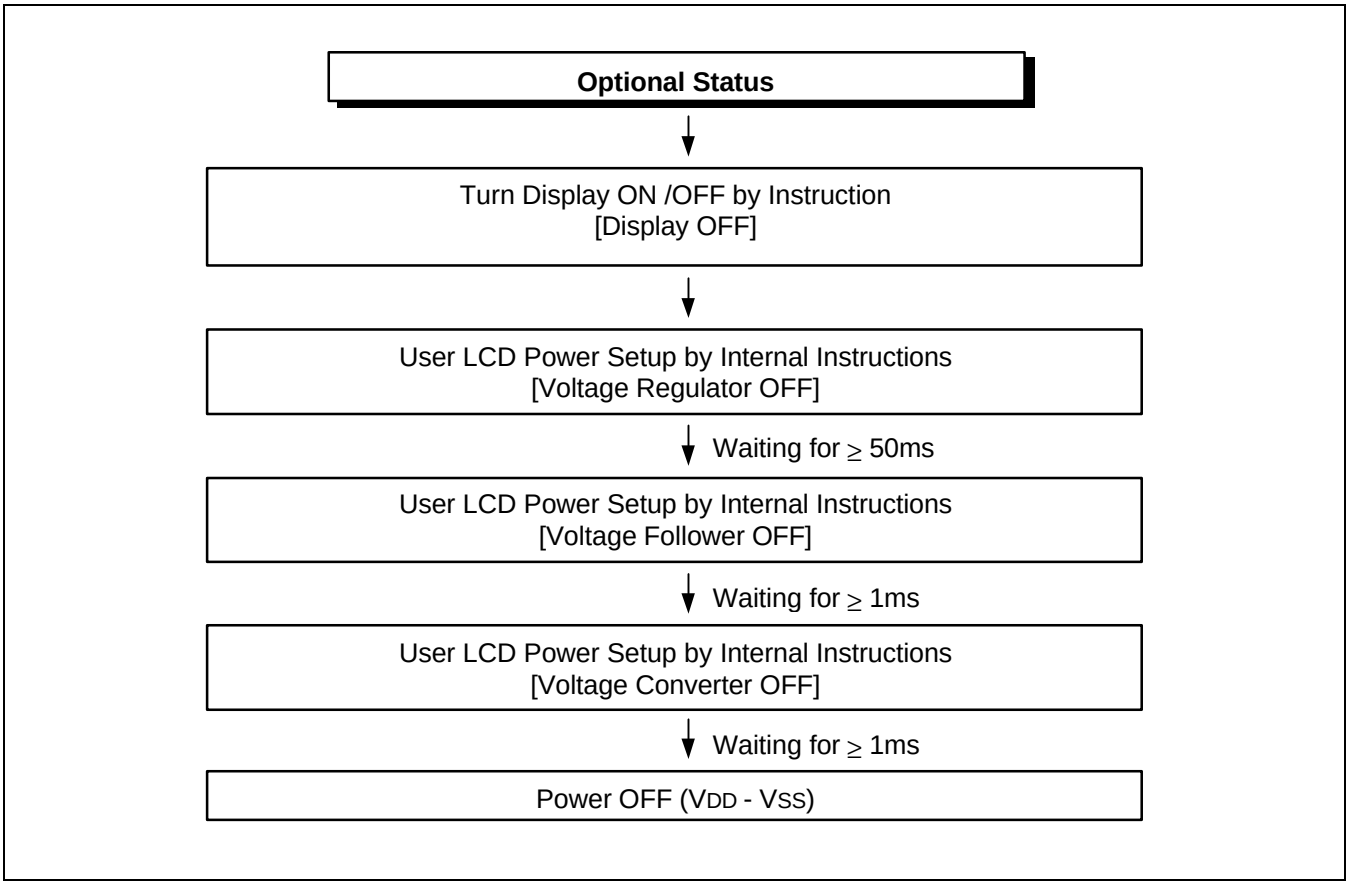


Figure 29. Power OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 to +7.0	V
	V_{LCD}	- 0.3 to +17.0	V
Input voltage range	V_{IN}	- 0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 to +85	°C
Storage temperature range	T_{STR}	- 55 to +125	°C

NOTES:

1. VDD and VLCD are based on VSS = 0V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.(VLCD = V0 – VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 20. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 3.6V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}		2.4	-	3.6	V	VDD *1
Operating voltage (2)		V0		4.5	-	15.0	V	V0 *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Internal	f_{OSC}	Ta = 25°C Duty ratio = 1/65	32.7	43.6	54.5	kHz	CL *8
	External	f_{CL}		4.09	5.45	6.81		
Voltage converter input voltage		VCI	× 2	2.4	-	3.6	V	VCI
			× 3	2.4	-	3.6		
			× 4	2.4	-	3.6		
			× 5	2.4	-	3.2		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT		6.0	-	16.0	V	VOUT
Voltage follower operating voltage		V0		4.5	-	15.0	V	V0 *9
Reference voltage		V_{REF}	Ta = 25°C - 0.05%/°C	2.04	2.1	2.16	V	*10

Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V_{DD} = 3.0V V0 – V_{SS} = 11.0V 1/65 duty ratio Display pattern OFF	-	15	23	μA	*11

Dynamic Current Consumption (2) when the Built-in Power Circuit is ON (At Operate Mode)

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V, (VCI = V_{DD}, 4 times boosting) V0 – V_{SS} = 11.0V, 1/65 duty ratio, Display pattern OFF, Normal power mode	-	40	60	μA	*12
		V_{DD} = 3.0V, (VCI = V_{DD}, 4 times boosting) V0 – V_{SS} = 11.0V, 1/65 duty ratio, Display pattern checker, Normal power mode	-	150	200	μA	*12

Current Consumption during Power Save Mode

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DDS1}	During sleep	-	-	2.0	μA	
Standby mode current	I_{DDS2}	During standby	-	-	10.0	μA	

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	f_{CL}	f_{FR}
1/65	On-chip oscillator circuit is used	$\frac{fosc}{8}$	$\frac{fosc}{2 \times 8 \times 65}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{fosc}{2 \times 65}$
1/55	On-chip oscillator circuit is used	$\frac{fosc}{9}$	$\frac{fosc}{2 \times 9 \times 55}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{fosc}{2 \times 55}$
1/49	On-chip oscillator circuit is used	$\frac{fosc}{10}$	$\frac{fosc}{2 \times 10 \times 49}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{fosc}{2 \times 49}$
1/33	On-chip oscillator circuit is used	$\frac{fosc}{15}$	$\frac{fosc}{2 \times 15 \times 33}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{fosc}{2 \times 33}$

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: LCD AC signal frequency)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RDB, RW_WRB, RESETB, MS, C68, PS, INTRS, HPMB, CLS, CL, M, FR, DISP pins.
*4. DB0 to DB7, M, FR, DISP, CL pins.
*5. CS1B, CS2, RS, DB[7:0], E_RDB, RW_WRB, RESETB, MS, C68, PS, INTRS, HPMB, CLS, CL, M, FR, DISP pins.
*6. Applies when the DB[7:0], M, FR, DISP, and CL pins are in high impedance.
*7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON = ΔV / 0.1 [kΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)
*8. See table 21 for the relationship between oscillation frequency and frame frequency.
*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

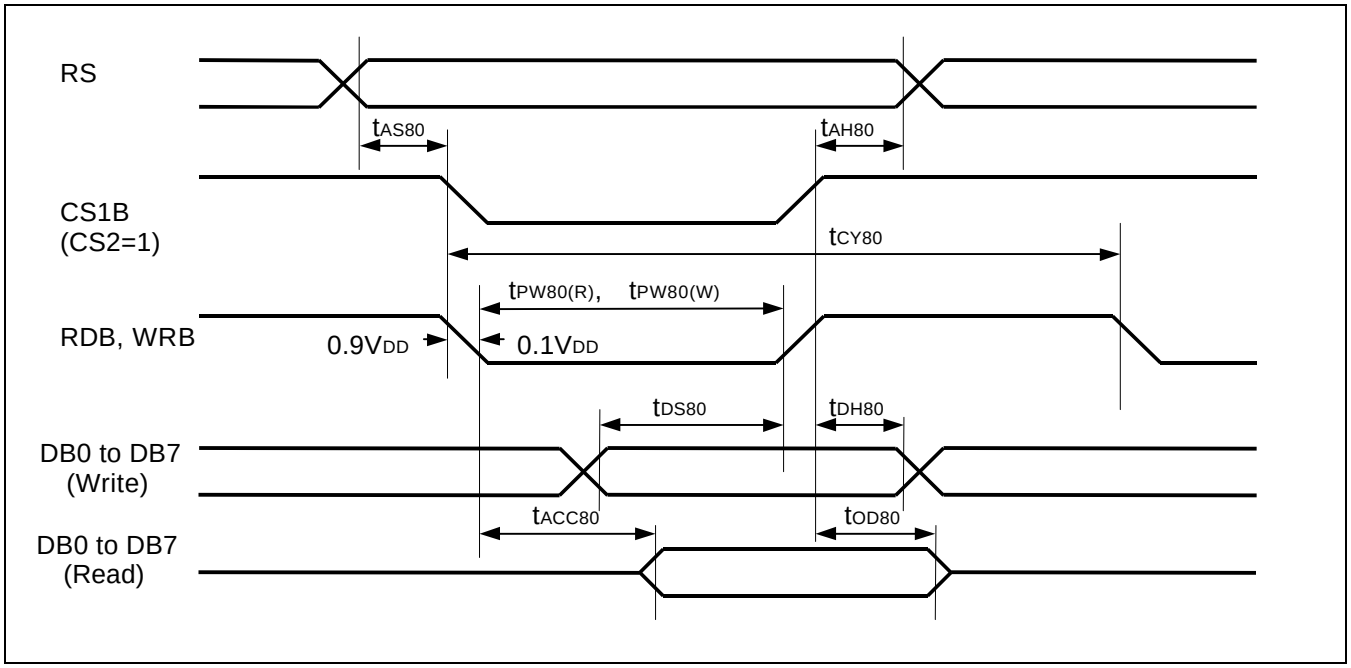


Figure 30. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time	RS	t_{CY80}	300	-	-	ns	
Pulse width (WRB)	RW_WRB	$t_{PW80\ (W)}$	60	-	-	ns	
Pulse width (RDB)	E_RDB	$t_{PW80\ (R)}$	60	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	40 15	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	- 10	-	140 100	ns	C_L = 100 pF

Read / Write Characteristics (6800-series Microprocessor)

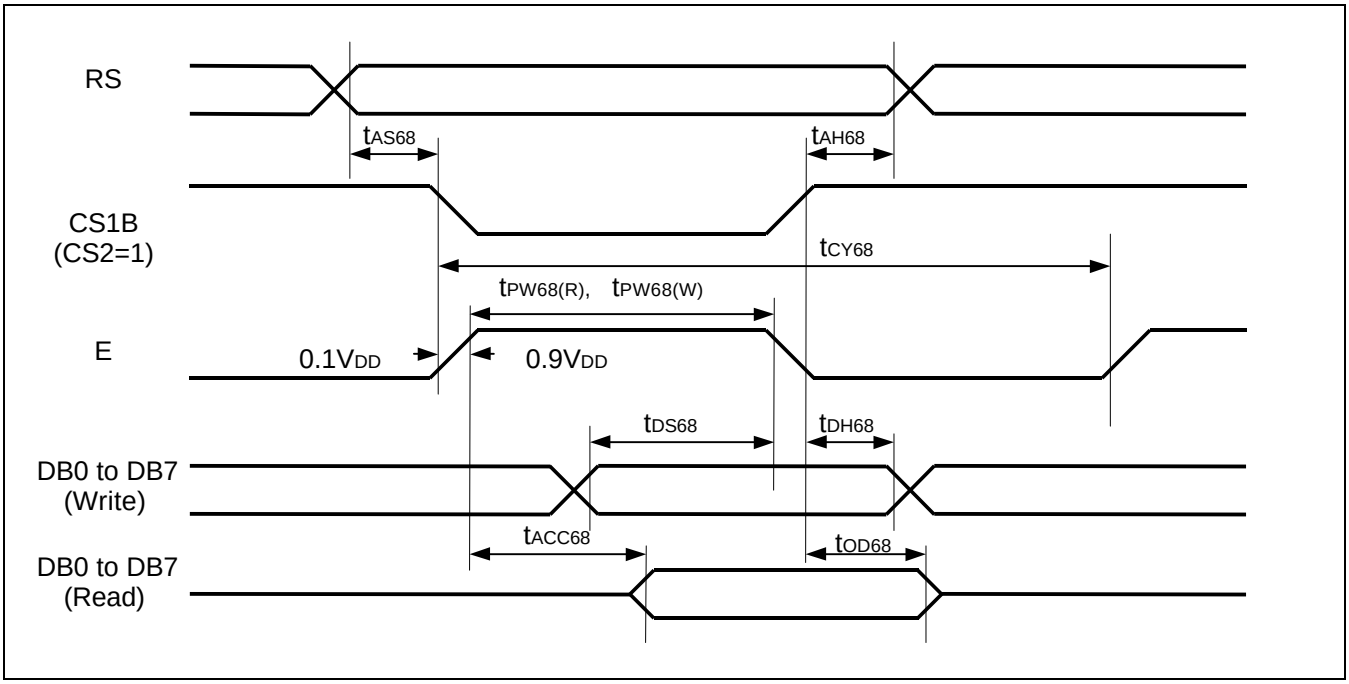


Figure 31. Read / Write Characteristics (6800-series Microprocessor)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle time		RS	t_{CY68}	300	-	-	ns	
Data setup time Data hold time		DB7 to DB0	t_{DS68} t_{DH68}	40 15	-	-	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	- 10	-	140 100	ns	C_L = 100 pF
Enable pulse width	Read Write	E_RDB	$t_{PW68(R)}$ $t_{PW68(W)}$	120 60	-	-	-	

Serial Interface Characteristics

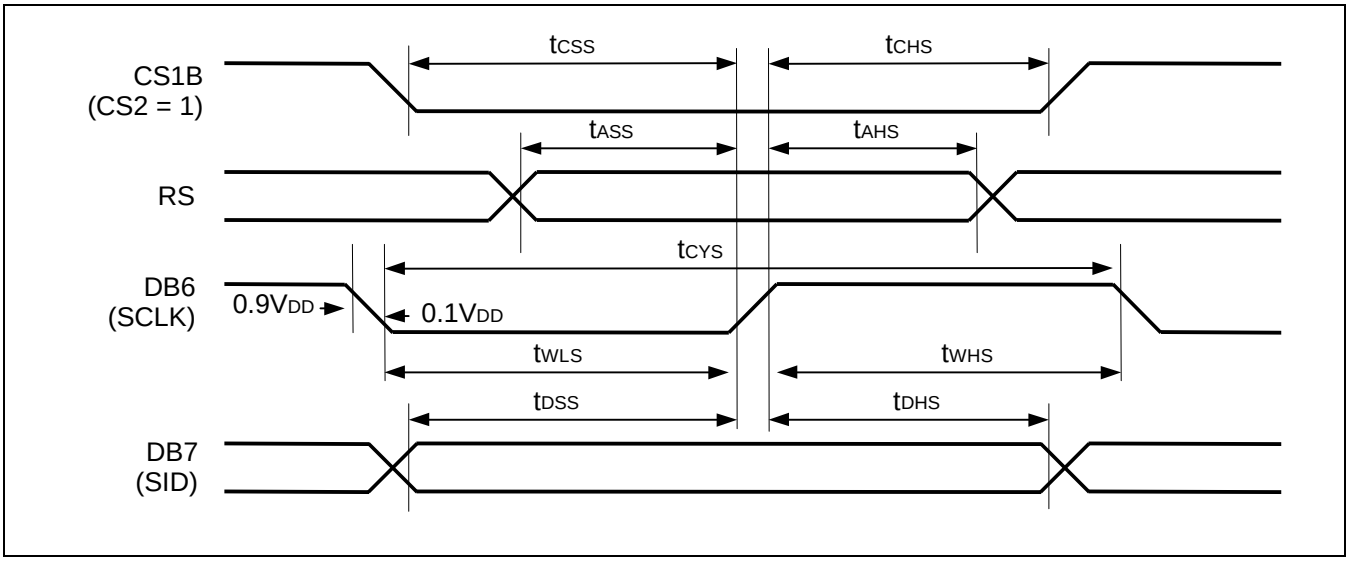


Figure 32. Serial Interface Characteristics

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	250 100 100	- - -	- - -	ns	
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	100 100	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	150 150	- -	- -	ns	

Reset Input Timing

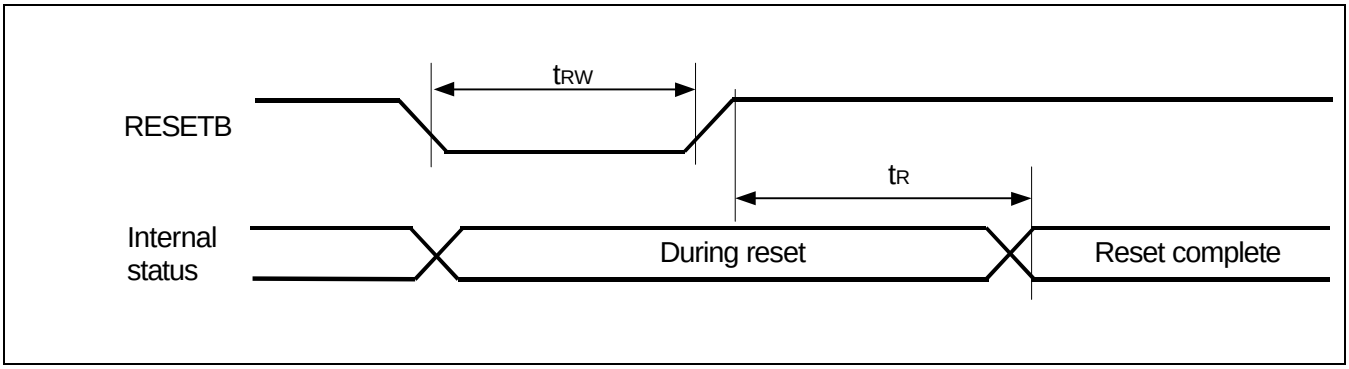


Figure 33. Reset Input Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	1.0	-	-	µs	
Reset time	-	t_R	-	-	1.0	µs	

Display Control Output Timing

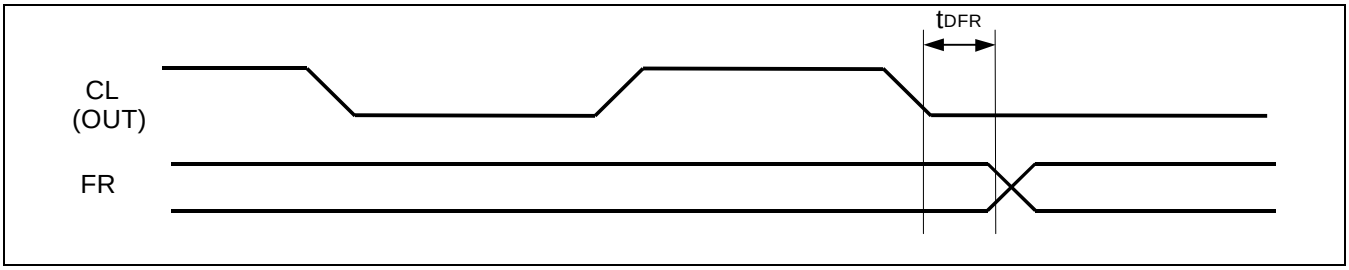


Figure 34. Display Control Output Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	20	80	ns	C_L = 50 pF

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = "H", C68 = "H")

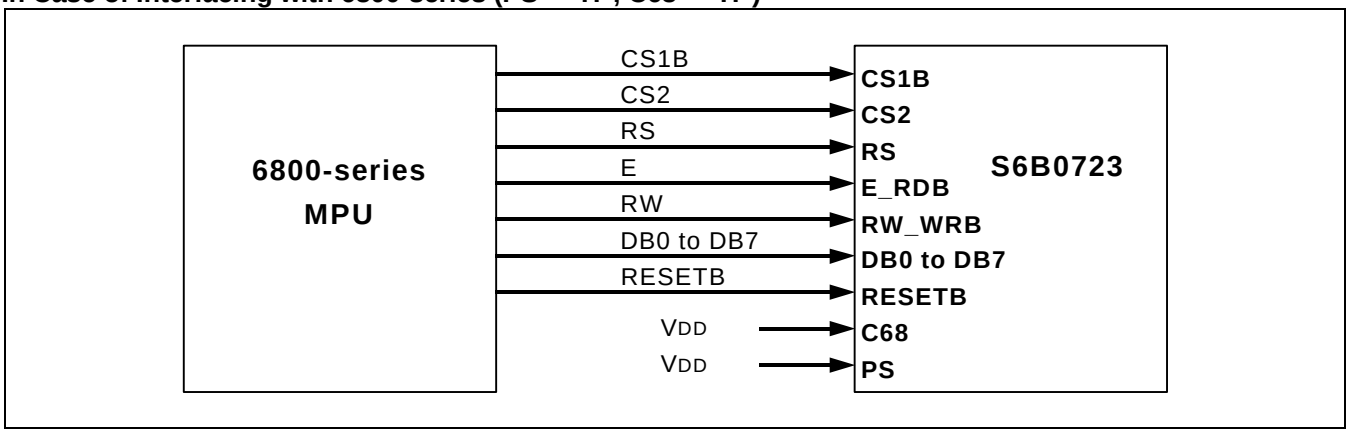


Figure 35. Interfacing with 6800-series (PS = "H", C68 = "H")

In Case of Interfacing with 8080-series (PS = "H", C68 = "L")

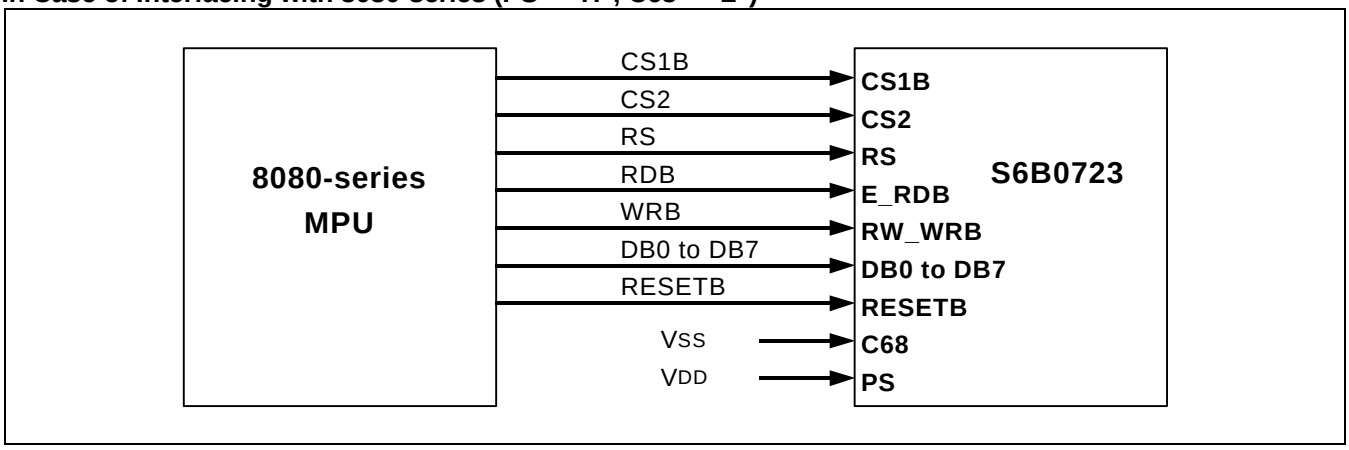


Figure 36. Interfacing with 8080-series (PS = "H", C68 = "L")

In Case of Serial Interface (PS = "L", C68 = "H or L")

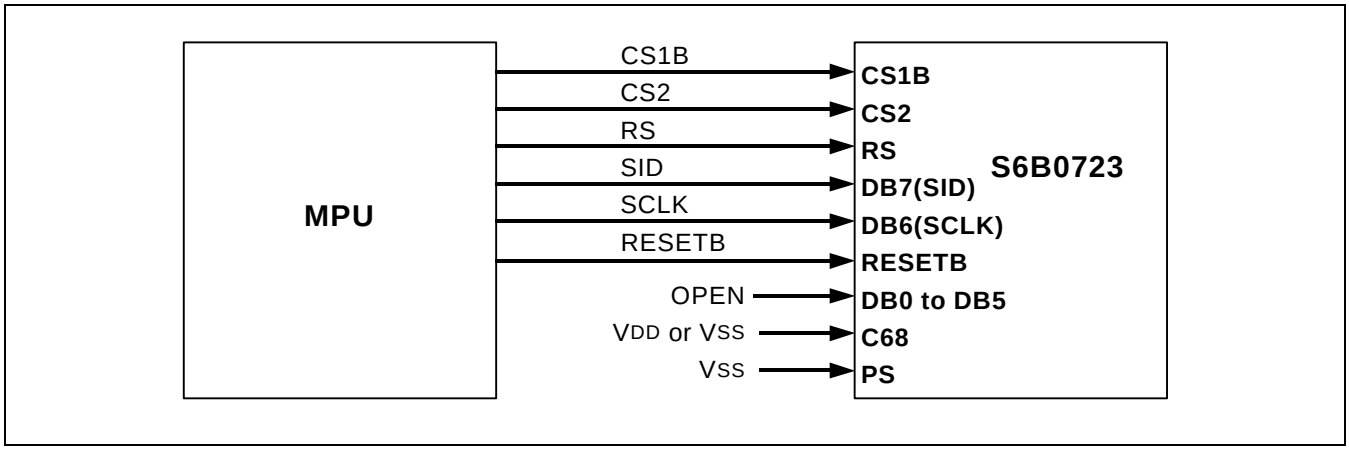


Figure 37. Serial Interface (PS = "L", C68 = "H or L")

CONNECTIONS BETWEEN S6B0723 AND LCD PANEL

Single Chip Structure (1/65 Duty Configurations)

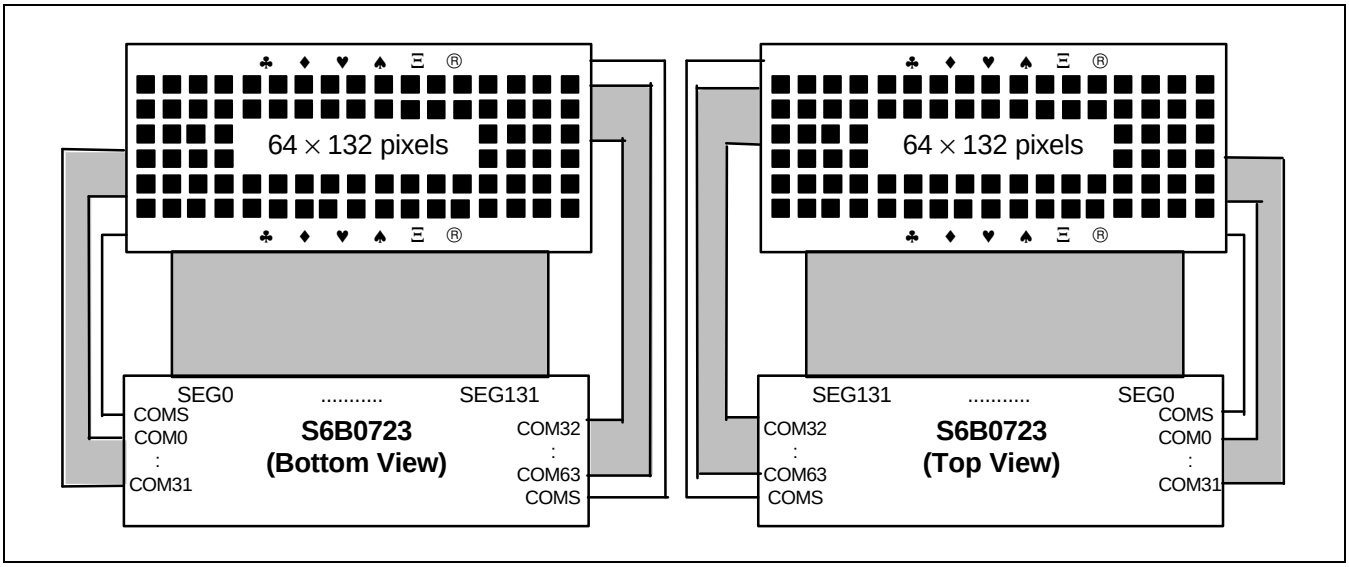


Figure 38. SHL = 1, ADC = 0 **Figure 39. SHL = 1, ADC = 1**

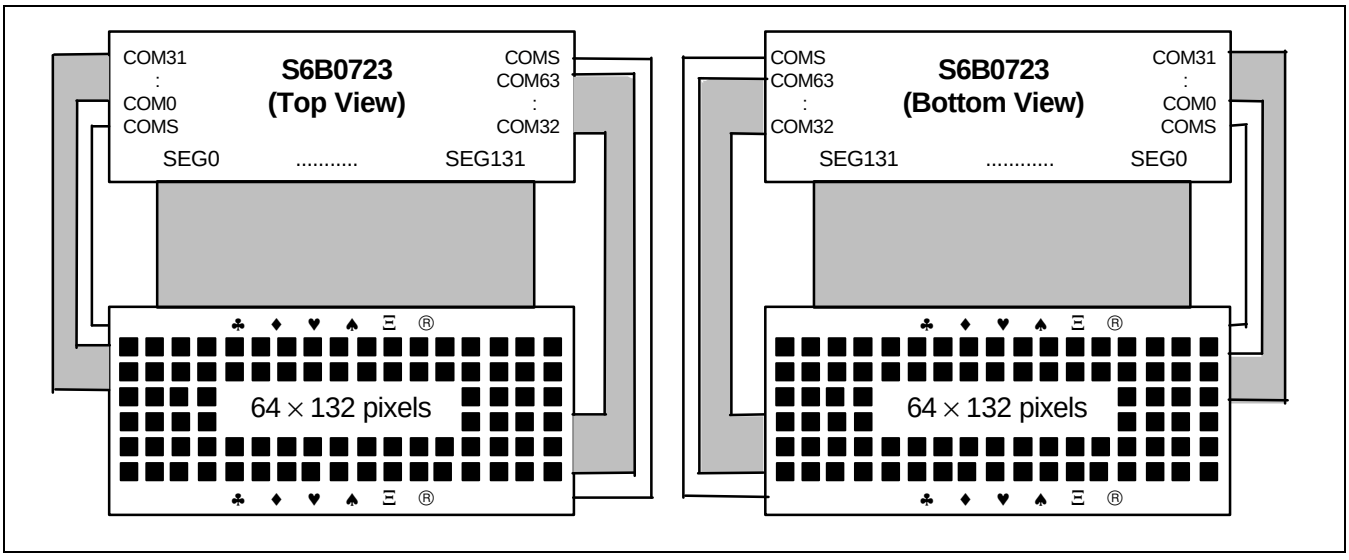


Figure 40. SHL = 0, ADC = 0 **Figure 41. SHL = 0, ADC = 1**

Single Chip Structure (1/55 Duty Configurations)

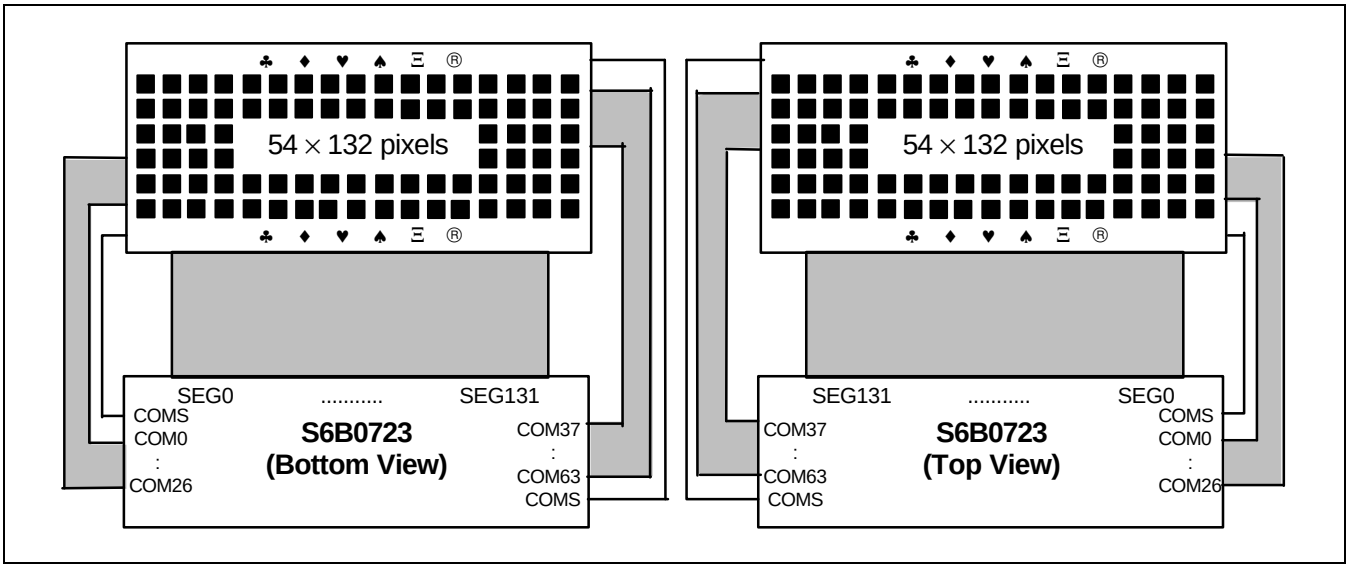


Figure 42. SHL = 1, ADC = 0

Figure 43. SHL = 1, ADC = 1

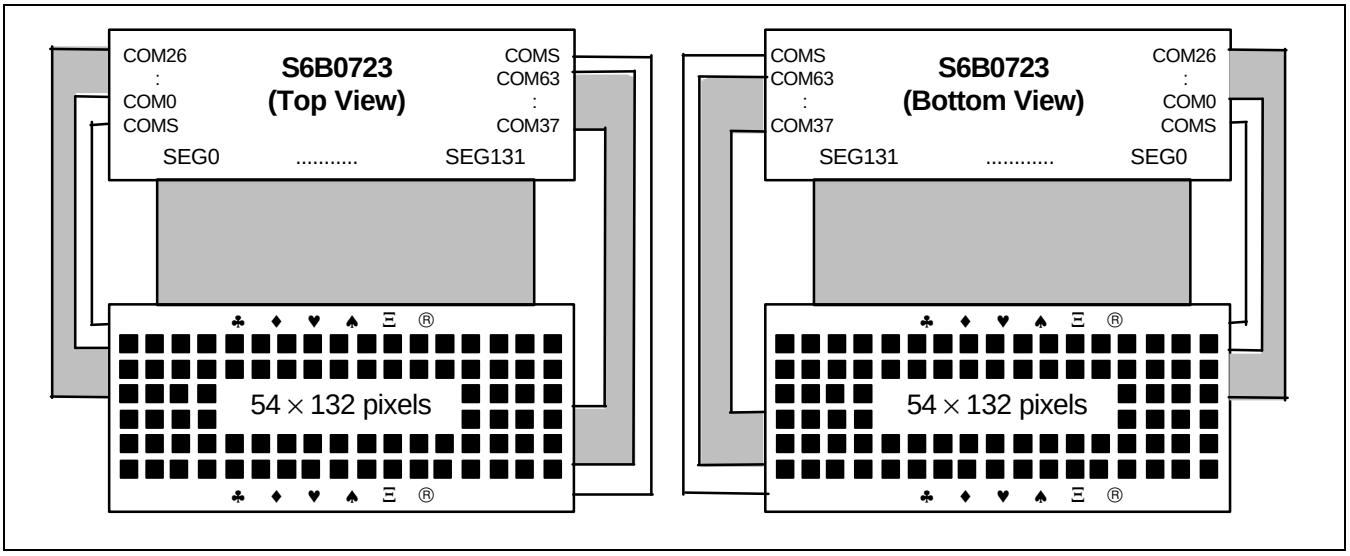


Figure 44. SHL = 0, ADC = 0

Figure 45. SHL = 0, ADC = 1

Single Chip Structure (1/49 Duty Configurations)

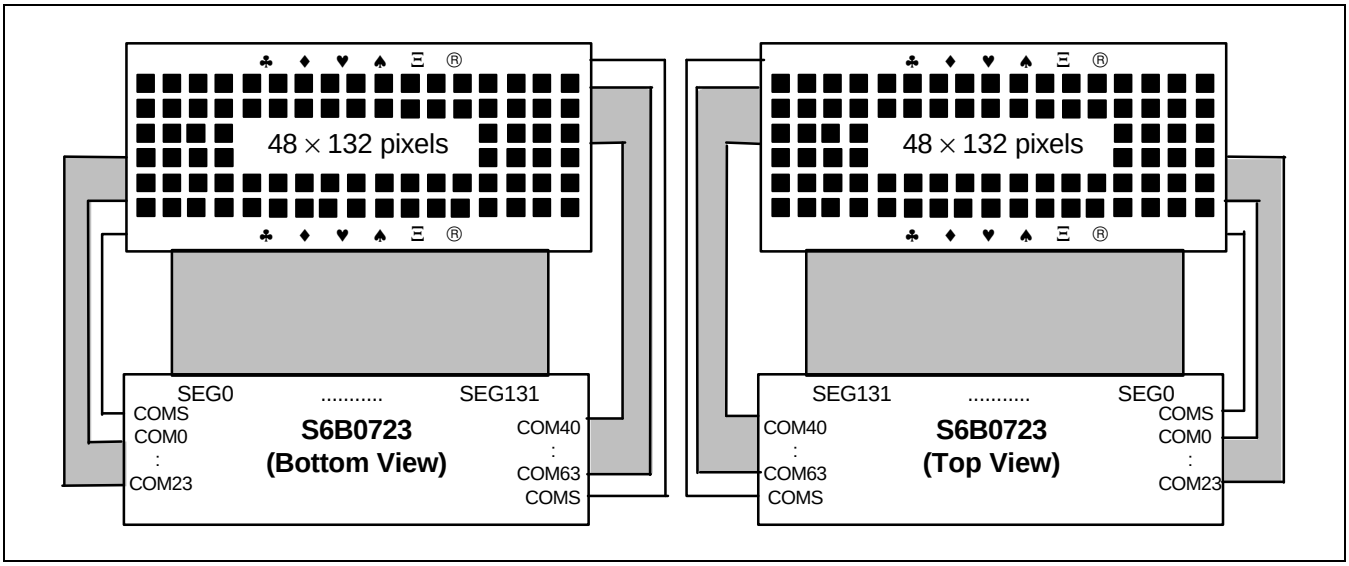


Figure 46. SHL = 1, ADC = 0 **Figure 47. SHL = 1, ADC = 1**

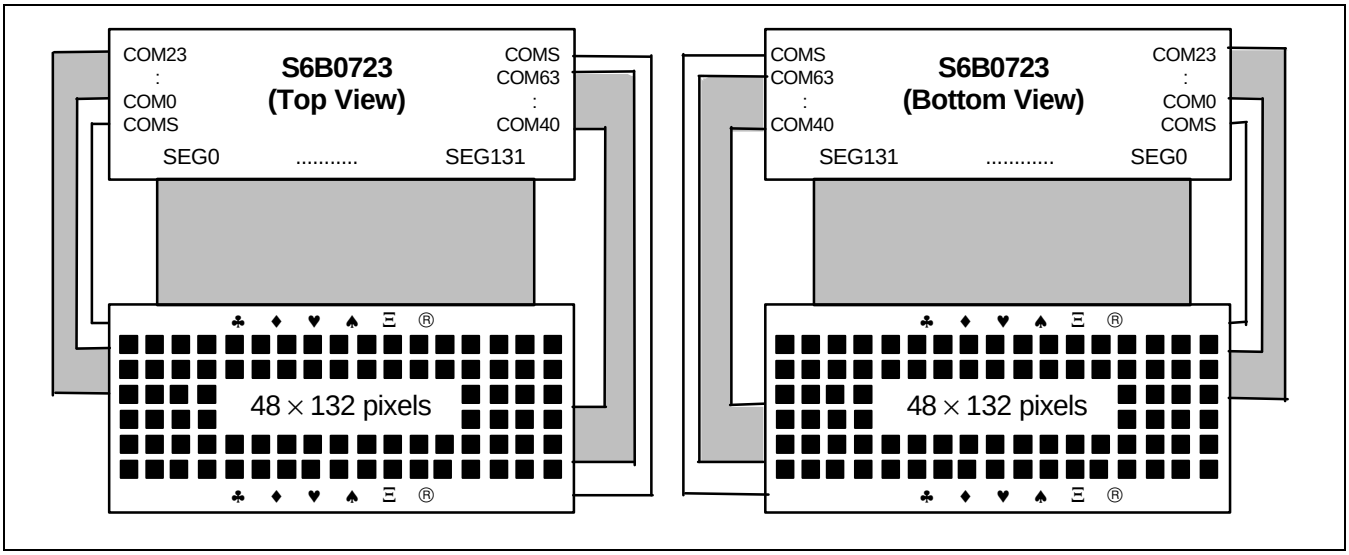


Figure 48. SHL = 0, ADC = 0 **Figure 49. SHL = 0, ADC = 1**

Single Chip Structure (1/33 Duty Configurations)

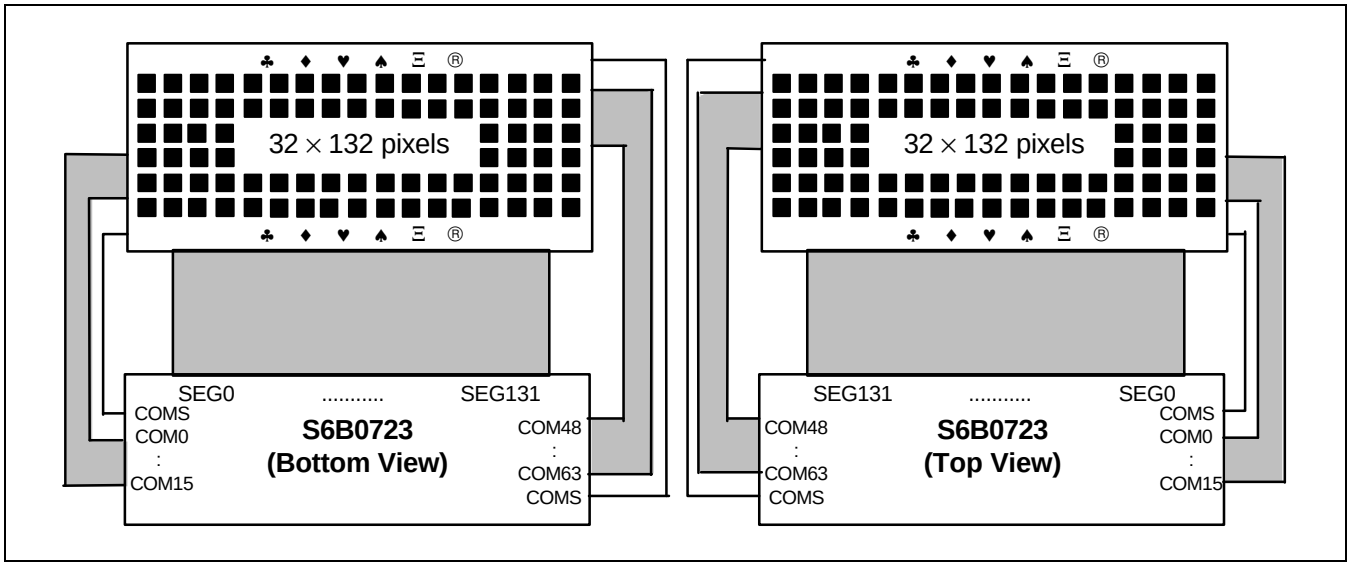


Figure 50. SHL = 1, ADC = 0

Figure 51. SHL = 1, ADC = 1

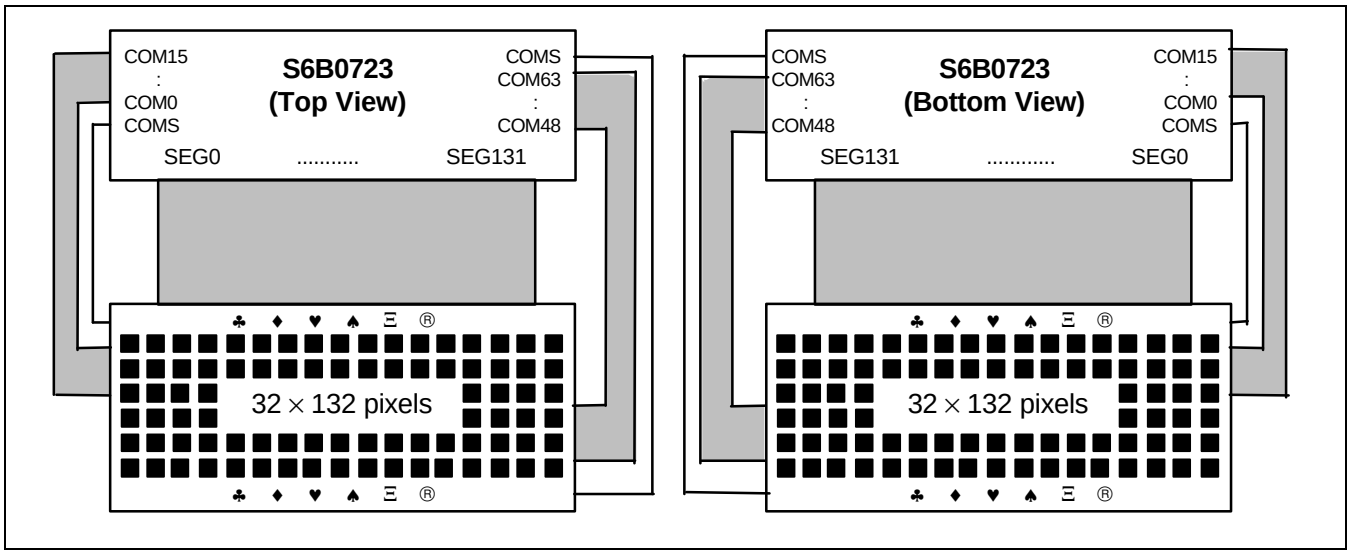


Figure 52. SHL = 0, ADC = 0

Figure 53. SHL = 0, ADC = 1

Multiple Chip Structure

- 65COM (64COM + 1COMS) ´ 264SEG (132SEG ´ 2)

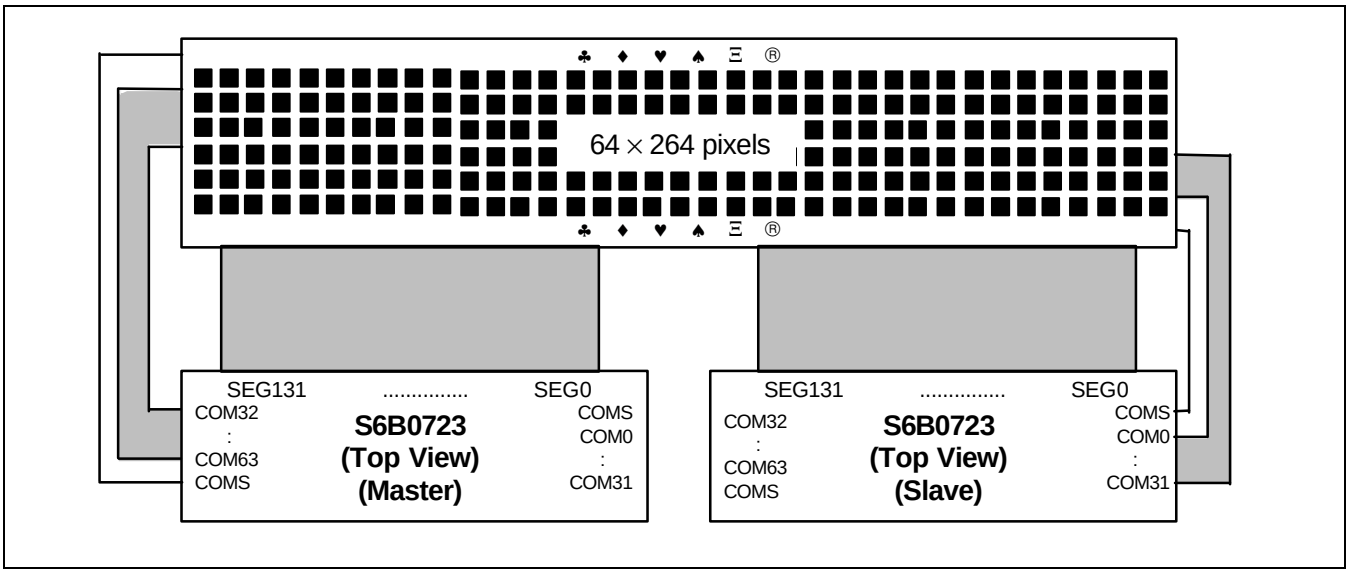


Figure 54. SHL = 1, ADC = 1

- Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

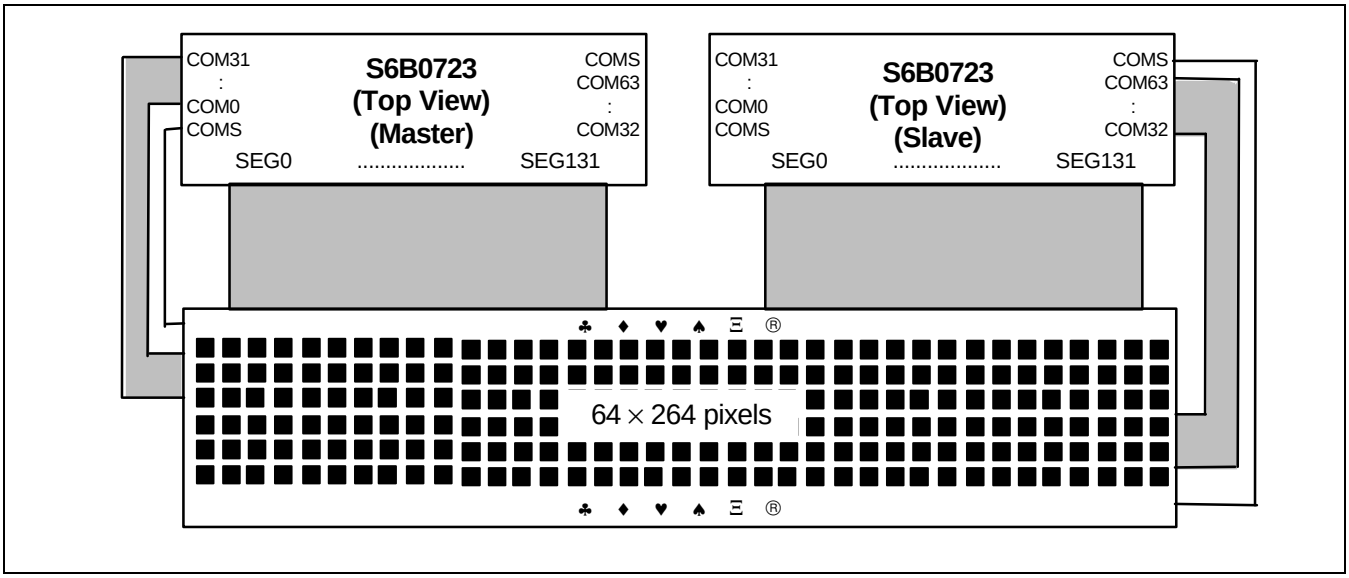


Figure 55. SHL = 0, ADC = 0

- Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

- 130COM (128COM + 2COMS) ´ 132SEG

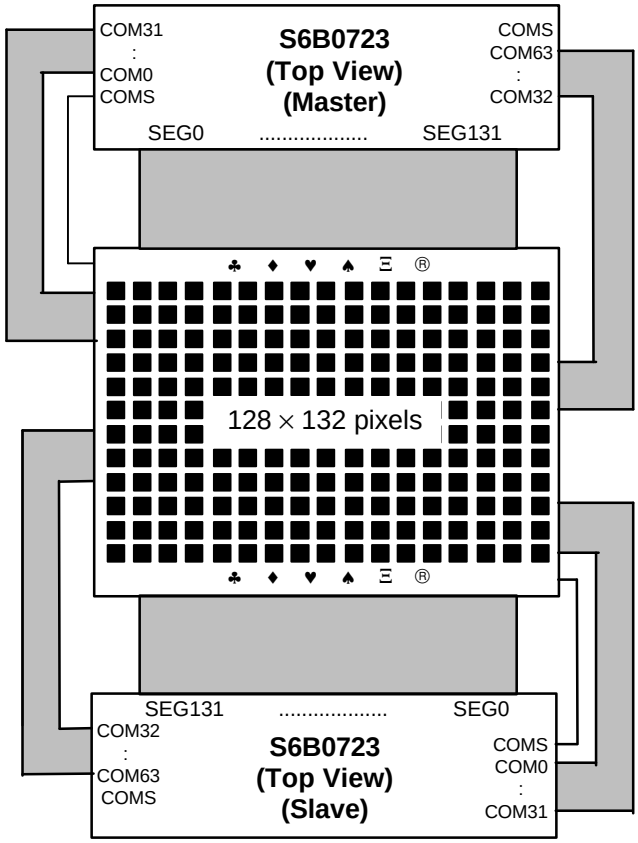


Figure 56. 130COM (128COM + 2COMS) ´ 132SEG

- Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

- Common/Segment output direction select
  - Master chip: SHL = 0, ADC = 0
  - Slave chip: SHL = 1, ADC = 1

S6B0723 APPLICATION CIRCUIT (6800 / 8080 / SERIAL)

S6B0723 Application Circuit for 6800-series

- **Package Type: TCP**
- **Device Mode: Master Mode, Internal OSC, Normal Mode, 4 Times Boost-up, Internal Rb / Ra**

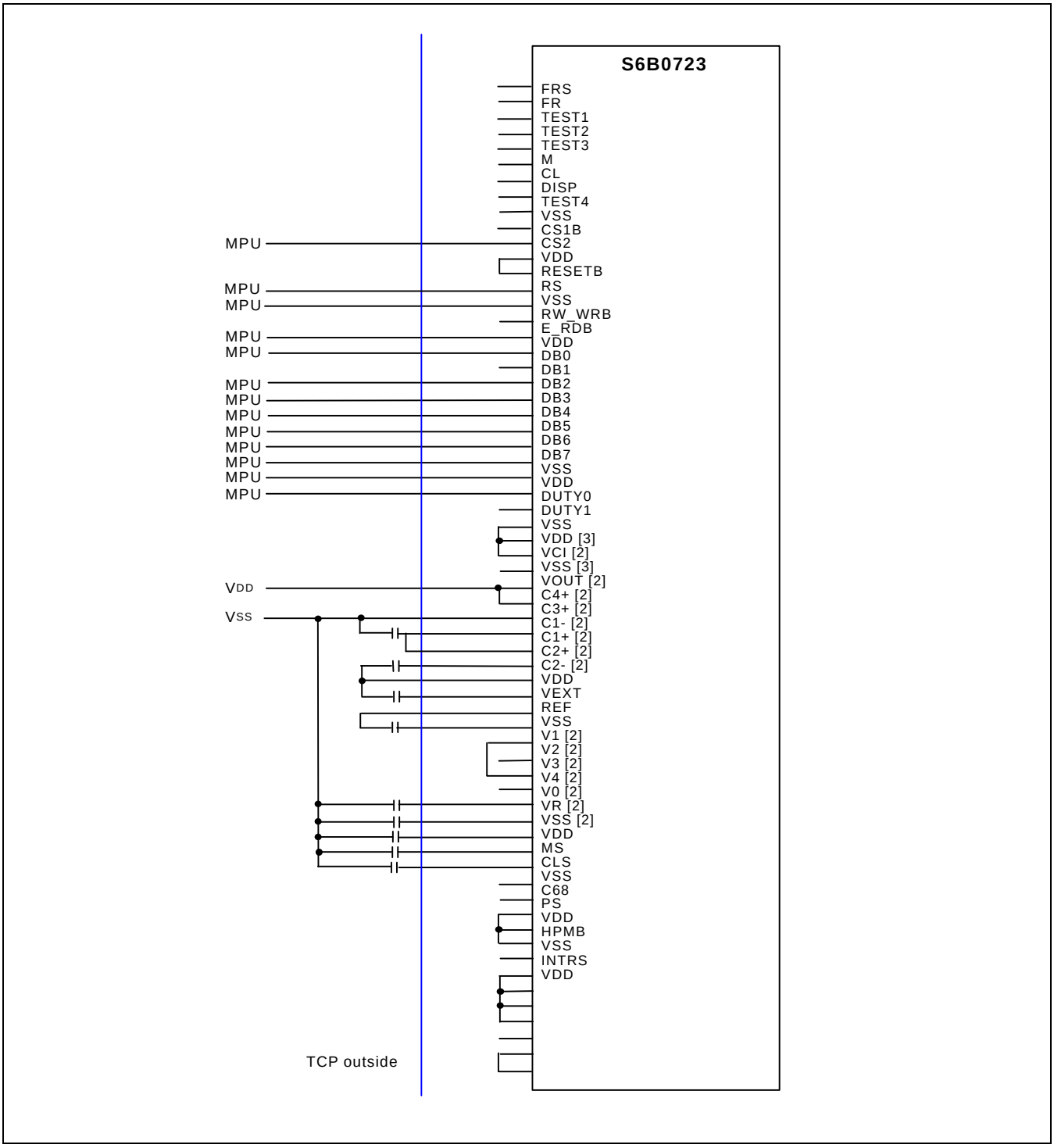


Figure 57. S6B0723 Application Circuit for 68-series

S6B0723 Application Circuit for 8080-series

- **Package Type: TCP**
- **Device Mode: Master Mode, Internal OSC, Normal Mode, 4 Times Boost-up, Internal Rb / Ra**

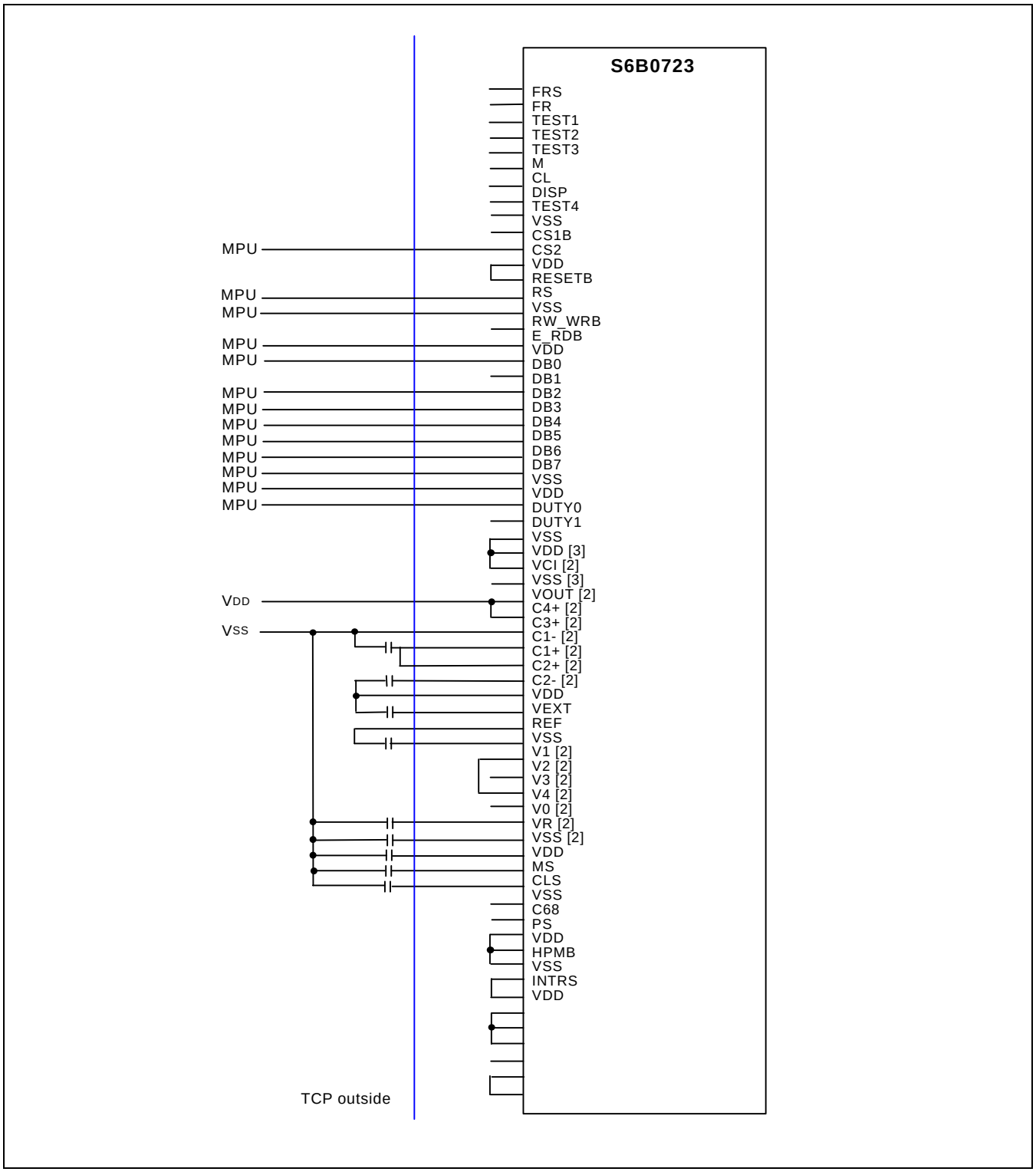


Figure 58. S6B0723 Application Circuit for 80-series

S6B0723 Application Circuit for Serial

- **Package Type: TCP**
- **Device Mode: Master Mode, Internal OSC, Normal Mode, 4 Times Boost-up, Internal Rb / Ra**

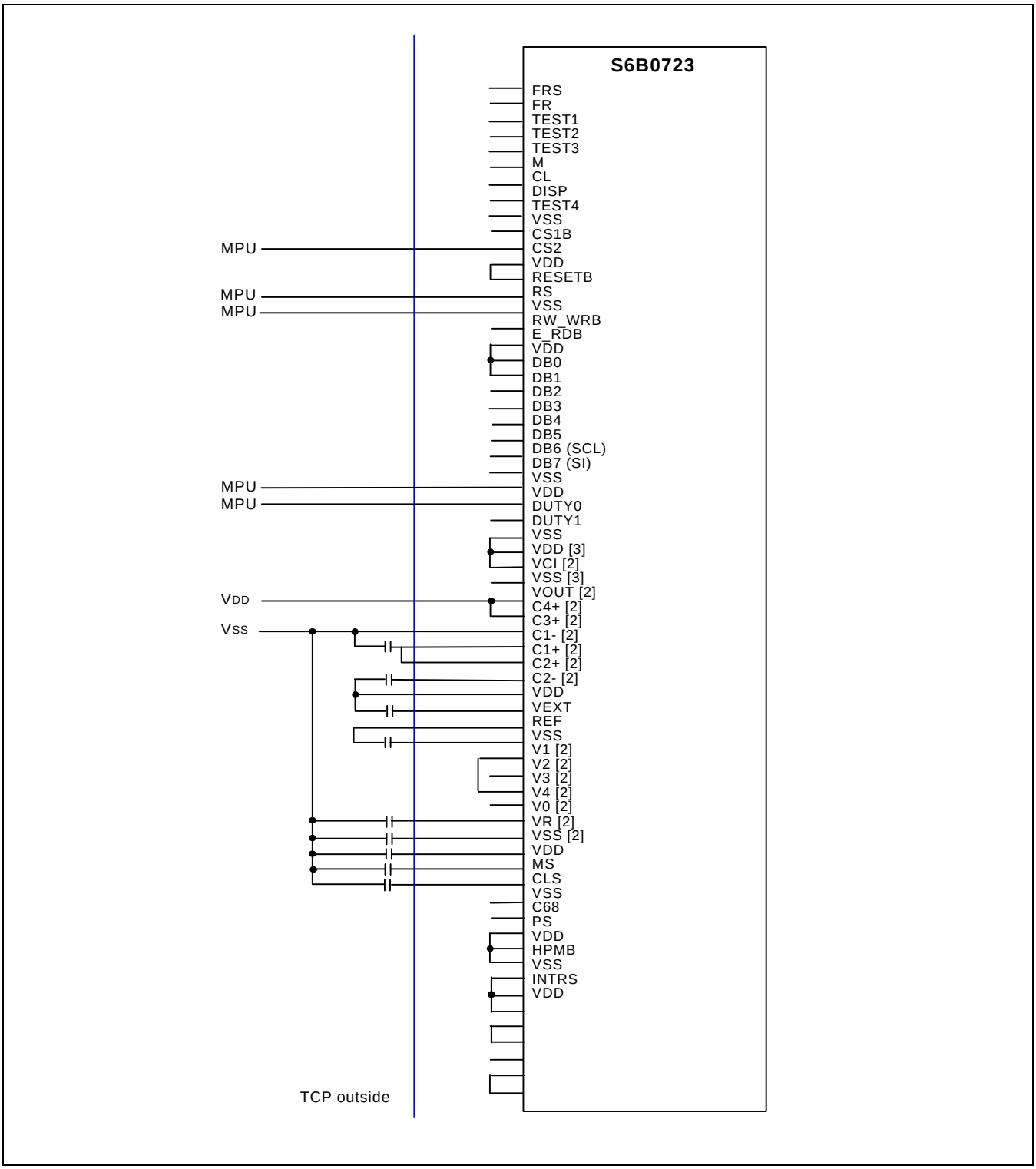


Figure 59. S6B0723 Application Circuit for Serial

TCP PIN LAYOUT (SAMPLE)

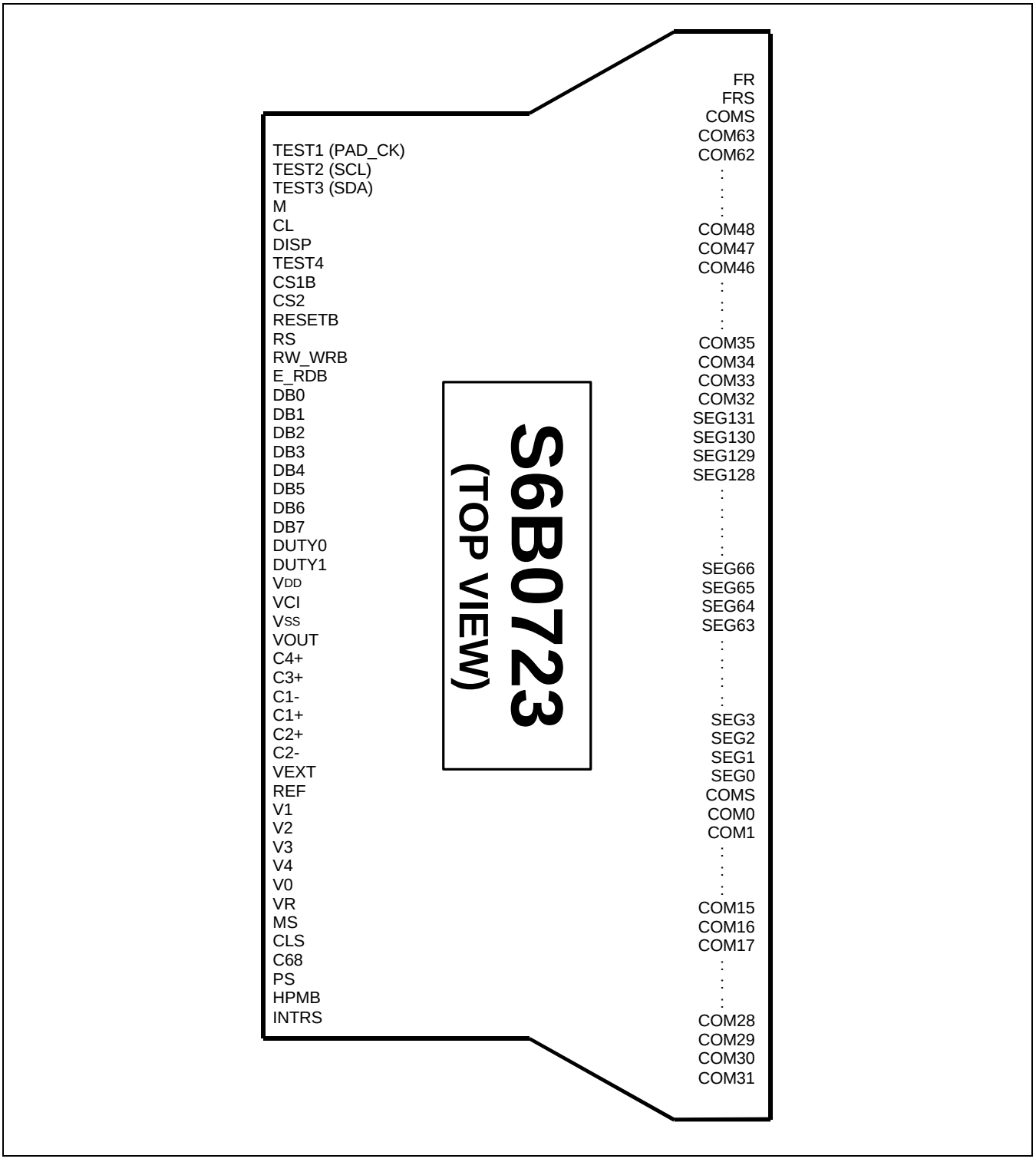


Figure 60. TCP Pin Layout