

Low-Voltage CMOS 16-Bit Microcontrollers TMP91CU10F

1. Outline and Device Characteristics

The TMP91CU10 is an original Toshiba TLCS-900/L1 Series 16-bit microcontroller. The TMP91CU10 integrates a 16-bit CPU, ROM, RAM, multi-functional timer and event counter, general-purpose serial interface, an A/D converter and various other units in a single chip, and has been developed for controlling medium- to large-scale equipment.

The TMP91CU10 is housed in a 100-pin mini flat package.

The device characteristics are as follows:

- (1) Original high-speed 16-bit CPU (900/H CPU)
 - TLCS-90/900 instruction mnemonics (upwards compatible)
 - 16-Mbyte linear address space
 - General-purpose registers and register bank system
 - 16-bit multiplication/division and bit transfer/arithmetic instructions
 - High-speed μ DMA: 4 channels (1.18 μ s at 13.5 MHz) (1.0 μ s at 16 MHz)
- (2) Minimum instruction execution time
 - 400 ns at 10 MHz ($V_{CC} = 2.0$ V) for mask ROM products only
 - 296 ns at 13.5 MHz ($V_{CC} = 3.0$ V)
- (3) Internal RAM: 3 Kbytes
Internal ROM: 96 Kbytes
- (4) External memory expansion
 - Can be expanded up to 16 Mbytes (for both programs and data).
 - $AM8/\overline{16}$ pin (selects the external data bus width)
 - Can mix 8- and 16-bit external data buses (dynamic bus sizing) .
- (5) Chip Select and Wait controller: 3 blocks
- (6) 8-bit timer: 8 channels
 - Including event count function: 2 channels
- (7) 16-bit timer and event counter: 2 channels
- (8) General-purpose serial interface: 3 channels
 - UART and Synchronous modes
- (9) (10-bit A/D converter: 8 channels

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
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(10) Watchdog timer

(11) Interrupt functions

- 2 CPU interrupts (SWI instruction and Illegal instruction)
- 26 internal interrupts 7-level priority can be set.
- 10 external interrupts 7-level priority can be set.

(12) I/O ports: 80 pins

(13) Standby function: 4 Halt modes (Run, Idle2, Idle1, Stop)

(14) Clock gear function

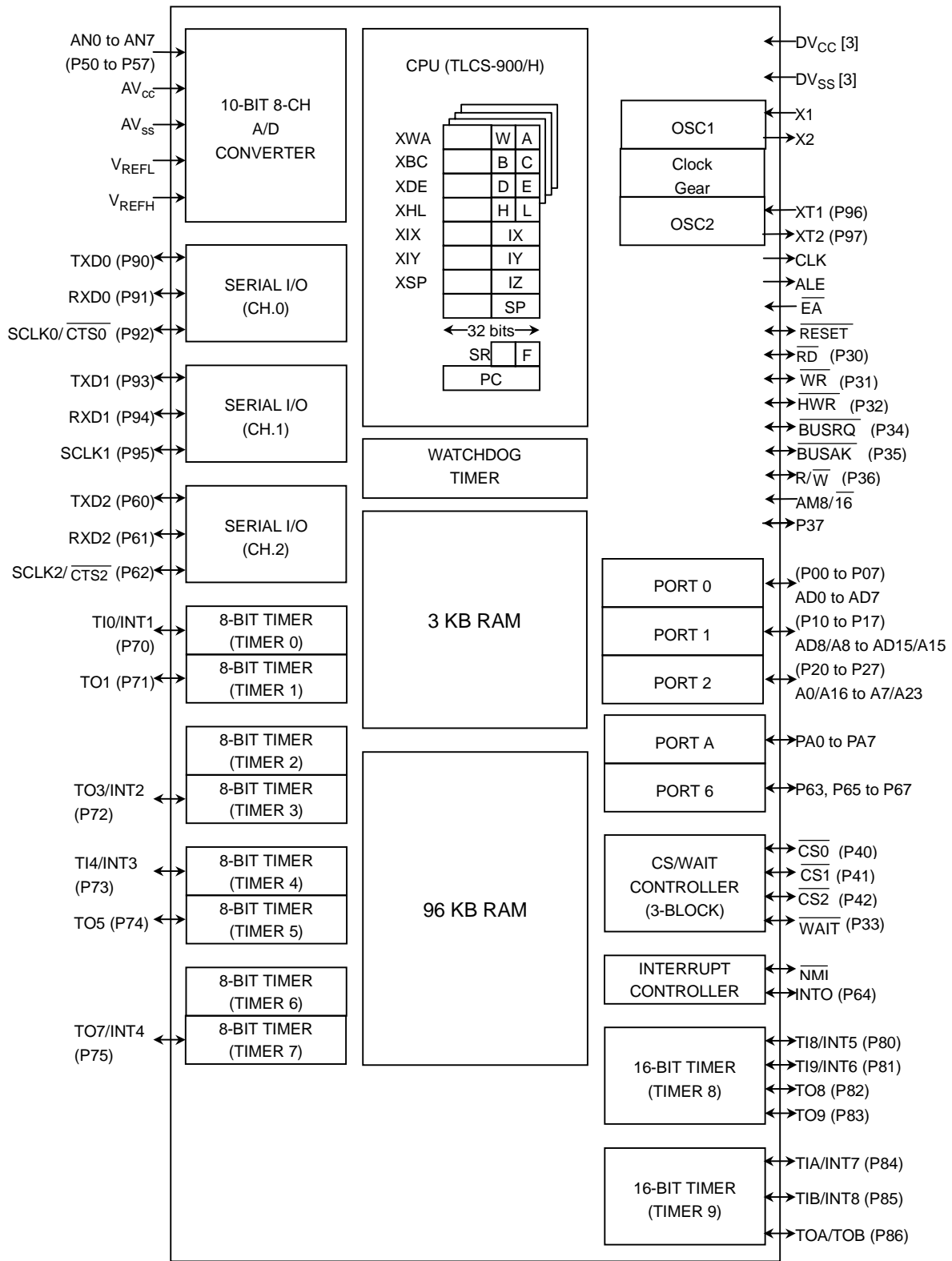
- Clock gear: High-frequency clock can be changed from f_c to $f_c/16$.
- Dual clock operation

(15) Low operating voltage

- 2.0 to 3.6 V

(16) Package

- Compact 14 mm × 14 mm × 1.4 mm (0.5 mm pitch)



() : Default function after reset

Figure 1.1 TMP91CU10F Block Diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP91CU10, their names and functions are described as follows:

2.1 Pin Assignment

Figure 2.1.1 shows the pin assignment of the TMP91CU10.

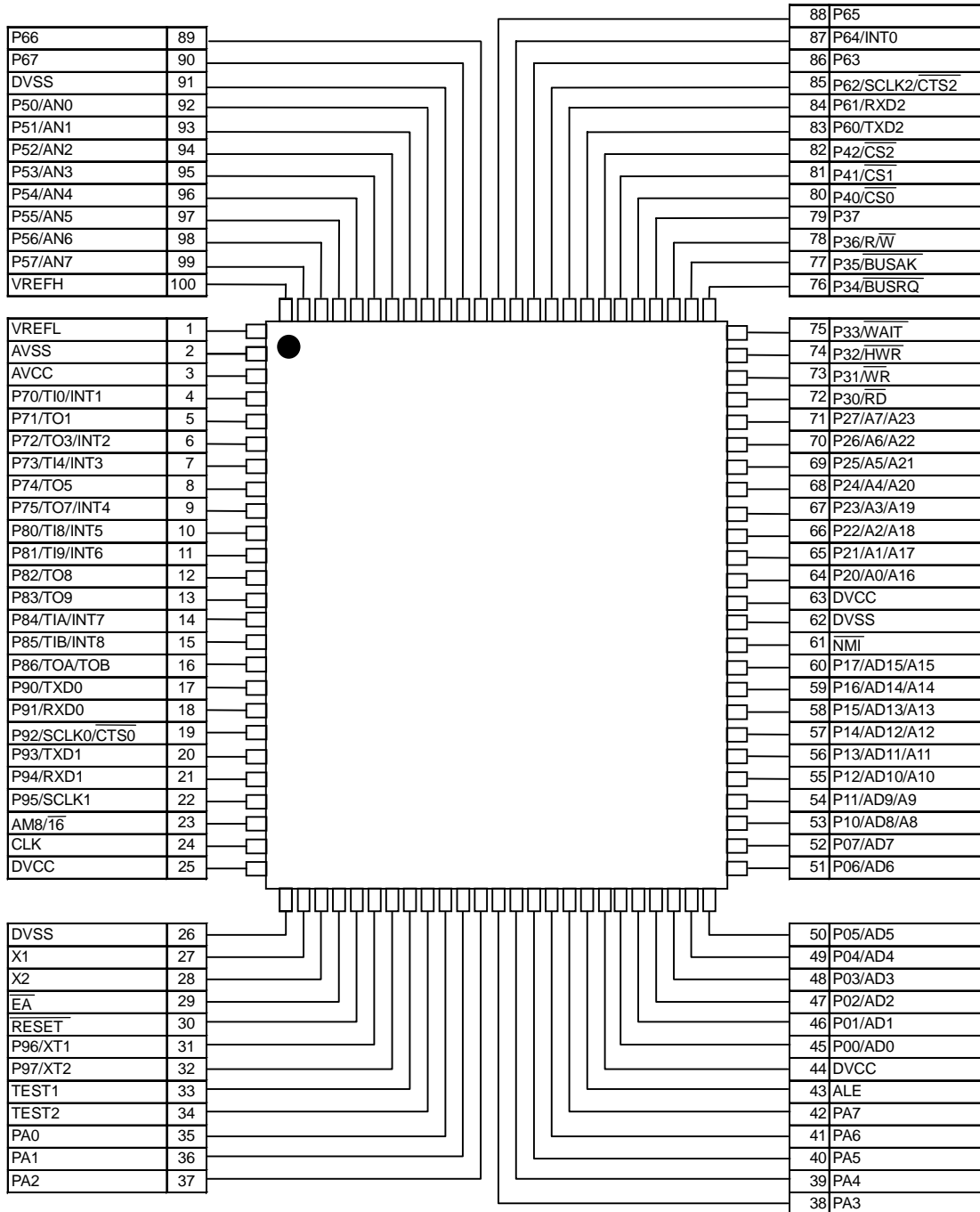


Figure 2.1.1 Pin Assignment diagram

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described in Table 2.2.1.

Table 2.2.1 Pin names and Functions (1/3)

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O I/O	Port 0: I/O port that allows I/O to be selected at the bit level Address (lower): Bits 0 to 7 for address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O I/O Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level (with pull-up resistor) Address: Bits 0 to 7 for address bus Address: Bits 16 to 23 for address bus
P30 \overline{RD}	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory When P3<RDE> = 0 and P3FC<P30F> = 1, \overline{RD} is output and internal memory is read.
P31 \overline{WR}	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins D0 to 7
P32 HWR	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data to pins D8 to D15
P33 \overline{WAIT}	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU Bus Wait
P34 \overline{BUSRQ}	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus Request: Signal used to request high impedance on pins D0 to D15, A0 to A23, \overline{RD} , \overline{WR} , HWR, $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$.
P35 \overline{BUSAK}	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus Acknowledge: Signal used to acknowledge high impedance on pins D0 to D15, A0 to A23, \overline{RD} , \overline{WR} , HWR, $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ by receiving \overline{BUSRQ} .
P36 R/ \overline{W}	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle.
P37	1	I/O	Port 37: I/O port
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip Select 0: Outputs 0 when address is within specified address area.
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip Select 1: Outputs 0 when address is within specified address area.
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-down resistor) Chip Select 2: Outputs 0 when address is within specified address area.
P50 to P57 ANO to AN7	8	Input Input	Port 5: Input port Analog input: Pin used to input to AD converter
P60 TXD2	1	I/O Output	Port 60: I/O port Serial Send Data 2 (programmable open drain)
P61 RXD2	1	I/O Input	Port 61: I/O port Serial Receive Data 2 (programmable open drain)
P62 SCLK2 $\overline{CTS2}$	1	I/O I/O Input	Port 62: I/O port Serial Clock I/O 2 Serial Data Send Enable 2 (Clear to Send) (programmable open drain)
P63	1	I/O	Port 63: I/O port
P64 INT0	1	I/O Input	Port 64: I/O port Interrupt Request pin 0: Interrupt request pin with programmable level/rising edge
P65 to P67	3	I/O	Port 65 to 67: I/O ports

Note: A DMAC controller's internal memory or I/O devices cannot be accessed using \overline{BUSRQ} and \overline{BUSAK} .

Table 2.2.1 Pin names and Function (2/3)

Pin name	Number of pins	I/O	Functions
P70 TI0 INT1	1	I/O Input Input	Port 70: I/O port Timer Input 0: Timer 0 input pin Interrupt Request pin 1: Interrupt request on rising edge
P71 TO1	1	I/O Output	Port 71: I/O port Timer Output 1: Timer 0 or 1 output
P72 TO3 INT2	1	I/O Output Input	Port 72: I/O port Timer Output 3: Timer 2 or 3 output Interrupt Request pin 2: Interrupt request on rising edge
P73 TI4 INT3	1	I/O Input Input	Port 74: I/O port Timer Input 4: Timer 4 input Interrupt Request pin 3: Interrupt request on rising edge
P74 TO5	1	I/O Output	Port 75: I/O port Timer Output 5: Timer 4 or 5 output
P75 TO7 INT4	1	I/O Output Input	Port 76: I/O port Timer Output 7: Timer 6 or 7 output Interrupt Request pin 4: Interrupt request on rising edge
P80 TI8 INT5	1	I/O Input Input	Port 80: I/O port Timer Input 8: Timer 8 count or capture trigger signal input Interrupt Request pin 5: Interrupt request pin with programmable rising / falling edge
P81 TI9 INT6	1	I/O Input Input	Port 81: I/O port Timer Input 9: Timer 8 count or capture trigger signal input Interrupt Request pin 6: Interrupt request on rising edge
P82 TO8	1	I/O Output	Port 82: I/O port Timer Output 8: Timer 8 output pin
P83 TO9	1	I/O Output	Port 83: I/O port Timer Output 9: Timer 9 output pin
P84 TIA INT7	1	I/O Input Input	Port 84: I/O port Timer Input A: Timer 9 count or capture trigger signal input Interrupt Request pin 7: Interrupt request pin with programmable rising / falling edge
P85 TIB INT8	1	I/O Input Input	Port 85: I/O port Timer Input B: Timer 9 count or capture trigger signal input Interrupt Request pin 8: Interrupt request on rising edge
P86 TOA TOB	1	I/O Output Output	Port 86: I/O port Timer Output A: Timer A output pin Timer Output B: Timer B output pin
P90 TXD0	1	I/O Output	Port 90: I/O port Serial Send Data 0 (programmable open drain)
P91 RXD0	1	I/O Input	Port 91: I/O port Serial Receive Data 0
P92 SCLK0 CTS0	1	I/O I/O Input	Port 92: I/O port Serial Clock I/O 0 Serial Data Send Enable 0 (Clear to Send)
P93 TXD1	1	I/O Output	Port 93: I/O port Serial Send Data 1 (programmable open drain)
P94 RXD1	1	I/O Input	Port 94: I/O port Serial Receive Data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port Serial Clock I/O 1
P96 XT1	1	I/O Input	Port 96: I/O port (open drain output) Low-frequency oscillator connecting pin
P97 XT2	1	I/O Output	Port 97: I/O port (open drain output) Low-frequency oscillator connecting pin

Table 2.2.1 Pin names and Function (3/3)

Pin name	Number of pins	I/O	Functions
PA0 to PA7	3	I/O	Port A0 to A7: I/O ports
ALE	1	Output	Address Latch Enable (can be disabled for reducing noise.)
$\overline{\text{NMI}}$	1	Input	Non-Maskable Interrupt Request pin: Interrupt request pin with programmable falling edge or both edges.
CLK	1	Output	Clock Output: Outputs (external input clock/4) clock. Pulled-up during reset
$\overline{\text{EA}}$	1	Input	The Vcc pin should be connected.
AM8/ $\overline{\text{16}}$	1	Input	Address Mode: Selects external data bus width. The Vcc pin should be connected. The data bus width for external access is set by the Chip Select/WAIT Control register and the Port 1 Control register.
TEST1/TEST2	2	Output /Input	TEST1 Should be connected with TEST2 pin.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
VREFH	1	Input	Reference power supply input pin for AD converter (H)
VREFL	1	Input	Reference power supply input pin for AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND power supply pin for AD converter (0 V)
X1/X2	2	I/O	Oscillator connecting pin
TEST1/TEST2	2	Output /Input	TEST1 should be connected with TEST2 pin.
DVCC1	3		Power supply pin
DVSS	3		GND pin (0 V)

Note: All pins that have built-in pull-up / pull-down resistors (other than the $\overline{\text{RESET}}$ pin) can be disconnected from their built-in pull-up / pull-down resistors by software.

3. Operation

This section describes the functions and basic operations of the TMP91CU10. Please also refer to Section 7, Precautions, which describes some points requiring careful attention.

3.1 CPU

TMP91CU10 device has a built-in high-performance 16-bit CPU (TLCS-900/L1 CPU). (For a basic description of the CPU operation, see the information on the TLCS-900/L1 CPU).

This section describes some CPU functions unique to the TMP91CU10 that are not described in the description of the TLCS-900/L1 CPU.

3.1.1 Reset

Figure 3.1.1 shows the basic timing chart for a Reset operation.

To reset a TMP91CU10 device, the $\overline{\text{RESET}}$ pin must be kept at 0 for at least ten consecutive system clock cycles (equivalent to 160 states: 24 μs at 13.5 MHz). The pin must be kept within the specified operating voltage range and stable clock oscillation must be maintained.

When a Reset signal is received, the CPU is set as follows:

- The Program Counter (PC) is set according to the Reset Vector that is stored from FFFF00H to FFFF02H.
PC (7 to 0) \leftarrow data in location FFFF00H
PC (15 to 8) \leftarrow data in location FFFF01H
PC (23 to 16) \leftarrow data in location FFFF02H
- The Stack Pointer (XSP) for System mode is set to 100H.
- The <IFF2 to 0> bits of the Status register SR are set to 111. (The Mask register is set to interrupt level 7.)
- The <MAX> bit of SR is set to 1 (Maximum mode).
(Note: This device does not support Minimum mode. Do not set <MAX> to 0.)
- The <REP2 to 0> bits of SR are set to 000. (The register banks are cleared to 0.)

When the Reset is released, instruction execution starts from PC (the Reset Vector). The Reset makes no changes to the values in any CPU internal registers other than those specifically mentioned above.

When a Reset is received, signal and data processing for built-in I/Os, ports and other pins is affected as follows:

- Initializes built-in I/O registers as described in the specifications.
- Sets port pins (including pins also used as built-in I/Os) to General-Purpose Input/Output Port mode.
- Pulls up the CLK pin to 1.
- Sets the ALE pin to High Impedance (Hi-Z).

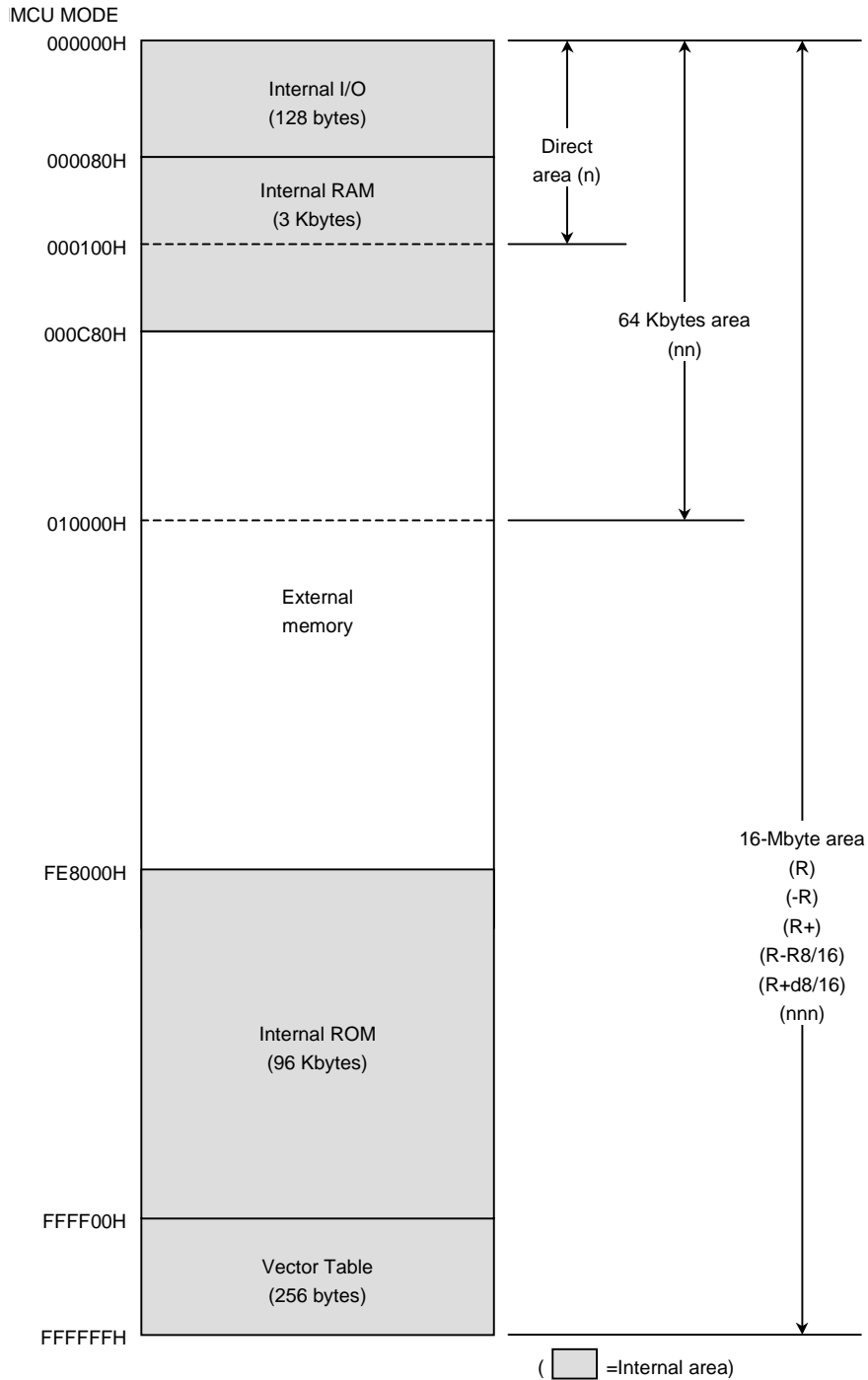
Note 1: Resetting makes no change to the contents of any register in the CPU except the Program Counter (PC), Status Register (SR) and Stack Pointer (XSP), nor to the data in the internal RAM.

Note 2: The CLK pin is pulled up during a Reset. When the voltage is externally reduced, there is a possibility of malfunction.

3.2 Memory Map

The TMP91CU10 uses an address area of 128 bytes as the internal I/O area, which is allocated from addresses 000000H to 00007FH. The CPU can access this internal I/O using a short internal code in Direct Addressing Mode.

Figure 3.2.1 shows the memory map and the accessible area for each CPU addressing mode.



Note: The stack pointer XSP is set to 100H after a Reset.

Figure 3.2.1 TMP91CU10 Memory Map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

“X” used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>. The value of X changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for f_c , with gear=1/ f_c (SYSCR1<SYSCK, GEAR2 to 0>=0000).

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V _{CC}	-0.5 to 4.0	V
Input Voltage	V _{IN}	-0.5 to V _{CC} + 0.5	V
Output Current (total)	ΣI _{OL}	120	mA
Output Current (total)	ΣI _{OH}	-80	mA
Power Dissipation (Ta=85°C)	PD	600	mW
Soldering Temperature (10 s)	TSOLDER	260	°C
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	-40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note1)	Max	Unit
Power Supply Voltage AV _{CC} =V _{CC} AV _{SS} =V _{SS} =0V		V _{CC}	f _c = 4 to 16 MHz f _s = 30 to 34 kHz (Ta = -40 to 85°C)	2.7		3.6	V
			f _c = 4 to 10 MHz f _s = 30 to 34 kHz (Ta = -40 to 85°C)	2.2 (Note 2)			
Input Low Voltage	AD0 to 15	V _{IL}	V _{CC} ≥ 2.7 V V _{CC} < 2.7 V			0.8 0.4	V
	Port2 to A(exceptP87, P5)	V _{IL1}		-0.3		0.3 V _{CC}	
	RESET, NIMI, INT0	V _{IL2}	V _{CC} = 2.7 to 3.6 V			0.25 V _{CC}	
	EA, AM8/16	V _{IL3}				0.3	
	X1, Port5	V _{IL4}				0.2 V _{CC}	
Input High Voltage	AD0 to 15	V _{IH}	V _{CC} ≥ 2.7 V V _{CC} < 2.7 V		2.2 2.0		V _{CC} +0.3
	Port2 to A(exceptP87)	V _{IH1}		0.7 V _{CC}			
	RESET, NIMI, INT0	V _{IH2}	V _{CC} = 2.7 to 3.6 V	0.75 V _{CC}			
	EA, AM8/16	V _{IH3}		V _{CC} -0.3			
	X1	V _{IH4}		0.8 V _{CC}			

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

Note 2: The operation of the A/D converter is guaranteed at V_{CC} = 2.7 to 3.6 V.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note1)	Max	Unit
Output Low Voltage	VOL	IOL = 1.6 mA (Vcc = 2.7 to 3.6 V)			0.45	V
Output High Voltage	VOH1	IOH = -400 μ A (Vcc = 2.2 V \pm 10%)	1.4			
	VOH2	IOH = -400 μ A (Vcc = 3 V \pm 10 %)	2.4			
Darlington Drive Current (8 Output Pins max.)	IDAR (Note2)	VEXT = 1.5 V REXT = 1.1 k Ω (Vcc = 3 V \pm 10%)	-1.0		-3.5	mA
Input Leakage Current	ILI	0.0 \leq VIN \leq Vcc		0.02	\pm 5	μ A
Output Leakage Current	ILO	0.2 \leq VIN \leq Vcc-0.2		0.05	\pm 10	
Power Down Voltage (@STOP, RAM Back up)	VSTOP	VIL2 = 0.2 Vcc, VIH2 = 0.8 Vcc	2.0		6.0	V
RESET Pull Up Resister	RRST	Vcc = 3 V \pm 10%	50		250	k Ω
		Vcc = 2.2 V \pm 10%	80		500	
Pin Capacitance	CIO	fc = 1 MHz			10	pF
Schmitt Width RESET, NIMI, INT0	VTH		0.4	1.0		V
Programmable Pull Down Resistor	PKL	Vcc = 3 V \pm 10%	30		200	k Ω
		Vcc = 2.2 V \pm 10%	80		500	
Programmable Pull Up Resistor	PKH	Vcc = 3 V \pm 10%	80		300	k Ω
		Vcc = 2.2 V \pm 10%	80		500	
NORMAL2	Icc	Vcc = 3 V \pm 10% fc = 13.5 MHz (Typ. : Vcc = 3.0 V)		14	23	mA
RUN				10	17	
IDLE2				6	11	
IDLE1				1.1	2.8	
NORMAL2		Vcc = 2.2 V \pm 10% fc = 10 MHz (Typ. : Vcc = 2.2 V)		8.0	12	mA
RUN				4.5	9.5	
IDLE2				2.5	6.5	
IDLE1				0.5	1.5	
SLOW		Vcc = 3 V \pm 10% fs = 32.768 kHz (Typ. : Vcc = 3.0 V)		40	55	μ A
RUN				32	45	
IDLE2				18	35	
IDLE1				6	20	
STOP	Ta \leq 50°C	Vcc = 2.0 to 3.6 V		0.2	10	μ A
	Ta \leq 70°C		20			
	Ta \leq 85°C		50			

Note 1: Typical values are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

Note 2: I-DAR is guaranteed for up to eight ports.

Note 3: ICC measurement condition (NORMAL2):

All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) $V_{CC} = 2.5$ to 3.6 V

No.	Parameter	Symbol	Variable		12.5 MHz		16 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (=x)	t_{OSC}	62.5	31250	80		74		ns
2	CLK width	t_{CLK}	$2x - 40$		120		108		ns
3	A0 to A23 Valid→CLK Hold	t_{AK}	$0.5x - 20$		20		7		ns
4	CLK Valid→A0 to A23 Hold	t_{KA}	$1.5x - 70$		50		26		ns
5	A0 to A15 Valid→ALE Fall	t_{AL}	$0.5x - 15$		25		30		ns
6	ALE Fall→A0 to A15 Hold	t_{LA}	$0.5x - 20$		20		7		ns
7	ALE High Width	t_{LL}	$x - 40$		40		24		ns
8	ALE Fall→ \overline{RD} / \overline{WR} Fall	t_{LC}	$0.5x - 25$		15		10		ns
9	\overline{RD} / \overline{WR} Rise→ALE Rise	t_{CL}	$0.5x - 20$		20		7		ns
10	A0 to A15 Valid→ \overline{RD} / \overline{WR} Fall	t_{ACL}	$x - 25$		55		34		ns
11	A0 to A23 Valid→ \overline{RD} / \overline{WR} Fall	t_{ACH}	$1.5x - 50$		70		61		ns
12	\overline{RD} / \overline{WR} Rise→A0 to A23 Hold	t_{CA}	$0.5x - 25$		15		0		ns
13	A0 to A15 Valid→D0 to D15 Input	t_{ADL}		$3.0x - 55$		130		182	ns
14	A0 to A23 Valid→D0 to D15 Input	t_{ADH}		$3.5x - 65$		215		194	ns
15	\overline{RD} Fall→D0 to D15 Input	t_{RD}		$2.0x - 60$		100		103	ns
16	\overline{RD} Low Pulse Width	t_{RR}	$2.0x - 40$		120		108		ns
17	\overline{RD} Rise→D0 to D15 Hold	t_{HR}	0		0		0		ns
18	\overline{RD} Rise→A0 to A15 Output	t_{RAE}	$x - 15$		65		54		ns
19	\overline{WR} Low Pulse Width	t_{WW}	$2.0x - 40$		120		108		ns
20	D0 to D15 Valid→ \overline{WR} Rise	t_{DW}	$2.0x - 55$		105		68		ns
21	\overline{WR} Rise→D0 to D15 Hold	t_{WD}	$0.5x - 15$		25		5		ns
22	A0 to A23 Valid→ \overline{WAIT} Input (1WAIT + n mode)	t_{AWH}		$3.5x - 90$		190		199	ns
23	A0 to A15 Valid→ \overline{WAIT} Input (1WAIT + n mode)	t_{AWL}		$3.0x - 80$		160		162	ns
24	\overline{RD} / \overline{WR} Fall→ \overline{WAIT} Hold (1WAIT + n mode)	t_{CW}	$2.0x + 0$		160		148		ns
25	A0 to A23 Valid→PORT Input	t_{APH}		$2.5x - 120$		80		65	ns
26	A0 to A23 Valid→PORT Hold	t_{APH2}	$2.5x + 50$		250		235		ns
27	\overline{WR} Rise→PORT Valid	t_{CP}		200		200		359	ns

AC Measuring Conditions

- Output Level: High 2.2 V/Low 0.8 V, $CL=50$ pF
(However, $CL = 100$ pF for AD0 to AD15, A0 to A23, ALE \overline{RD} , \overline{WR} , \overline{HWR} , R/\overline{W} , \overline{CLK})
- Input Level: High 2.4 V/Low 0.45 V (AD0 to AD15)
High 0.8 Vcc/Low 0.2 Vcc (except for AD0 to AD15)

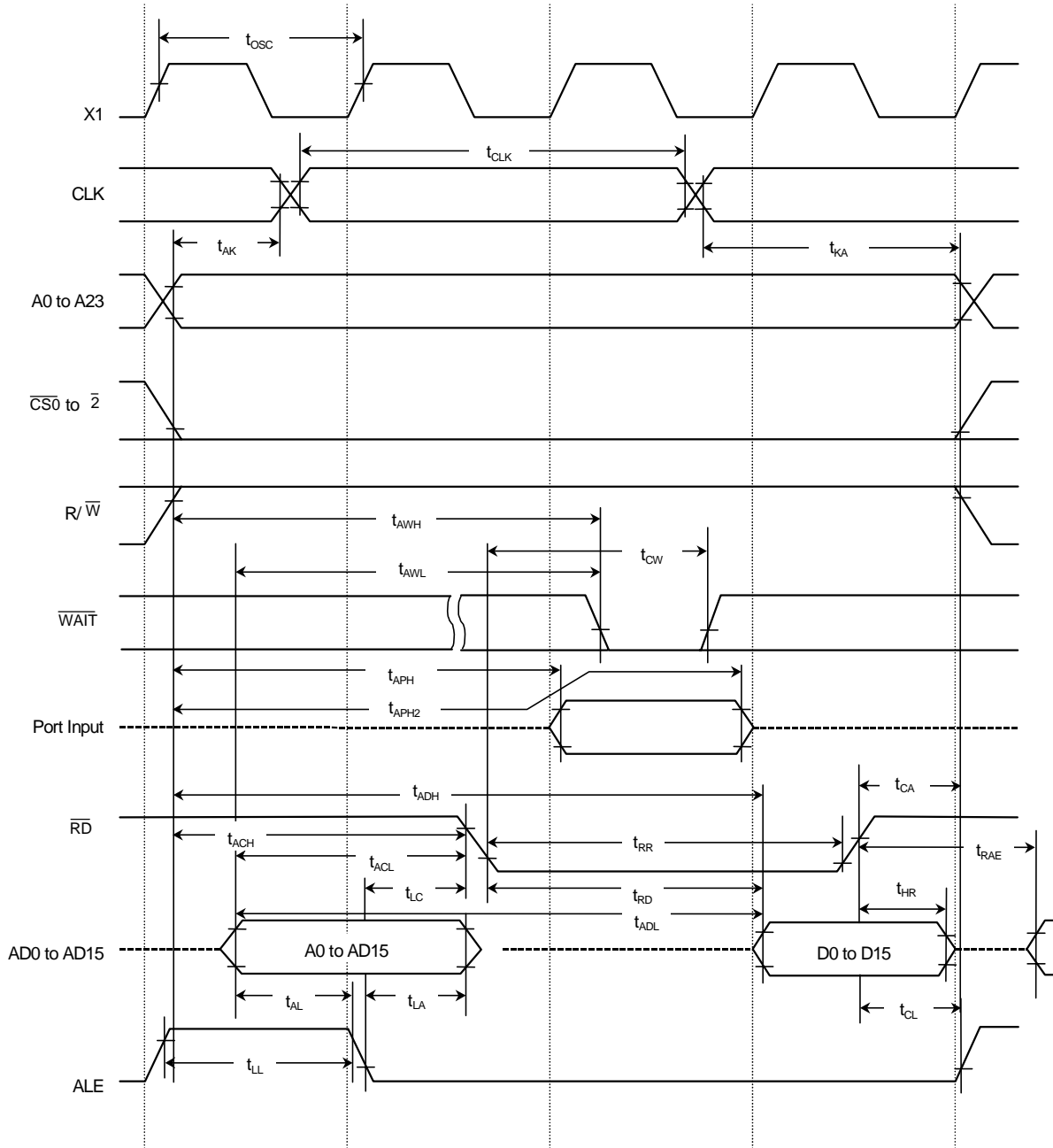
(2) $V_{CC} = 2.2 \text{ V} \pm 10 \%$

No.	Parameter	Symbol	Variable		10 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (=x)	t_{OSC}	100	31250	100		ns
2	CLK width	t_{CLK}	$2x - 40$		160		ns
3	A0 to A23 Valid→CLK Hold	t_{AK}	$0.5x - 30$		20		ns
4	CLK Valid→A0 to A23 Hold	t_{KA}	$1.5x - 80$		70		ns
5	A0 to A15 Valid→ALE Fall	t_{AL}	$0.5x - 35$		15		ns
6	ALE Fall→A0 to A15 Hold	t_{LA}	$0.5x - 35$		15		ns
7	ALE High Width	t_{LL}	$x - 60$		40		ns
8	ALE Fall→ \overline{RD} / \overline{WR} Fall	t_{LC}	$0.5x - 35$		15		ns
9	\overline{RD} / \overline{WR} Rise→ALE Rise	t_{CL}	$0.5x - 40$		10		ns
10	A0 to A15 Valid→ \overline{RD} / \overline{WR} Fall	t_{ACL}	$x - 50$		50		ns
11	A0 to A23 Valid→ \overline{RD} / \overline{WR} Fall	t_{ACH}	$1.5x - 50$		100		ns
12	\overline{RD} / \overline{WR} Rise→A0 to A23 Hold	t_{CA}	$0.5x - 40$		10		ns
13	A0 to A15 Valid→D0 to D15 Input	t_{ADL}		$3.0x - 110$		190	ns
14	A0 to A23 Valid→D0 to D15 Input	t_{ADH}		$3.5x - 125$		225	ns
15	\overline{RD} Fall→D0 to D15 Input	t_{RD}		$2.0x - 115$		85	ns
16	\overline{RD} Low Pulse Width	t_{RR}	$2.0x - 40$		160		ns
17	\overline{RD} Rise→D0 to D15 Hold	t_{HR}	0		0		ns
18	\overline{RD} Rise→A0 to A15 Output	t_{RAE}	$x - 25$		75		ns
19	\overline{WR} Low Pulse Width	t_{WW}	$2.0x - 40$		160		ns
20	D0 to D15 Valid→ \overline{WR} Rise	t_{DW}	$2.0x - 120$		80		ns
21	\overline{WR} Rise→D0 to D15 Hold	t_{WD}	$0.5x - 40$		10		ns
22	A0 to A23 Valid→ \overline{WAIT} Input (1WAIT + n mode)	t_{AWH}		$3.5x - 130$		220	ns
23	A0 to A15 Valid→ \overline{WAIT} Input (1WAIT + n mode)	t_{AWL}		$3.0x - 100$		200	ns
24	\overline{RD} / \overline{WR} Fall→ \overline{WAIT} Hold (1WAIT + n mode)	t_{CW}	$2.0x + 0$		200		ns
25	A0 to A23 Valid→PORT Input	t_{APH}		$2.5x - 120$		130	ns
26	A0 to A23 Valid→PORT Hold	t_{APH2}	$2.5x + 50$		200		ns
27	\overline{WR} Rise→PORT Valid	t_{CP}		200		200	ns

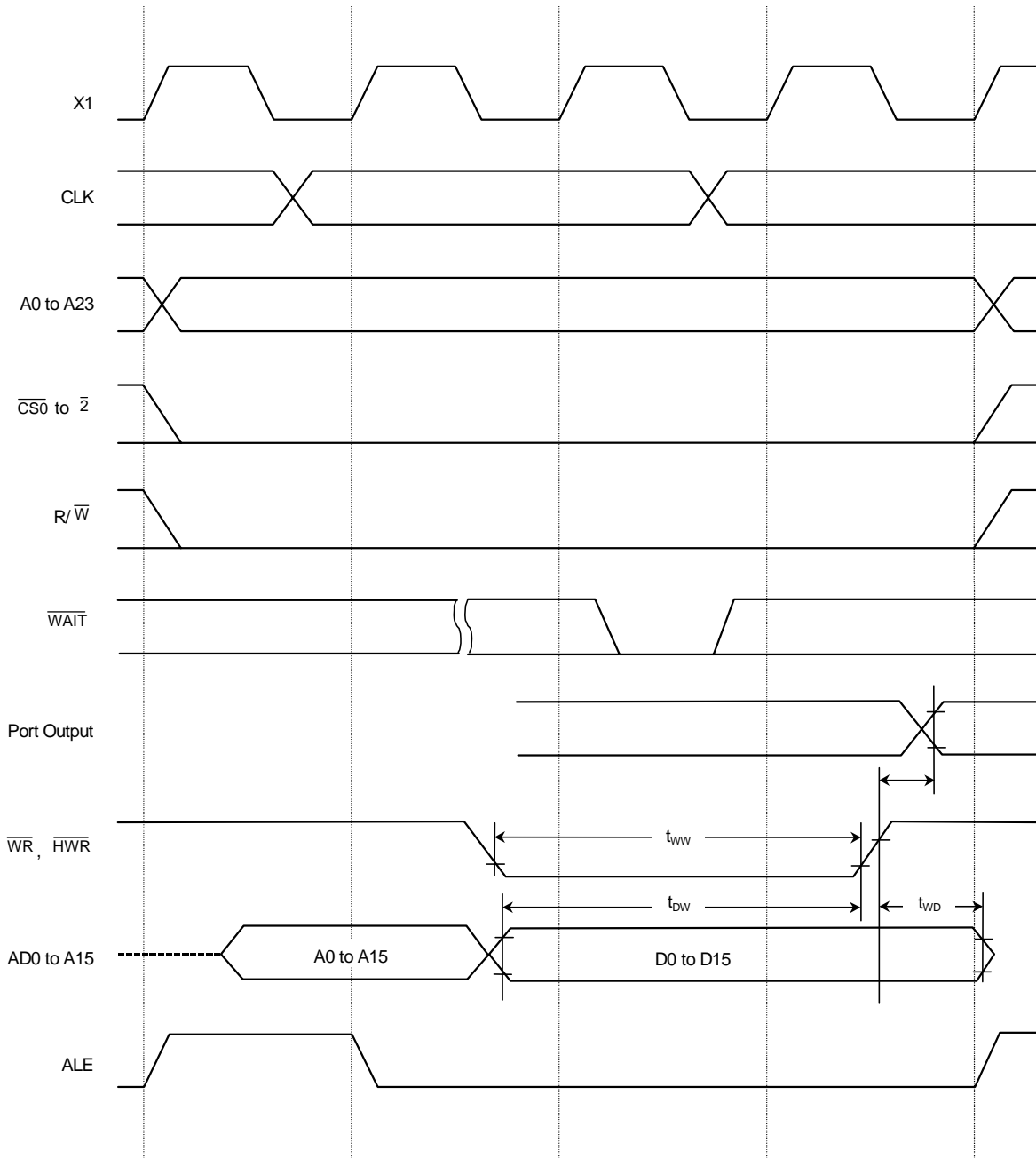
AC Measuring Conditions

- Output Level: High $\times 0.7 V_{CC}$ /Low $0.3 \text{ V} \times V_{CC}$, CL = 50 pF
- Input Level: High $\times 0.9 V_{CC}$ /Low $0.1 \text{ V} \times V_{CC}$

(3) Read Cycle



(4) Write Cycle



4.4 A/D Conversion Characteristics

AVCC = VCC, AVSS = VSS

Parameter	Symbol	Min	Typ.	Max	Unit
Analog Reference Voltage (+)	V_{REFH}	$V_{CC} - 0.2 \text{ V}$	V_{CC}	V_{CC}	V
Analog Reference Voltage (-)	V_{REFL}	V_{SS}	V_{SS}	$V_{SS} + 0.2 \text{ V}$	
Analog Input Voltage Range	V_{AIN}	V_{REFL}		V_{REFH}	
Analog Current for Analog Reference Voltage $V_{CC} = 3 \text{ V} \pm 10\%$ $\langle V_{REFON} \rangle = 1$	I_{REF} ($V_{REFL} = 0$)		0.5	1.5	mA
$V_{CC} = 3 \text{ V} \pm 10\%$ $\langle V_{REFON} \rangle = 0$	V)		0.02	5.0	μA
Error (not including quantizing errors)	—		± 1	± 3	LSB

Note 1: $1\text{LSB} = (V_{REFH} - V_{REFL}) / 2^{10} \text{ [V]}$

Note 2: The operation of the A/D converter is guaranteed only when f_c (the high frequency oscillator) is used (it is not guaranteed when f_s is used). It is guaranteed when $f_{FPH} \geq 4 \text{ MHz}$.

Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

Note 4: The operation of the TMP91CU10 is guaranteed within 2.7 to 3.6 V.

4.5 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

Parameter	Symbol	Variable		32.768 kHz ^{Note)}		13.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle	t_{SCY}	16x		488 μ s		1.18		μ s
Output Data → Rising Edge or Falling Edge* of SCLK	t_{OSS}	$t_{SCY}/2-5x-50$		91.5 μ s		172		ns
SCLK Rising Edge or Falling Edge* →Output Data Hold	t_{OHS}	5x-100		152 μ s		270		ns
SCLK Rising Edge or Falling Edge* →Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising Edge or Falling Edge* →Effective Data Input	t_{SRD}		$t_{SCY}-5x-100$		336 μ s		714	ns

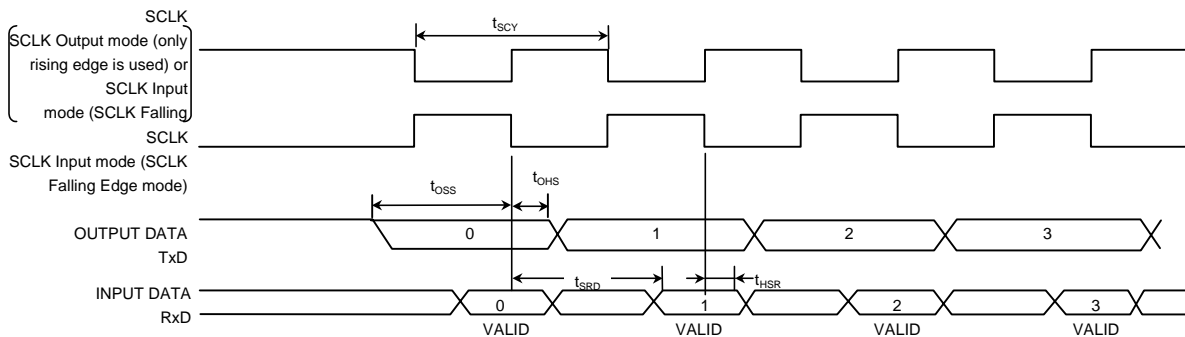
Note: System clock is fs, or input clock to prescaler is divisor clock of fs.

*) The rising edge is used in SCLK Rising mode. The falling edge is used SCLK Falling mode.

② SCLK Output mode

Parameter	Symbol	Variable		32.768 kHz ^{Note)}		13.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle (Programmable)	t_{SCY}	16x	8192x	488 μ s	250 ms	1.18	655.4	μ s
Output Data → SCLK Rising Edge	t_{OSS}	$t_{SCY}/2-5x-50$		427 μ s		886		ns
SCLK Rising Edge→ Output Data Hold	t_{OHS}	2x-80		60 μ s		68		ns
SCLK Rising Edge→ Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising Edge→ Effective Data Input	t_{SRD}		$t_{SCY}-2x-150$		428 μ s		886	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.



4.6 Event Counter (TI0, TI4, TI8, TI9, TIA, TIB)

Parameter	Symbol	Variable		13.5 MHz		Unit
		Min	Max	Min	Max	
Clock Cycle	t_{VCK}	$8X + 100$		692		ns
Low Level Clock Pulse Width	t_{VCKL}	$4X + 40$		336		ns
High Level Clock Pulse Width	t_{VCKH}	$4X + 40$		336		ns

4.7 Interrupt and Capture

(1) \overline{NMI} , INT0 interrupts

Parameter	Symbol	Variable		13.5 MHz		Unit
		Min	Max	Min	Max	
\overline{NMI} , INT0 to 4 Low Level Pulse Width	t_{INTAL}	$4X$		296		ns
\overline{NMI} , INT0 High Level Pulse Width	t_{INTAH}	$4X$		296		ns

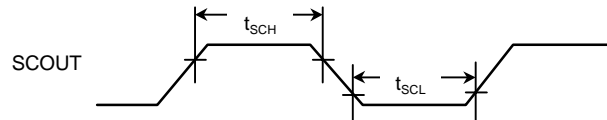
(2) INT5 to 8 interrupts, capture

The INT4 to 7 input pulse width depends on the CPU operation clock and timer (9-bit prescaler). The following shows the pulse width for each clock.

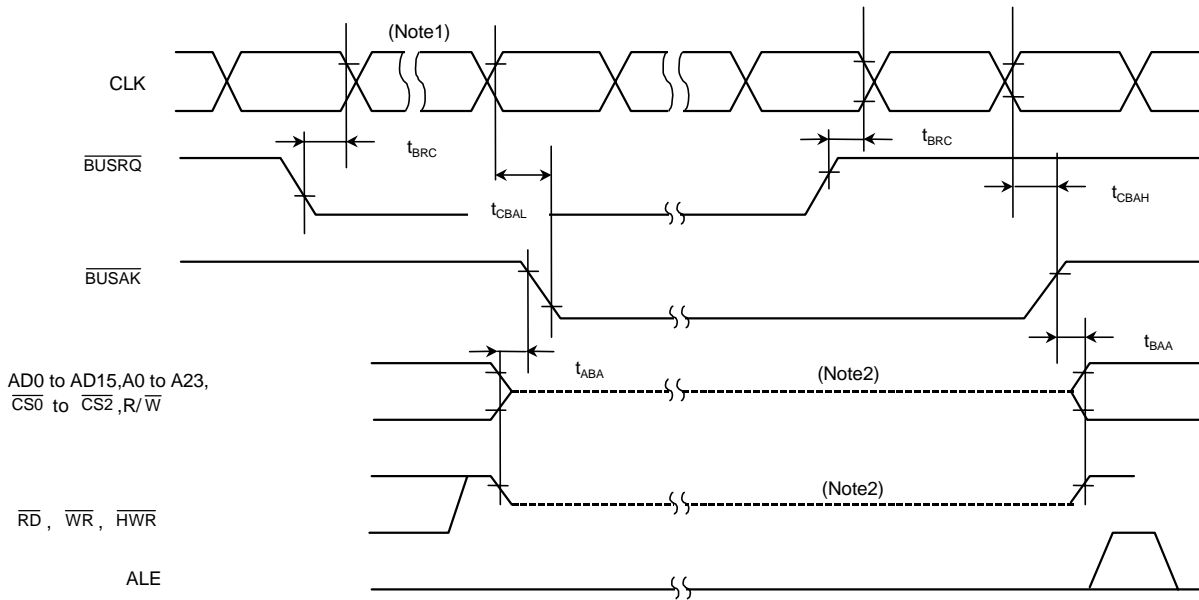
System clock selected <SYSCK>	Prescaler clock selected <PRCK1 to 0>	t_{INTBL} (INT5 to 8 low level pulse width)		t_{INTBH} (INT5 to 8 high level pulse width)		Unit
		Variable	13.5 MHz	Variable	13.5 MHz	
		Min	Min	Min	Min	
0(f_c)	00 (f_{FPH})	$8X + 100$	692	$8X + 100$	692	ns
	01 (f_s)	$8XT + 0.1$	244.3	$8XT + 0.1$	244.3	
	10 ($f_c/16$)	$128X + 0.1$	9.572	$128X + 0.1$	9.572	
1 (f_s) ^(Note 2)	00 (f_{FPH})	$8XT + 0.1$	244.3	$8XT + 0.1$	244.3	μs
	01 (f_s)					

Note 1: XT represents the frequency of the low frequency clock f_s . Calculated at $f_s = 32.768$ kHz.

Note 2: When using f_s as the system clock, $f_c/16$ cannot be selected as the prescaler clock.



4.8 Timing Chart for Bus Request / Bus Acknowledge



Parameter	Symbol	Variable		13.5 MHz		Unit
		Min	Max	Min	Max	
\overline{BUSRQ} BUSRQ Set-up Time to CLK	t_{BRC}	120		120		ns
CLK → \overline{BUSAK} BUSAK Falling Edge	t_{CBAL}		$1.5x + 120$		231	ns
CLK → \overline{BUSAK} BUSAK Rising Edge	t_{CBAH}		$0.5x + 40$		77	ns
Output Buffer off to BUSAK	t_{ABA}	0	80	0	80	ns
BUSAK to Output Buffer on	t_{BAA}	0	80	0	80	ns

Note 1: Even if the \overline{BUSRQ} signal goes low, the bus will not be released while the WAIT signal is low. The bus will only be released when \overline{BUSRQ} goes low while WAIT is high.

Note 2: This line shows only that the output buffer is in the off state. It does not indicate that the signal level is fixed.

Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary as fixing of the level is delayed. The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.