NEC

MOS INTEGRATED CIRCUITS

# μPD63335

## STEREO SOUND CODEC

### DESCRIPTION

The μPD63335 is a stereo sound codec LSI that enables full-duplex communications and features two channels each of on-chip 16-bit ADC and DAC circuits for mutual conversion between digital signals and audio analog signals (having a maximum signal bandwidth of 20 kHz).

The analog signal input block enables four pairs of stereo signals plus three monaural signals to be output from the output stage's internal mixing circuit, which can then be multiplexed and input to the ADC. One type of monaural signal can be selected from two external pins via a selector as a monaural signal connected to an internal microphone amplifier (MIC amp), with selectable gain of 0 dB or 20 dB.

The analog signal output block enables mixed output of analog signals output by the DAC, four pairs of stereo analog signals, and an output signal from the MIC amp, and the volume of each signal can be controlled independently before mixing. The digital audio signal I/O block supports an audio-type serial interface (two's complement). In addition, a clocked serial interface (CSI) can be used for direct connection to a general-purpose microcontroller for access to internal registers such as for volume control.

### FEATURES

- Two channels each of over sample ΔΣ type ADC and DAC
  - ADC SNR = 85 dB Typ.
  - DAC SNR = 90 dB Typ.
- ADC and DAC digital filter characteristics
  - Pass band ripple: ±0.1 dB (0 to 0.4 $f_S$) for ADC and DAC
  - Stop band attenuation: −74 dB (0.6 $f_S$) or above for ADC and DAC
- Sampling frequency ($f_S$): 0.4 to 48 kHz
  - Division rate from master clock can be set to 3072, 1536, 768, or 512
- Analog input block includes a multiplexer and analog output block includes a mixing circuit
- Low-noise monaural MIC amp is on chip
- On-chip reference voltage power supply (1.4 V (TYP.))
- Low supply voltage operation: $DV_{DD}$ = 3.3 V, $AV_{DD}$ = 3.3 V
- Support for power down mode in each internal block
- Operating ambient temperature: −40 to +85°C

### APPLICATIONS

- Speech recognition systems, including car navigation systems
- Electronic toys with speech/audio I/O functions

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD63335GA-9EU | 48-pin plastic TQFP (fine pitch) (7 × 7) |

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**Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.**

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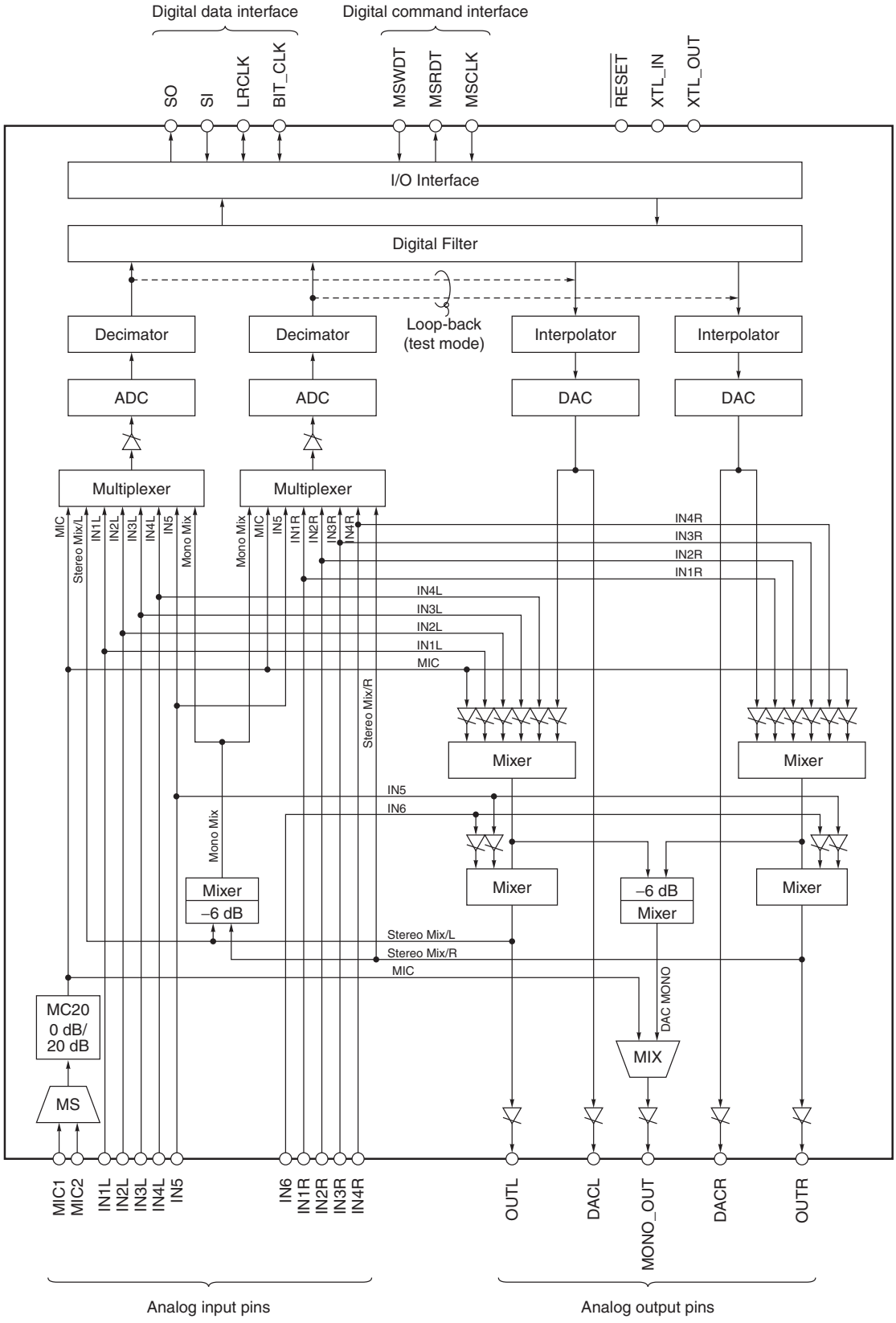
The mark ★ shows major revised points.

## BLOCK DIAGRAM

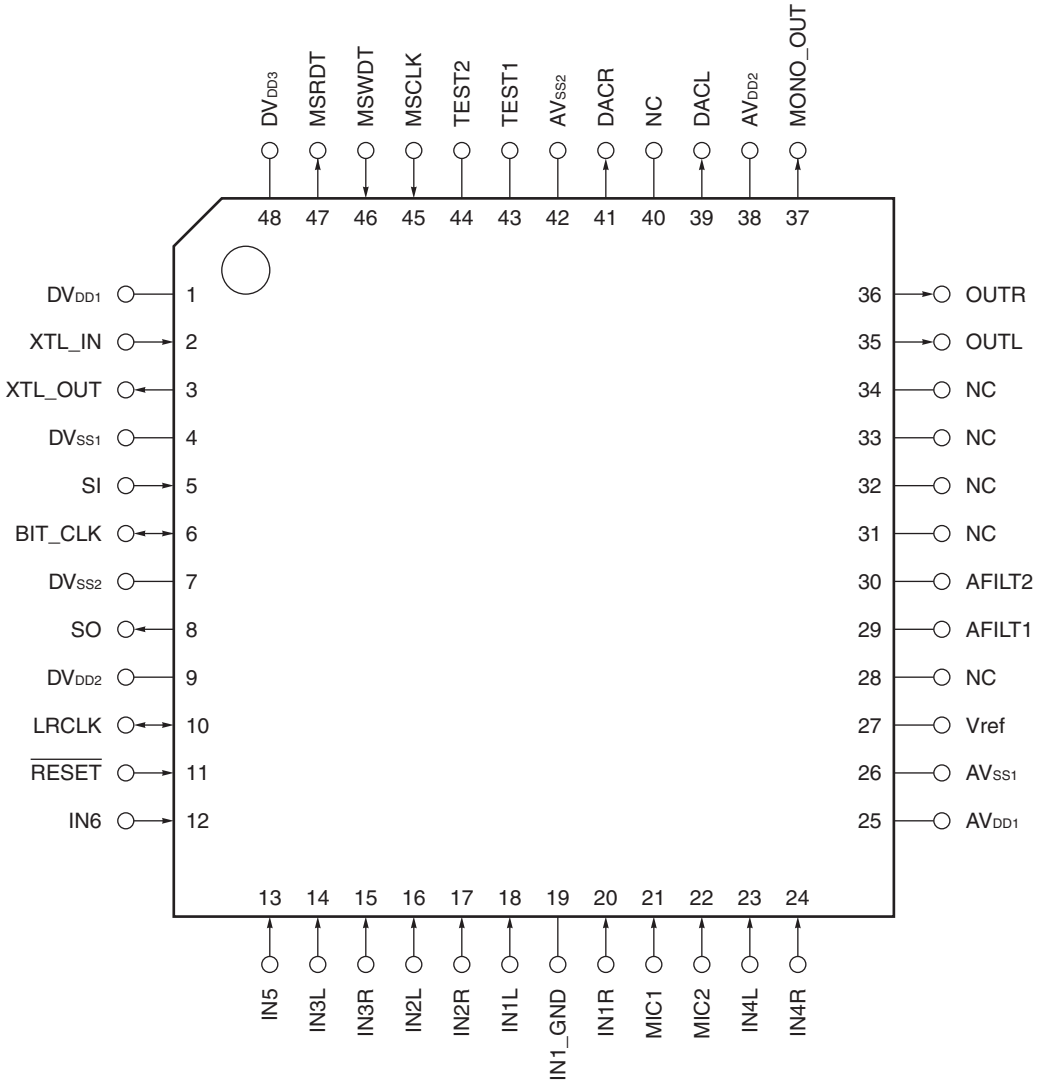



**Remark** The MS and MIX blocks are selectors.

## PIN CONFIGURATION (TOP VIEW)

48-pin plastic TQFP (fine pitch) (7 × 7)

- μPD63335GA-9EU



## PIN FUNCTIONS

(1/2)

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | $DV_{DD1}$ | – | Digital power supply |
| 2 | XTL_IN | I | Crystal resonator connection pin/external master clock input (see **1.3 Clock**) |
| 3 | XTL_OUT | O | Crystal resonator connection pin. Leave this pin open when using an external master clock. |
| 4 | $DV_{SS1}$ | – | Digital ground |
| 5 | SI | I | Data input for serial data interface[Note] |
| 6 | BIT_CLK | I/O | Bit sync clock for serial data interface[Note] |
| 7 | $DV_{SS2}$ | – | Digital ground |
| 8 | SO | O | Data output for serial data interface |
| 9 | $DV_{DD2}$ | – | Digital power supply |
| 10 | LRCLK | I/O | Frame sync clock for serial data interface[Note] |
| 11 | $\overline{\text{RESET}}$ | I | Reset signal input. Sets reset mode when low. |
| 12 | IN6 | I | Analog audio monaural input 6 |
| 13 | IN5 | I | Analog audio monaural input 5 |
| 14 | IN3L | I | Analog audio input 3, L channel |
| 15 | IN3R | I | Analog audio input 3, R channel |
| 16 | IN2L | I | Analog audio input 2, L channel |
| 17 | IN2R | I | Analog audio input 2, R channel |
| 18 | IN1L | I | Analog audio input 1, L channel |
| 19 | IN1_GND | – | AC ground pin for IN1. Generally connect to $AV_{SS}$ via a 1 μF capacitor. |
| 20 | IN1R | I | Analog audio input 1, R channel |
| 21 | MIC1 | I | MIC input 1 |
| 22 | MIC2 | I | MIC input 2 |
| 23 | IN4L | I | Analog audio input 4, L channel |
| 24 | IN4R | I | Analog audio input 4, R channel |
| 25 | $AV_{DD1}$ | – | Analog power supply |
| 26 | $AV_{SS1}$ | – | Analog ground |
| 27 | Vref | – | Reference voltage output for connecting bypass capacitor |
| 28 | NC | – | Not used. Leave this pin open. |
| 29 | AFILT1 | – | ADC L channel anti alias filter pin |
| 30 | AFILT2 | – | ADC R channel anti alias filter pin |
| 31 | NC | – | Not used. Leave this pin open. |
| 32 | NC | – | Not used. Leave this pin open. |
| 33 | NC | – | Not used. Leave this pin open. |
| 34 | NC | – | Not used. Leave this pin open. |

**Note** The SI, BIT_CLK, and LRCLK pins are neither pulled up nor pulled down within the LSI. Since malfunction may occur if these pins are somehow set to high impedance, pull-up or pull-down should be performed externally, via a resistor.

(2/2)

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 35 | OUTL | O | Analog audio output pin, L channel |
| 36 | OUTR | O | Analog audio output pin, R channel |
| 37 | MONO_OUT | O | Analog audio monaural output |
| 38 | $AV_{DD2}$ | – | Analog power supply |
| 39 | DACL | O | Analog DAC signal output, L channel |
| 40 | NC | – | Not used. Leave this pin open. |
| 41 | DACR | O | Analog DAC signal output, R channel |
| 42 | $AV_{SS2}$ | – | Analog ground |
| 43 | TEST1 | – | Test pin for IC sorting. Leave this pin open. |
| 44 | TEST2 | – | Test pin for IC sorting. Leave this pin open. |
| 45 | MSCLK | I | Sync clock input for serial command interface |
| 46 | MSWDT | I | Input for serial command interface |
| 47 | MSRDT | O | Output for serial command interface |
| 48 | $DV_{DD3}$ | – | Digital power supply |

## CONTENTS

# 1. DESCRIPTION OF FUNCTIONS

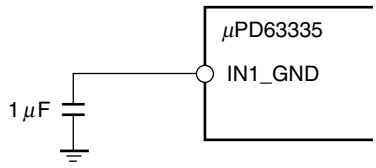
## 1.1 Analog Input Block

The μPD63335 features an on-chip two-channel ADC, which can convert analog signals selected by the multiplexer at the previous stage and input via the analog input pin to digital signals. An amplifier is configured between the ADC and multiplexer, and the input gain can be set in a range from 0 dB to 22.5 dB.

The multiplexer receives signals that are input from the analog output block's mixer circuit, and four-channel stereo signals, two monaural signals, and a monaural MIC input signal (selected from two input pins) from the analog input pins.

The IN1 input has a dedicated AC ground pin for canceling common-mode noise. Use of the IN1_GND pin enables connections to output pins that have a ground line, such as a CD audio output pin, via a 4.7 μF capacitor. If not using IN1_GND, connect to a ground via a 1 μF capacitor (see **Figure 1-1**).

**Figure 1-1. Connection Example When Not Using IN1_GND**




## 1.2 Analog Output Block

The analog output block includes two stereo output amplifiers, a monaural output amplifier, and a mixer circuit. The mixer circuit can be used to mix not only stereo analog signals from the DAC but also four pairs of stereo signals (IN1 to IN4), one monaural signal, and one MIC input signal (selected from two input pins). The analog signals from the DAC output can be connected to the mixer circuit or DAC L/R output via volume circuits. Monaural mixed signals to the monaural output selector (MIX) are the sum of the L channel/R channel mixer circuit output to which –6 dB of gain adjustment is applied within the LSI.

## 1.3 Clock

The μPD63335 features an on-chip clock generator. The μPD63335's master clock can be generated if a crystal resonator is connected via the XTL_IN or XTL_OUT pin.

The on-chip clock generator can be used only at the 24.576 MHz setting.

In addition, an external master clock can be input to the on-chip clock generator. In such cases, input the clock signal directly to the XTL_IN pin and leave the XTL_OUT pin open. In this case, the recommended frequency range of the external master clock is from 1.024 MHz to 24.576 MHz.

### 1.3.1 Switching external master clock frequency

To switch the external master clock frequency during ADC and DAC operation, use the following procedure.

**(1) When using the Master mode (LRCLK, BIT_CLK generated internally)**

<1> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h) to MUTE[Note 1].
<2> Switch the external master clock frequency.
<3> Set the LRCLK/BIT_CLK operation mode (if there is a change) (use the reset/clock status register (00h)).
<4> Set the audio format (if there is a change) (use the interface/timing register (01h)).
<5> Set the DAC volume register (10h, 11h) and DAC master volume register (14h, 15h)[Note 2]

**Notes 1.** The instant that the external master clock frequency is switched, noise may occur. For this reason, before switching the external master clock, set the volume for the DAC output to MUTE.

**2.** To prevent popping noises, after switching the external master clock frequency and following the lapse of an interval of time sufficient for three or more LRCLK cycles to be supplied, cancel the MUTE setting of the volume for the DAC output.
Also handle the ADC output data (SO) as valid data once the same interval of time has elapsed.

**(2) When using the slave mode (LRCLK, BIT_CLK supplied from external)**

<1> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h) to MUTE[Note 1].
<2> Power down the ADC and DAC (use the power down control register (18h)).
<3> Switch the external master clock, LRCLK, BIT_CLK frequency.
<4> Set the LRCLK/BIT_CLK operation mode (if there is a change) (use the reset/clock status register (00h)).
<5> Set the audio format (if there is a change) (use the interface/timing register (01h)).
<6> Cancel ADC, DAC power down (use the power down control register (18h)).
<7> Set the DAC volume register (10h, 11h) and DAC master volume register (14h, 15h)[Note 2].

**Notes 1.** Immediately after the ADC and DAC are powered down, noise may occur in the ADC and DAC outputs. For this reason, before powering down the ADC and DAC, set the volume for the DAC output to MUTE.

**2.** To prevent popping noises, after canceling power down and following the lapse of an interval of time sufficient for three or more LRCLK cycles to be supplied, cancel the MUTE setting of the volume for the DAC output. Also handle the ADC output data (SO) as valid data once the same interval of time has elapsed.

### 1.4 Reset

The μPD63335 features three reset modes.

(1) Cold reset

Cold reset is controlled by input signals via the $\overline{\text{RESET}}$ pin, and is used to initialize the μPD63335. Registers are reset to their initial values.

(2) Warm reset

A warm reset is used to reset the digital command interface for any reason. When FFh is written to the warm reset register (7Fh), the μPD63335 performs a warm reset. Register values are retained during a warm reset.

(3) Register reset

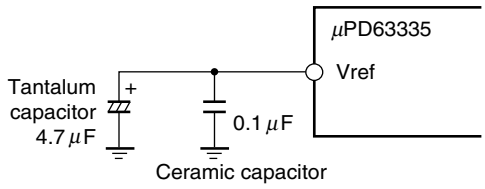
This initializes the μPD63335's internal registers. All registers are reset, except for the following registers.

- Reset/clock status register (00h)
- Interface/timing register (01h)
- Power down control register (18h)

### 1.5 Pin to Connect Noise-Reducing Capacitor

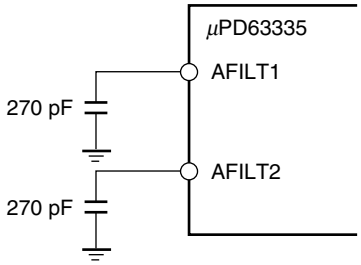
Pin 27 is a reference voltage pin that is used to connect to a bypass capacitor for stabilizing the internal reference voltage. Connect the bypass capacitor as shown in the figure below.

**Figure 1-2. Example of Bypass Capacitor Connection**




Pins 29 and 30 are used to connect capacitors for the ADC's anti alias filter. Connect the capacitor as shown in the figure below.

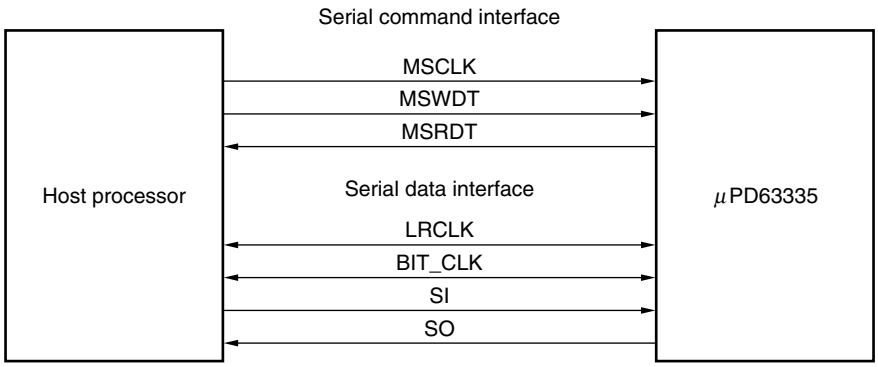
**Figure 1-3. Example of Capacitor Connection for Anti Alias Filter**



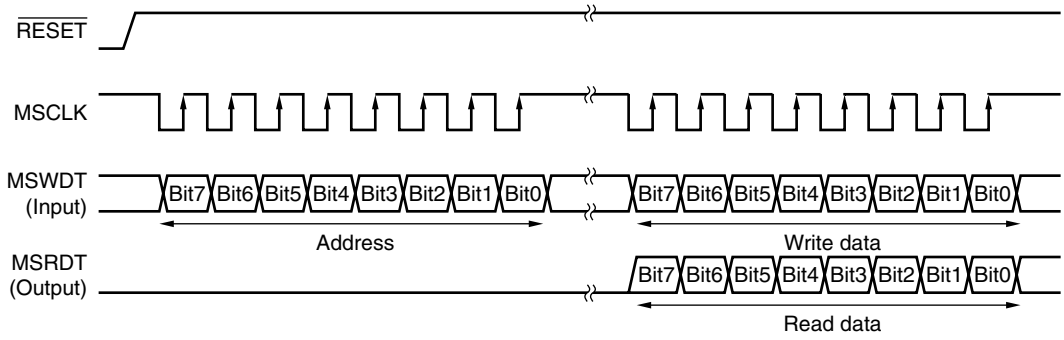
### 1.6 Digital Interfaces

The μPD63335 uses two different interfaces to connect to an external host processor (such as a CPU or sound controller). One is the serial command interface that controls the μPD63335, and the other is the serial data interface that is used for data input and output.

**Figure 1-4. Digital Interfaces**




#### 1.6.1 Serial command interface




When accessing the μPD63335 from an external host processor, use the clocked serial interface (MSCLK, MSWDT, MSRDT).

Transfer of addresses begins in sync with the rising edge of MSCLK, immediately after the $\overline{\text{RESET}}$ signal goes from low level to high level. Addresses consist of eight bits, of which bit 7 indicates the read/write attribute for access.

When a “1” is transferred to bit 7 in the address, a read operation is performed. After an address is input via the MSWDT pin, the contents of the corresponding register are output via the MSRDT pin.

When a “0” is transferred to bit 7 in the address, a write operation is performed. Once the address is sent from the host processor, 8-bit data is written.

The μPD63335 uses the data to check for bit drift in the serial command interface so as to ensure accurate control from the host processor.

When communication is being performed correctly, the D6 address bit of all the registers except the warm reset register (7Fh) is always “0”, and the D7 and D6 data bits are always “01”. The D6 data bit (SICK) is used to check for the occurrence of bit displacement among the serial command interface bits. For details of the SICK bit, refer to **2.1.1 Serial command interface check bit (SICK)**.

### 1.6.2 Serial data interface

Four sampling frequency settings can be made for the μPD63335 by setting the RATE[1:0] bit in an internal register (00h). Registers 00h and 01h can be used to set the polarity of the frame signal (LRCLK) and to switch the I/O status of the LRCLK and BIT_CLK signals. Some noise may occur when switching the format of the serial data interface during operation. Before switching, set the analog output volume to "mute" (see **2.1.14** to **2.1.16**).

**Selection of sampling rate (set via RATE[1:0] bit in register 00h)**

| RATE [1:0] | Sampling Rate | In Case of $f_{MCLK}$ = 24.576 MHz |
|---|---|---|
| 00 | $f_{MCLK}$/3072 (initial value) | 8 kHz |
| 01 | $f_{MCLK}$/1536 | 16 kHz |
| 10 | $f_{MCLK}$/768 | 32 kHz |
| 11 | $f_{MCLK}$/512 | 48 kHz |

**Selection of audio data format (set via FSDF[2:0] bit in register 01h)**

| FSDS [2:0] | Bit Clocks per Frame | Audio Data Format (2's Complement, MSB First) | |
|---|---|---|---|
| | | PCM Input Data: SI | PCM Output: SO |
| 000 | 64 | Left justified | Left justified |
| 001 | 64 | Left justified | Right justified |
| 010 | 64 | Right justified | Left justified |
| 011 | 64 | Right justified | Right justified |
| 100 | 48 | Left justified | Left justified |
| 101 | 48 | Left justified | Right justified |
| 110 | 48 | Right justified | Left justified |
| 111 | 32 (initial value) | – | – |

**Selection of LRCLK polarity (set via LRCLKS bit in register 00h)**

| LRCLKS | LRCLK Level | |
|---|---|---|
| | High Level | Low Level |
| 0 | L channel (initial value) | R channel (initial value) |
| 1 | R channel | L channel |

**Selection of LRCLK/BIT_CLK direction (set via CLKIOS bit in register 00h)**

| CLKIOS | LRCLK/BIT_CLK Direction |
|---|---|
| 0 | Input (initial value) |
| 1 | Output |

The μPD63335 can operate in both master mode (the mode in which the μPD63335 outputs LRCLK and BIT_CLK) and slave mode (the mode in which the μPD63335 is supplied with LRCLK and BIT_CLK externally). Set the registers related to each mode using the recommended procedure below.

**(1) When using the master mode (LRCLK, BIT_CLK generated internally)**

**(a) To start ADC, DAC operation from the ADC, DAC power down status (including at power ON)**

<1> Set the DAC volume register (10h, 11h) and DAC master volume register (14h, 15h) to MUTE[Note 1].

<2> Set the LRCLK/BIT_CLK operation mode (use the reset/clock status register (00h))[Note 2].

<3> Set the audio format (use the interface/timing register (01h)).

<4> Cancel ADC, DAC power down (use the power down control register (18h)).

<5> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h)[Note 3].

**(b) To change the LRCLK/BIT_CLK operation mode setting during ADC, DAC operation**

<1> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h) to MUTE[Note 4].

<2> Change the LRCLK/BIT_CLK operation mode setting (use the reset/clock status register (00h)).

<3> Set the audio format (if there is a change) (use the interface/timing register (01h)).

<4> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h)[Note 5].

**Notes 1.** Immediately after canceling ADC, DAC power down, noise may occur in the ADC and DAC outputs. For this reason, before canceling power down, set the volume for DAC output to MUTE. (If these volumes are already set to MUTE, at power ON, etc., setting them to MUTE again is not required.)

**2.** The LRCLK/BIT_CLK operation mode is set to the slave mode by default. To use it in the master mode, switch the LRCLK/BIT_CLK operation mode to the master mode while the ADC and DAC are powered down.

**3.** To prevent popping noises, after canceling power down and following the lapse of an interval of time sufficient for three or more LRCLK cycles to be supplied, cancel the MUTE setting of the volume for the DAC output. Also handle the ADC output data (SO) as valid data once the same interval of time has elapsed.

**4.** Immediately after changing the LRCLK/BIT_CLK operation mode, noise may occur in the ADC and DAC outputs. For this reason, before changing this setting, set the volume for DAC output to MUTE.

**5.** To prevent popping noises, after changing the LRCLK/BIT_CLK operation mode, following the lapse of an interval of time sufficient for three or more LRCLK cycles to be supplied, cancel the MUTE setting of the volume for the DAC output. Also handle the ADC output data (SO) as valid data once the same interval of time has elapsed.

**(2) When using the slave mode (LRCLK, BIT_CLK supplied from external)**

**(a) To start ADC, DAC operation from the ADC, DAC power down status (including at power ON)**

<1> Set the DAC volume register (10h, 11h) and DAC master volume register (14h, 15h) to MUTE[Note 1].

<2> Start supplying the external clock (LRCLK, BIT_CLK)[Note 2].

<3> Set the LRCLK/BIT_CLK operation mode (use the reset/clock status register (00h)).

<4> Set the audio format (use the interface/timing register (01h)).

<5> Cancel ADC, DAC power down (use the power down control register (18h)).

<6> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h)[Note 3].

**(b) To change the LRCLK/BIT_CLK operation mode setting during ADC, DAC operation**

<1> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h) to MUTE[Note 4].

<2> Switch the external clock (LRCLK, BIT_CLK)[Note 5].

<3> Change the LRCLK/BIT_CLK operation mode setting (use the reset/clock status register (00h)).

<4> Set the audio format (if there is a change) (use the interface/timing register (01h)).

<5> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h)[Note 6].

**Notes 1.** Immediately after canceling ADC, DAC power down, noise may occur in the ADC and DAC outputs. For this reason, before canceling power down, set the volume for DAC output to MUTE. (If these volumes are already set to MUTE, at power ON, etc., setting them to MUTE again is not required.)

**2.** Start supplying the external clock (LRCLK, BIT_CLK) prior to setting the LRCLK/BIT_CLK operation mode.

**3.** To prevent popping noises, after canceling power down and following the lapse of an interval of time sufficient for three or more LRCLK cycles to be supplied, cancel the MUTE setting of the volume for the DAC output. Also handle the ADC output data (SO) as valid data once the same interval of time has elapsed.

**4.** Immediately after changing the LRCLK/BIT_CLK operation mode, noise may occur in the ADC and DAC outputs. For this reason, before changing this setting, set the volume for DAC output to MUTE.

**5.** Start supplying the external clock (LRCLK, BIT_CLK) immediately it has been changed prior to changing the LRCLK/BIT_CLK operation mode setting.

**6.** To prevent popping noises, after changing the LRCLK/BIT_CLK operation mode, following the lapse of an interval of time sufficient for three or more LRCLK cycles to be supplied, cancel the MUTE setting of the volume for the DAC output. Also handle the ADC output data (SO) as valid data once the same interval of time has elapsed.

**(c) To pause supply of the external clock (LRCLK, BIT_CLK) while the power is ON**

Power down the ADC and DAC in the sequence described below. To restart the external clock supply, perform steps <2> to <6> of section (a) To start ADC, DAC operation from the ADC, DAC power down status (including at power ON).

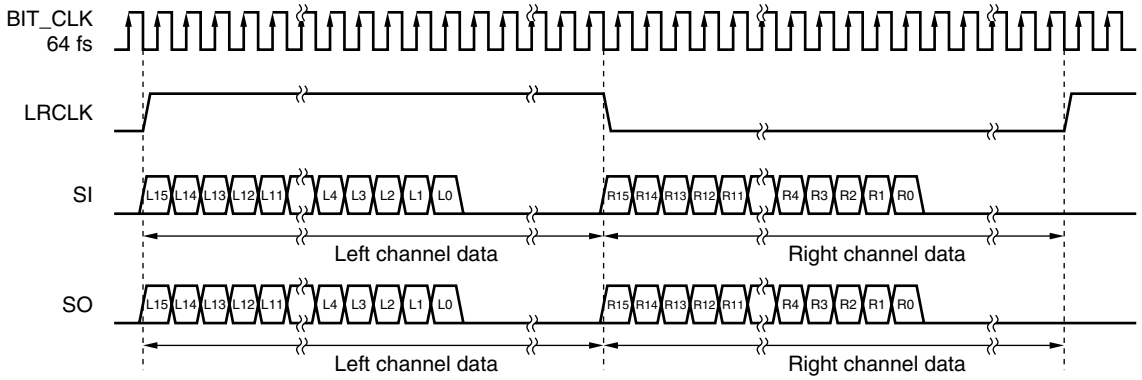
<1> Set the DAC volume register (10h, 11h) and the DAC master volume register (14h, 15h) to MUTE[Note 1].
<2> Power down the ADC and DAC (use power down control register (18h)).
<3> Stop the external clock (LRCLK, BIT_CLK) (fix it to high level or low level)[Note 2].

**Notes 1.** Immediately after executing ADC, DAC power down, noise may occur in the ADC and DAC outputs. For this reason, before executing power down, set the volume for the DAC output to MUTE.

**2.** To reliably power down ADC and DAC, following input of the ADC, DAC power down command, stop supplying the external clock (LRCLK, BIT_CLK) after supplying LRCLK for three cycles or more.

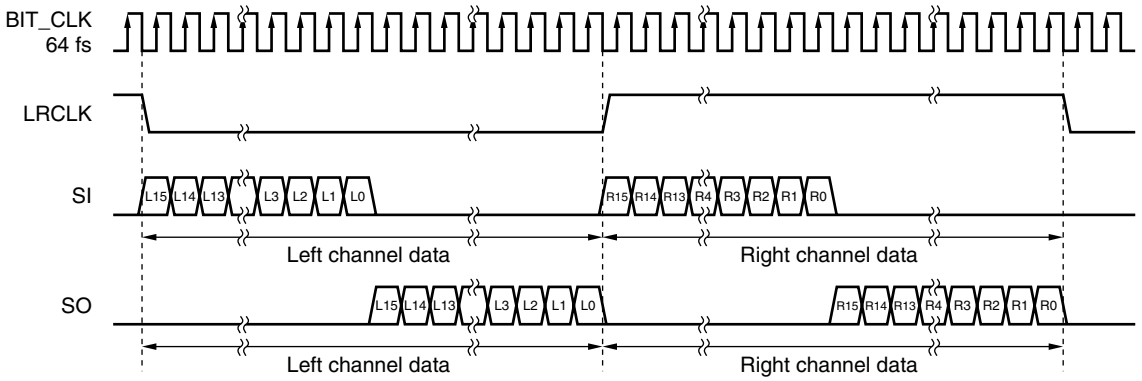
### 1.6.3 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 0:0:0:0

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 64 fs
- Data I/O occurs via the L channel while LRCLK is at high level and occurs via the R channel while LRCLK is at low level.
- SI and SO have left-justified data input and output.



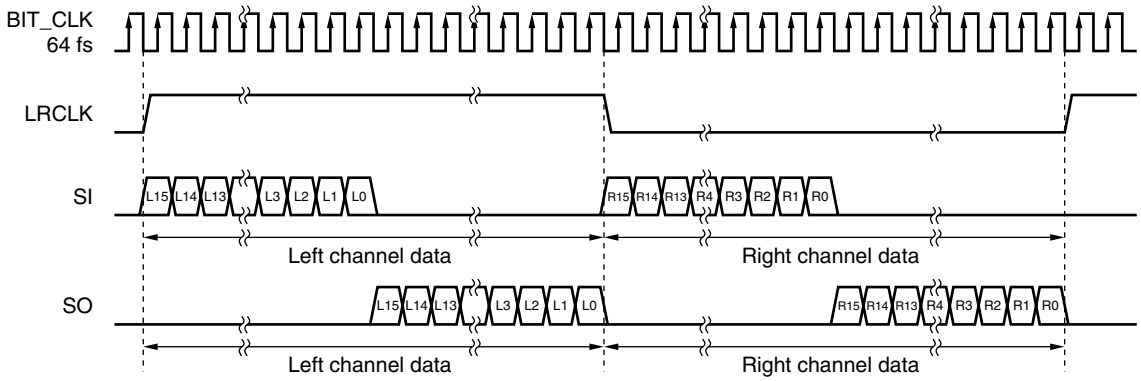

### 1.6.4 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 0:0:0:1

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 64 fs
- Data I/O occurs via the R channel while LRCLK is at high level and occurs via the L channel while LRCLK is at low level.
- SI and SO have left-justified data input and output.



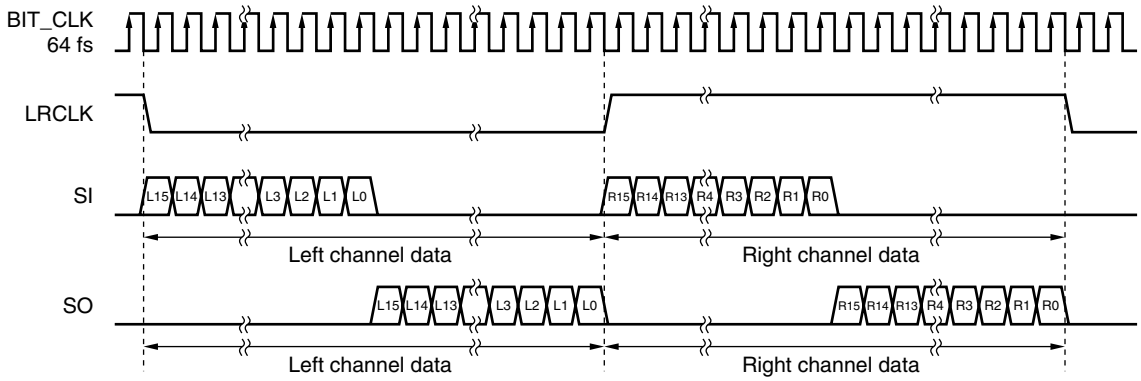
### 1.6.5 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 0:0:1:0

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 64 fs
- Data I/O occurs via the L channel while LRCLK is at high level and occurs via the R channel while LRCLK is at low level.
- SI has left-justified data input and SO has right-justified data output.



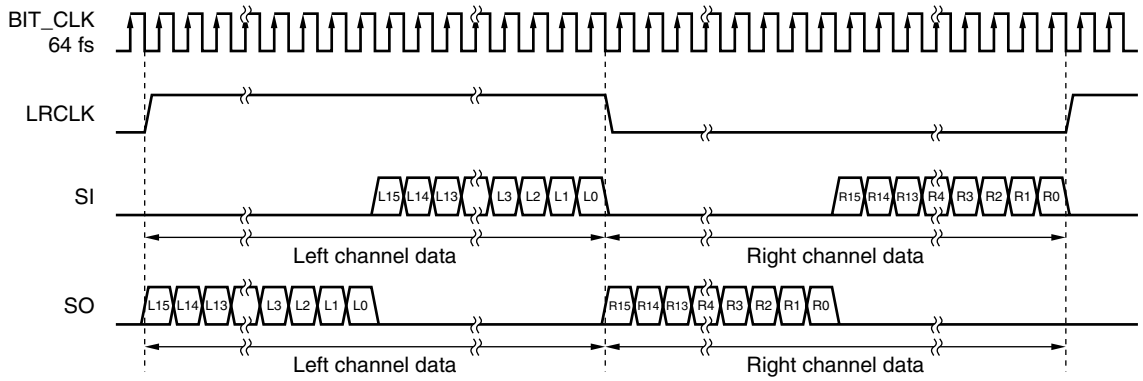

### 1.6.6 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 0:0:1:1

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 64 fs
- Data I/O occurs via the R channel while LRCLK is at high level and occurs via the L channel while LRCLK is at low level.
- SI has left-justified data input and SO has right-justified data output.



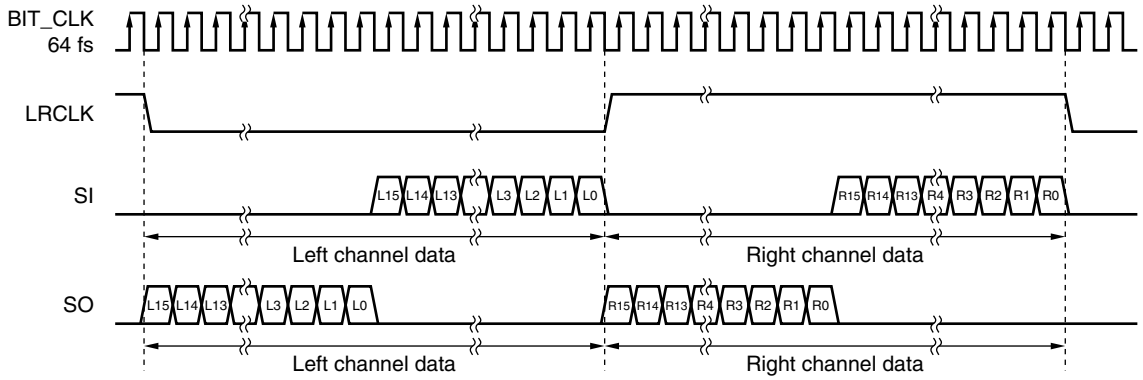
### 1.6.7 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 0:1:0:0

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 64 fs
- Data I/O occurs via the L channel while LRCLK is at high level and occurs via the R channel while LRCLK is at low level.
- SI has right-justified data input and SO has left-justified data output.



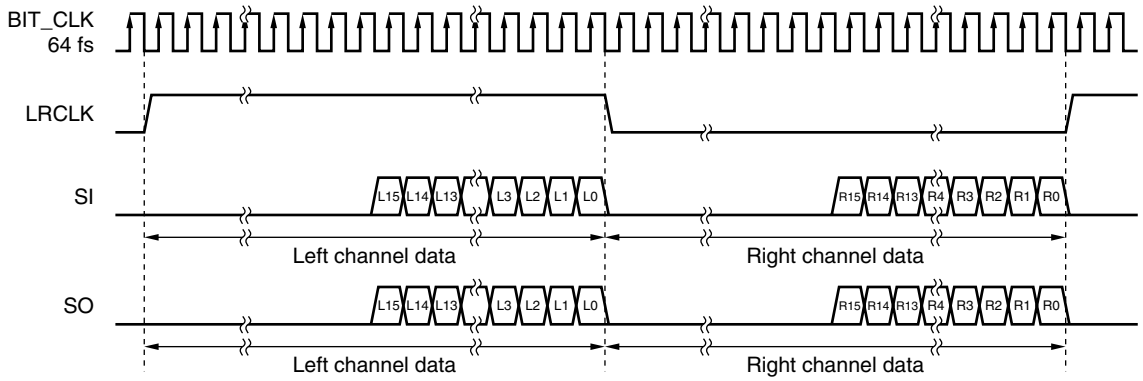

### 1.6.8 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 0:1:0:1

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 64 fs
- Data I/O occurs via the R channel while LRCLK is at high level and occurs via the L channel while LRCLK is at low level.
- SI has right-justified data input and SO has left-justified data output.



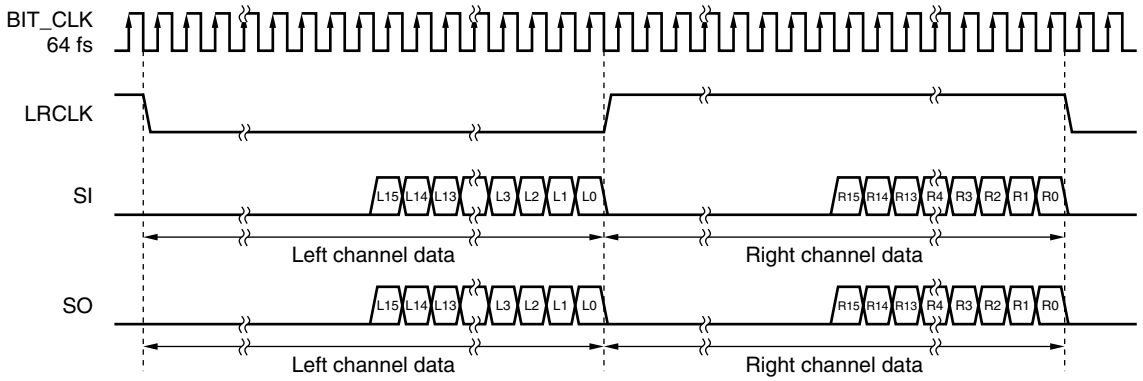
### 1.6.9 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 0:1:1:0

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 64 fs
- Data I/O occurs via the L channel while LRCLK is at high level and occurs via the R channel while LRCLK is at low level.
- SI and SO have right-justified data input and output.




### 1.6.10 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 0:1:1:1

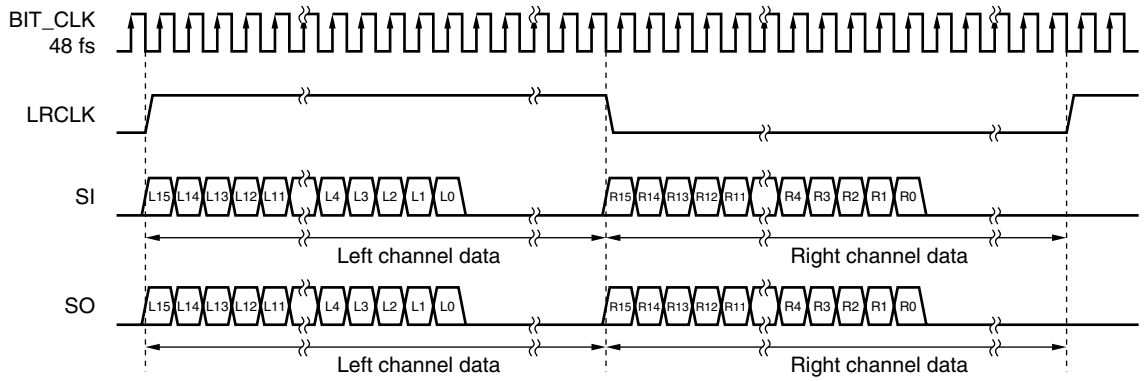
- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 64 fs
- Data I/O occurs via the R channel while LRCLK is at high level and occurs via the L channel while LRCLK is at low level.
- SI and SO have right-justified data input and output.



### 1.6.11 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 1:0:0:0

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK[Note] and LRCLK
- BIT_CLK: 48 fs
- Data I/O occurs via the L channel while LRCLK is at high level and occurs via the R channel while LRCLK is at low level.
- SI and SO have left-justified data input and output.

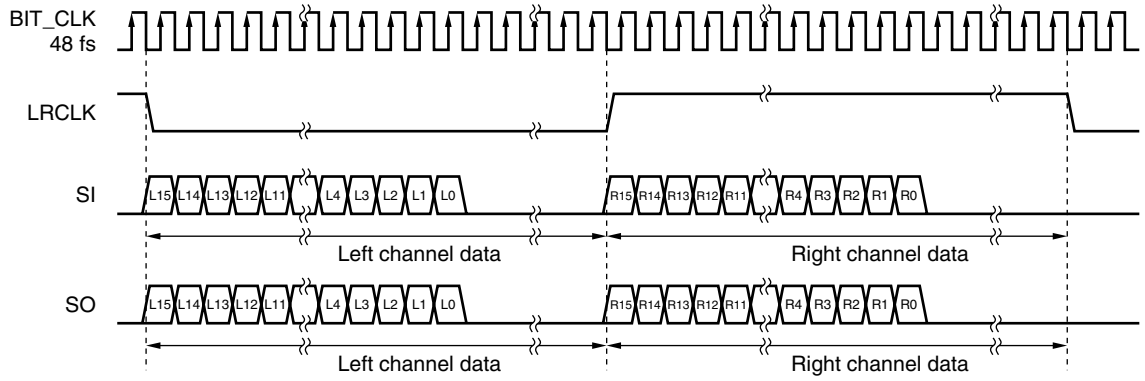
**Note** The duty factor of output BIT_CLK is not 50%.




### 1.6.12 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 1:0:0:1

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK[Note] and LRCLK
- BIT_CLK: 48 fs
- Data I/O occurs via the R channel while LRCLK is at high level and occurs via the L channel while LRCLK is at low level.
- SI and SO have left-justified data input and output.

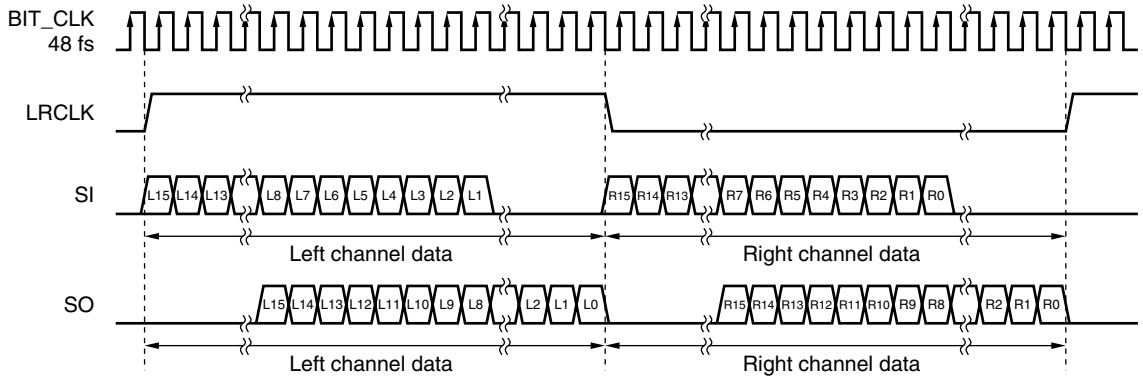
**Note** The duty factor of output BIT_CLK is not 50%.



### 1.6.13 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 1:0:1:0

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK[Note] and LRCLK
- BIT_CLK: 48 fs
- Data I/O occurs via the L channel while LRCLK is at high level and occurs via the R channel while LRCLK is at low level.
- SI has left-justified data input and SO has right-justified data output.

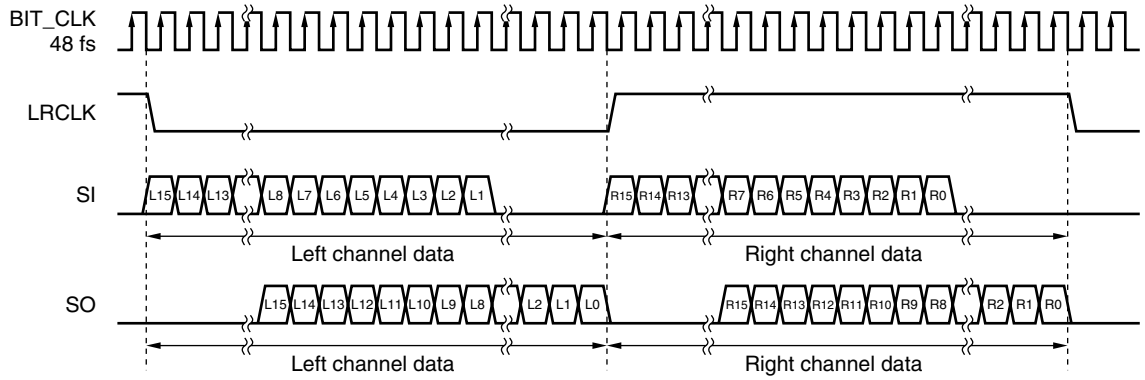
**Note** The duty factor of output BIT_CLK is not 50%.




### 1.6.14 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 1:0:1:1

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK[Note] and LRCLK
- BIT_CLK: 48 fs
- Data I/O occurs via the R channel while LRCLK is at high level and occurs via the L channel while LRCLK is at low level.
- SI has left-justified data input and SO has right-justified data output.

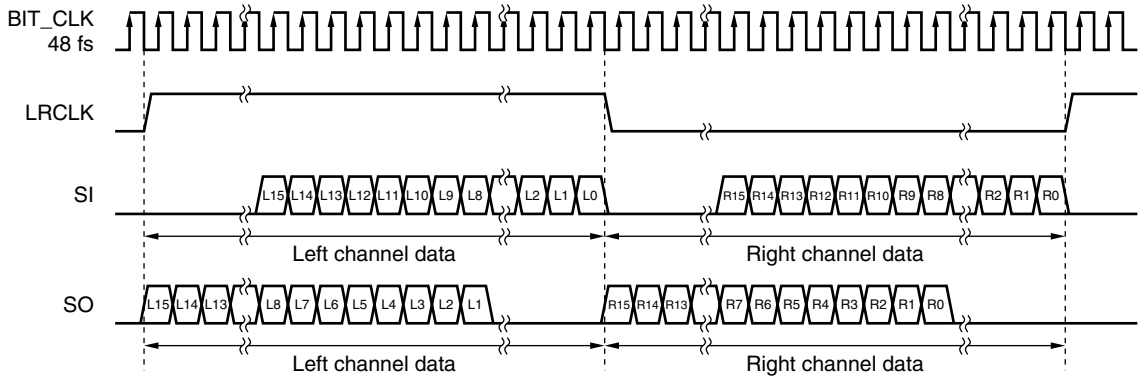
**Note** The duty factor of output BIT_CLK is not 50%.



### 1.6.15 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 1:1:0:0

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK[Note] and LRCLK
- BIT_CLK: 48 fs
- Data I/O occurs via the L channel while LRCLK is at high level and occurs via the R channel while LRCLK is at low level.
- SI has right-justified data input and SO has left-justified data output.

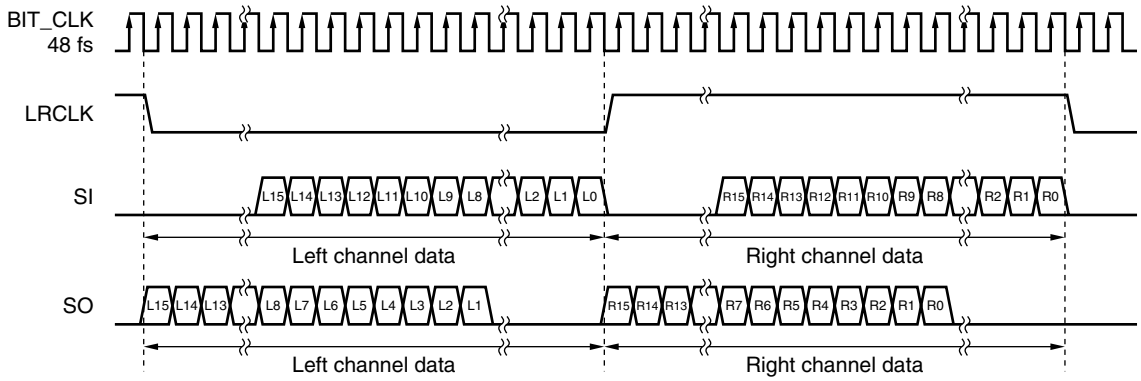
**Note** The duty factor of output BIT_CLK is not 50%.




### 1.6.16 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 1:1:0:1

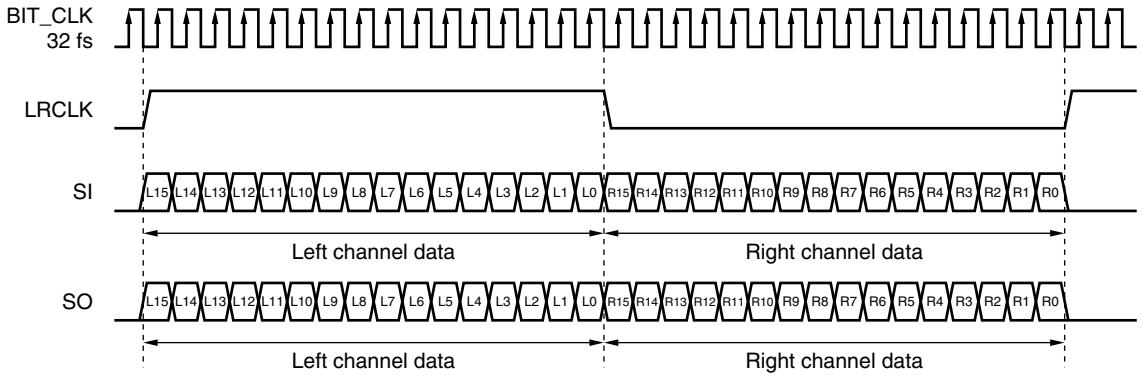
- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK[Note] and LRCLK
- BIT_CLK: 48 fs
- Data I/O occurs via the R channel while LRCLK is at high level and occurs via the L channel while LRCLK is at low level.
- SI has right-justified data input and SO has left-justified data output.

**Note** The duty factor of output BIT_CLK is not 50%.



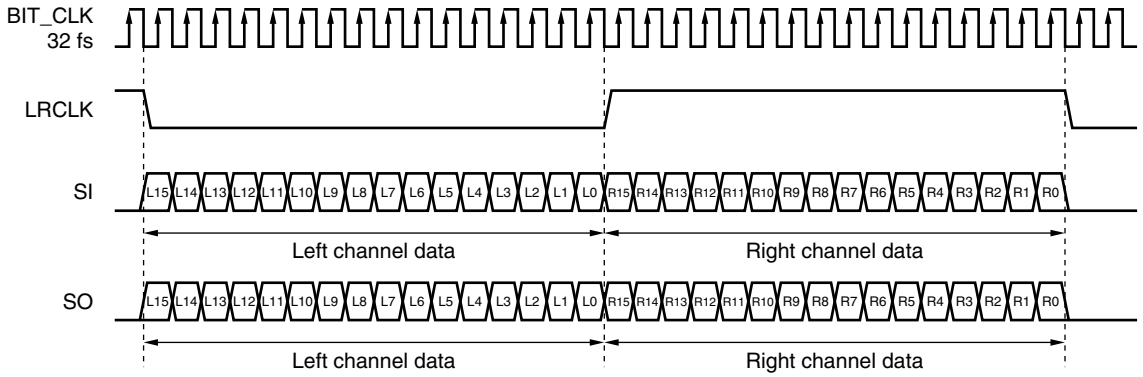
### 1.6.17 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 1:1:1:0 (initial value)

- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 32 fs
- Data I/O occurs via the L channel while LRCLK is at high level and occurs via the R channel while LRCLK is at low level.




### 1.6.18 Data format of FSDF2:FSDF1:FSDF0:LRCLKS = 1:1:1:1

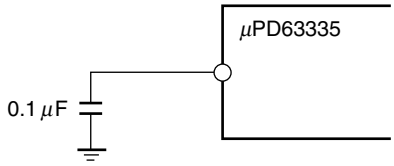
- CLKIOS = “0”: Input of both BIT_CLK and LRCLK
- CLKIOS = “1”: Output of both BIT_CLK and LRCLK
- BIT_CLK: 32 fs
- Data I/O occurs via the R channel while LRCLK is at high level and occurs via the L channel while LRCLK is at low level.




## 1.7 Usage Precautions

Analog input pins may influence the internal circuit characteristics if register mute is cancelled while they are open. Therefore, ground all unused analog input pins via a capacitor (refer to **Figure 1-5**) and set related registers to MUTE.

**Figure 1-5. Example of Handling of Unused Analog Input Pin**



## 2. REGISTERS

A register map of the μPD63335 is shown below.

**Table 2-1. μPD63335 Register Map**

| Address [A7:A0] | | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | Write | | | | | | | | | | |
| 80h | 00h | Reset and Clock Status Select | 0 | SICK | 0 | RRST | RATE1 | RATE0 | LRCLKS | CLKIOS | 40h |
| 81h | 01h | Interface Timing | 0 | SICK | 0 | 0 | 0 | FSDF2 | FSDF1 | FSDF0 | 47h |
| 82h | 02h | ADS Select | 0 | SICK | ADSL2 | ADSL1 | ADSL0 | ADSR2 | ADSR1 | ADSR0 | 40h |
| 83h | 03h | ADCL Gain | 0 | SICK | 0 | ADLM | ADLV3 | ADLV2 | ADLV1 | ADRV0 | 50h |
| 84h | 04h | ADCR Gain | 0 | SICK | 0 | ADRM | ADRV3 | ADRV2 | ADRV1 | ADRV0 | 50h |
| 85h | 05h | IN1L Volume | 0 | SICK | IN1LM | IN1LV4 | IN1LV3 | IN1LV2 | IN1LV1 | IN1LV0 | 68h |
| 86h | 06h | IN1R Volume | 0 | SICK | IN1RM | IN1RV4 | IN1RV3 | IN1RV2 | IN1RV1 | IN1RV0 | 68h |
| 87h | 07h | IN2L Volume | 0 | SICK | IN2LM | IN2LV4 | IN2LV3 | IN2LV2 | IN2LV1 | IN2LV0 | 68h |
| 88h | 08h | IN2R Volume | 0 | SICK | IN2RM | IN2RV4 | IN2RV3 | IN2RV2 | IN2RV1 | IN2RV0 | 68h |
| 89h | 09h | IN3L Volume | 0 | SICK | IN3LM | IN3LV4 | IN3LV3 | IN3LV2 | IN3LV1 | IN3LV0 | 68h |
| 8Ah | 0Ah | IN3R Volume | 0 | SICK | IN3RM | IN3RV4 | IN3RV3 | IN3RV2 | IN3RV1 | IN3RV0 | 68h |
| 8Bh | 0Bh | IN4L Volume | 0 | SICK | IN4LM | IN4LV4 | IN4LV3 | IN4LV2 | IN4LV1 | IN4LV0 | 68h |
| 8Ch | 0Ch | IN4R Volume | 0 | SICK | IN4RM | IN4RV4 | IN4RV3 | IN4RV2 | IN4RV1 | IN4RV0 | 68h |
| 8Dh | 0Dh | IN5 Volume | 0 | SICK | IN5M | IN5V4 | IN5V3 | IN5V2 | IN5V1 | IN5V0 | 68h |
| 8Eh | 0Eh | MIC Volume | 0 | SICK | MICM | MICV4 | MICV3 | MICV2 | MICV1 | MICV0 | 68h |
| 8Fh | 0Fh | IN6 Volume | 0 | SICK | IN6M | IN6V3 | IN6V2 | IN6V1 | IN6V0 | 0 | 60h |
| 90h | 10h | DACL Volume | 0 | SICK | DALM | DALV4 | DALV3 | DALV2 | DALV1 | DALV0 | 68h |
| 91h | 11h | DACR Volume | 0 | SICK | DARM | DARV4 | DARV3 | DARV2 | DARV1 | DARV0 | 68h |
| 92h | 12h | OUTL Master Volume | 0 | SICK | OMLM | OMLV4 | OMLV3 | OMLV2 | OMLV1 | OMLV0 | 60h |
| 93h | 13h | OUTR Master Volume | 0 | SICK | OMRM | OMRV4 | OMRV3 | OMRV2 | OMRV1 | OMRV0 | 60h |
| 94h | 14h | DALR Master Volume | 0 | SICK | DMLM | DMLV4 | DMLV3 | DMLV2 | DMLV1 | DMLV0 | 60h |
| 95h | 15h | DACR Master Volume | 0 | SICK | DMRM | DMRV4 | DMRV3 | DMRV2 | DMRV1 | DMRV0 | 60h |
| 96h | 16h | MONO Volume | 0 | SICK | MNMM | MNMV4 | MNMV3 | MNMV2 | MNMV1 | MNMV0 | 60h |
| 97h | 17h | Path Select | 0 | SICK | 0 | 1 | MIX | MS | MC20 | LPBK | 50h |
| 98h | 18h | Power down Control/Status | 0 | SICK | 0 | DIGPD | VREFPD | MIXPD | DACPD | ADCPD | 43h |
| – | 7Fh | Warm Reset | RW7 | RW6 | RW5 | RW4 | RW3 | RW2 | RW1 | RW0 | 00h |

**Cautions 1. Read/write access is prohibited for all registers that are not included in this table (i.e., for all non-existent registers).**

**2. Read access is prohibited for the warm reset register (7Fh).**

**3. A7, the MSB of the address, indicates the command read/write attribute.**

**4. The write data to write address 00h and 10h becomes valid after LRCLK is input (or output) for one clock cycle or more.**

## 2.1 Individual Registers

### 2.1.1 Serial command interface check bit (SICK)

The D7 and D6 bits of all registers except the warm reset register (7Fh) can be used to check the serial command interface transfer results. When write is performed to the μPD63335 register, "1" is always written to the SICK bit.

When the initial state and serial command interface operate normally, "1" is always written to the SICK bit and the D7 and D6 bits of all the registers except the warm reset register (7Fh) remain "01". If for some reason the D7 and D6 bits become other than "01" during write, "0" is written to SICK. In other words, when the D7 and D6 bits among the register values read from the host processor are "00", bit displacement occurs during serial command interface write or read, and register access may not be performed normally.

If the SICK bit of the read register is "0", perform a warm reset and execute a digital command interface reset.

Table 2-2 shows the relationship between the values written to the D7 and D6 bits and the SICK bit.

**Table 2-2. SICK Bit Setting Values**

| Write [D7:D6] | SICK Setting Value | Read [D7:D6] | Command I/F Status |
|---|---|---|---|
| 00 | 0 | 00 | Abnormal |
| 01 | 1 | 01 | Normal |
| 10 | 0 | 00 | Abnormal |
| 11 | 0 | 00 | Abnormal |

### 2.1.2 Reset/clock status register (00h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 80h | 00h | 0 | SICK | 0 | RRST | RATE1 | RATE0 | LRCLKS | CLKIOS | 40h |

This register is used to make register reset settings, serial data interface settings, and sampling rate settings. The bits and settings are described as follows. When 5xh is written to this register, a register reset is executed (refer to **1.4 Reset** for details of the register reset.). A register reset sets default values in all registers except the reset/clock status register (00h), interface/timing register (01h), and power down control register (18h). This register's default value is 40h (register reset: off, sampling rate setting: $f_{MCLK}$/3072, LRCLK setting: when LRCLK = high level, L channel PCM data I/O, BIT_CLK/LRCLK: input).

**Table 2-3. Bits and Settings in Reset/Clock Status Register (00h)**

| Bit | Name | Value | Description | Remark |
|---|---|---|---|---|
| D4 | RRST | 1 | Register reset | – |
| D3, D2 | RATE [1:0] | 00 | $f_S = f_{MCLK}/3072$ (8 kHz @ $f_{MCLK}$ = 24.576 MHz) | Default |
| | | 01 | $f_S = f_{MCLK}/1536$ (16 kHz @ $f_{MCLK}$ = 24.576 MHz) | – |
| | | 10 | $f_S = f_{MCLK}/768$ (32 kHz @ $f_{MCLK}$ = 24.576 MHz) | – |
| | | 11 | $f_S = f_{MCLK}/512$ (48 kHz @ $f_{MCLK}$ = 24.576 MHz) | – |
| D1 | LRCLKS | 0 | When LRCLK is at high level, L channel data | Default |
| | | 1 | When LRCLK is at high level, R channel data | – |
| D0 | CLKIOS | 0 | LRCLK and BIT_CLK are both input | Default |
| | | 1 | LRCLK and BIT_CLK are both output | – |

**Remark** $f_S$: Sampling rate
$f_{MCLK}$: Master clock (input frequency from XTL_IN pin)

### 2.1.3 Interface/timing register (01h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 81h | 01h | 0 | SICK | 0 | 0 | 0 | FSDF2 | FSDF1 | FSDF0 | 47h |

This register is used to set the data I/O method for the serial data interface. The default value is 47h.

**Table 2-4. Format of Interface/Timing Register (01h)**

| Bit | Name | Value | Audio Data Format (2's Complement, MSB First) | | |
|---|---|---|---|---|---|
| | | | Bit Clocks per Frame | PCM Input Data SI | PCM Output Data SO |
| D2 to D0 | FSDF [2:0] | 000 | 64 | Left justified | Left justified |
| | | 001 | 64 | Left justified | Right justified |
| | | 010 | 64 | Right justified | Left justified |
| | | 011 | 64 | Right justified | Right justified |
| | | 100 | 48 | Left justified | Left justified |
| | | 101 | 48 | Left justified | Right justified |
| | | 110 | 48 | Right justified | Left justified |
| | | 111 | 32 (default) | – | – |

### 2.1.4 Input select register (02h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 82h | 02h | 0 | SICK | ADSL2 | ADSL1 | ADSL0 | ADSR2 | ADSR1 | ADSR0 | 40h |

This register is used to make ADC input settings. The multiplexer that comes before the ADC can be set independently to L channel or R channel. The default value is 40h (MIC input).

**Table 2-5. Settings in Input Select Register (02h)**

| L Channel | | R Channel | |
|---|---|---|---|
| ADSL [2:0] | L Channel ADC Input Selection | ADSR [2:0] | R Channel ADC Input Selection |
| 000 | MIC (default value) | 000 | MIC (default value) |
| 001 | IN1L | 001 | IN1R |
| 010 | IN2L | 010 | IN2R |
| 011 | IN3L | 011 | IN3R |
| 100 | IN4L | 100 | IN4R |
| 101 | Stereo Mix/L | 101 | Stereo Mix/R |
| 110 | Mono Mix | 110 | Mono Mix |
| 111 | IN5 | 111 | IN5 |

**Remarks 1.** Stereo Mix: Output of output-side mixer is used as output of input-side multiplexer (ADC input).

**2.** Mono Mix: DAC MONO output is used as output of input-side multiplexer (ADC input).

### 2.1.5 ADC input gain registers (03h, 04h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 83h | 03h | 0 | SICK | 0 | ADLM | ADLV3 | ADLV2 | ADLV1 | ADLV0 | 50h |
| 84h | 04h | 0 | SICK | 0 | ADRM | ADRV3 | ADRV2 | ADRV1 | ADRV0 | 50h |

These registers are used to set the gain for the output signal from the multiplexer that is input to the ADC. The correspondence between bits and gain settings is shown below. Gain can be set in a range from 0.0 dB to +22.5 dB, in 1.5 dB steps. The default value is 50h (gain: 0 dB, mute: ON).

- ADLM: L channel ADC input mute control bit
- ADRM: R channel ADC input mute control bit
- ADLV[3:0]: L channel ADC input gain control bits
- ADRV[3:0]: R channel ADC input gain control bits

**Table 2-6. Correspondence of Bits and Gain Settings in ADC Input Gain Registers (03h, 04h)**

| ADLM/ADRM | ADLV[3:0]/ADRV[3:0] | Gain |
|---|---|---|
| 0 | 0000 | 0 dB |
| 0 | 0001 | +1.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1110 | +21.0 dB |
| 0 | 1111 | +22.5 dB |
| 1 | xxxx | Mute |
| 1 | 0000 | Default |

### 2.1.6 IN1 volume registers (05h, 06h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 85h | 05h | 0 | SICK | IN1LM | IN1LV4 | IN1LV3 | IN1LV2 | IN1LV1 | IN1LV0 | 68h |
| 86h | 06h | 0 | SICK | IN1RM | IN1RV4 | IN1RV3 | IN1RV2 | IN1RV1 | IN1RV0 | 68h |

These registers are used to set the IN1 input signal's mixer input volume. The correspondence between bits and gain settings is shown below. Gain can be set in a range from +12.0 dB to –34.5 dB, in 1.5 dB steps. The default value is 68h (gain: 0 dB, mute: ON).

- IN1LM: IN1 L channel mixer input mute control bit
- IN1RM: IN1 R channel mixer input mute control bit
- IN1LV[4:0]: IN1 L channel mixer input gain control bits
- IN1RV[4:0]: IN1 R channel mixer input gain control bits

**Table 2-7. Correspondence of Bits and Gain Settings in IN1 Volume Registers (05h, 06h)**

| IN1LM/IN1RM | IN1LV[4:0]/IN1RV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | +12.0 dB |
| 0 | 0 0001 | +10.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 0 1000 | 0 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | –33.0 dB |
| 0 | 1 1111 | –34.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 1000 | Default |

### 2.1.7 IN2 volume registers (07h, 08h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 87h | 07h | 0 | SICK | IN2LM | IN2LV4 | IN2LV3 | IN2LV2 | IN2LV1 | IN2LV0 | 68h |
| 88h | 08h | 0 | SICK | IN2RM | IN2RV4 | IN2RV3 | IN2RV2 | IN2RV1 | IN2RV0 | 68h |

These registers are used to set the IN2 input signal's mixer input volume. The correspondence between bits and gain settings is shown below. Gain can be set in a range from +12.0 dB to –34.5 dB, in 1.5 dB steps. The default value is 68h (gain: 0 dB, mute: ON).

- IN2LM: IN2 L channel mixer input mute control bit
- IN2RM: IN2 R channel mixer input mute control bit
- IN2LV[4:0]: IN2 L channel mixer input gain control bits
- IN2RV[4:0]: IN2 R channel mixer input gain control bits

**Table 2-8. Correspondence of Bits and Gain Settings in IN2 Volume Registers (07h, 08h)**

| IN2LM/IN2RM | IN2LV[4:0]/IN2RV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | +12.0 dB |
| 0 | 0 0001 | +10.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 0 1000 | 0 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | −33.0 dB |
| 0 | 1 1111 | −34.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 1000 | Default |

### 2.1.8 IN3 volume registers (09h, 0Ah)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 89h | 09h | 0 | SICK | IN3LM | IN3LV4 | IN3LV3 | IN3LV2 | IN3LV1 | IN3LV0 | 68h |
| 8Ah | 0Ah | 0 | SICK | IN3RM | IN3RV4 | IN3RV3 | IN3RV2 | IN3RV1 | IN3RV0 | 68h |

These registers are used to set the IN3 input signal's mixer input volume. The correspondence between bits and gain settings is shown below. Gain can be set in a range from +12.0 dB to –34.5 dB, in 1.5 dB steps. The default value is 68h (gain: 0 dB, mute: ON).

- IN3LM: IN3 L channel mixer input mute control bit
- IN3RM: IN3 R channel mixer input mute control bit
- IN3LV[4:0]: IN3 L channel mixer input gain control bits
- IN3RV[4:0]: IN3 R channel mixer input gain control bits

**Table 2-9. Correspondence of Bits and Gain Settings in IN3 Volume Registers (09h, 0Ah)**

| IN3LM/IN3RM | IN3LV[4:0]/IN3RV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | +12.0 dB |
| 0 | 0 0001 | +10.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 0 1000 | 0 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | –33.0 dB |
| 0 | 1 1111 | –34.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 1000 | Default |

### 2.1.9 IN4 volume registers (0Bh, 0Ch)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 8Bh | 0Bh | 0 | SICK | IN4LM | IN4LV4 | IN4LV3 | IN4LV2 | IN4LV1 | IN4LV0 | 68h |
| 8Ch | 0Ch | 0 | SICK | IN4RM | IN4RV4 | IN4RV3 | IN4RV2 | IN4RV1 | IN4RV0 | 68h |

These registers are used to set the IN4 input signal's mixer input volume. The correspondence between bits and gain settings is shown below. Gain can be set in a range from +12.0 dB to –34.5 dB, in 1.5 dB steps. The default value is 68h (gain: 0 dB, mute: ON).

- IN4LM: IN4 L channel mixer input mute control bit
- IN4RM: IN4 R channel mixer input mute control bit
- IN4LV[4:0]: IN4 L channel mixer input gain control bits
- IN4RV[4:0]: IN4 R channel mixer input gain control bits

**Table 2-10. Correspondence of Bits and Gain Settings in IN4 Volume Registers (0Bh, 0Ch)**

| IN4LM/IN4RM | IN4LV[4:0]/IN4RV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | +12.0 dB |
| 0 | 0 0001 | +10.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 0 1000 | 0 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | –33.0 dB |
| 0 | 1 1111 | –34.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 1000 | Default |

### 2.1.10 IN5 volume register (0Dh)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 8Dh | 0Dh | 0 | SICK | IN5M | IN5V4 | IN5V3 | IN5V2 | IN5V1 | IN5V0 | 68h |

This register is used to set the IN5 input signal's mixer input volume. The correspondence between bits and gain settings is shown below. Gain can be set in a range from +12.0 dB to –34.5 dB, in 1.5 dB steps. The default value is 68h (gain: 0 dB, mute: ON).

- IN5M: IN5 mixer input mute control bit
- IN5V[4:0]: IN5 mixer input gain control bits

**Table 2-11. Correspondence of Bits and Gain Settings in IN5 Volume Register (0Dh)**

| IN5M | IN5V[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | +12.0 dB |
| 0 | 0 0001 | +10.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 0 1000 | 0 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | –33.0 dB |
| 0 | 1 1111 | –34.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 1000 | Default |

### 2.1.11 MIC volume register (0Eh)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 8Eh | 0Eh | 0 | SICK | MICM | MICV4 | MICV3 | MICV2 | MICV1 | MICV0 | 68h |

This register is used to set the MIC's mixer input volume. The correspondence between bits and gain settings is shown below. Gain can be set in a range from +12.0 dB to –34.5 dB, in 1.5 dB steps. The default value is 68h (gain: 0 dB, mute: ON).

- MICM: MIC mixer input mute control bit
- MICV[4:0]: MIC mixer input gain control bits

**Table 2-12. Correspondence of Bits and Gain Settings in MIC Volume Register (0Eh)**

| MICM | MICV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | +12.0 dB |
| 0 | 0 0001 | +10.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 0 1000 | 0 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | –33.0 dB |
| 0 | 1 1111 | –34.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 1000 | Default |

### 2.1.12 IN6 volume register (0Fh)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 8Fh | 0Fh | 0 | SICK | IN6M | IN6V3 | IN6V2 | IN6V1 | IN6V0 | 0 | 60h |

This register is used to set the IN6 input signal's mixer input volume. The correspondence between bits and gain settings is shown below. Gain can be set in a range from 0 dB to –45 dB, in 3.0 dB steps. The default value is 60h (gain: 0 dB, mute: ON).

- IN6M: IN6 mixer input mute control bit
- IN6V[3:0]: IN6 mixer input gain control bits

**Table 2-13. Correspondence of Bits and Gain Settings in IN6 Volume Register (0Fh)**

| IN6M | IN6V[3:0] | Gain |
|---|---|---|
| 0 | 0000 | 0 dB |
| 0 | 0001 | –3.0 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1110 | –42.0 dB |
| 0 | 1111 | –45.0 dB |
| 1 | xxxx | Mute |
| 1 | 0000 | Default |

### 2.1.13 DAC volume registers (10h, 11h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 90h | 10h | 0 | SICK | DALM | DALV4 | DALV3 | DALV2 | DALV1 | DALV0 | 68h |
| 91h | 11h | 0 | SICK | DARM | DARV4 | DARV3 | DARV2 | DARV1 | DARV0 | 68h |

These registers are used to set the DAC output signal's mixer input volume. The correspondence between bits and gain settings is shown below. Gain can be set in a range from +12.0 dB to –34.5 dB, in 1.5 dB steps. The default value is 68h (gain: 0 dB, mute: ON).

- DALM: DAC L channel mixer input mute control bit
- DARM: DAC R channel mixer input mute control bit
- DALV[4:0]: DAC L channel mixer input gain control bits
- DARV[4:0]: DAC R channel mixer input gain control bits

**Table 2-14. Correspondence of Bits and Gain Settings in DAC Volume Registers (10h, 11h)**

| DALM/DARM | DALV[4:0]/DARV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | +12.0 dB |
| 0 | 0 0001 | +10.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 0 1000 | 0 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | –33.0 dB |
| 0 | 1 1111 | –34.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 1000 | Default |

### 2.1.14 OUT master volume registers (12h, 13h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 92h | 12h | 0 | SICK | OMLM | OMLV4 | OMLV3 | OMLV2 | OMLV1 | OMLV0 | 60h |
| 93h | 13h | 0 | SICK | OMRM | OMRV4 | OMRV3 | OMRV2 | OMRV1 | OMRV0 | 60h |

These registers are used to set the master volume for OUTL and OUTR and the gain for mixer output to the OUTL and OUTR pins. The correspondence between bits and gain settings is shown below. Gain can be set in a range from 0 dB to –46.5 dB, in 1.5 dB steps. The default value is 60h (gain: 0 dB, mute: ON).

- OMLM: OUTL output mute control bit
- OMRM: OUTR output mute control bit
- OMLV[4:0]: OUTL output gain control bits
- OMRV[4:0]: OUTR output gain control bits

**Table 2-15. Correspondence of Bits and Gain Settings in OUT Master Volume Registers (12h, 13h)**

| OMLM/OMRM | OMLV[4:0]/OMRV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | 0 dB |
| 0 | 0 0001 | –1.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | –45.0 dB |
| 0 | 1 1111 | –46.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 0000 | Default |

### 2.1.15 DAC master volume registers (14h, 15h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 94h | 14h | 0 | SICK | DMLM | DMLV4 | DMLV3 | DMLV2 | DMLV1 | DMLV0 | 60h |
| 95h | 15h | 0 | SICK | DMRM | DMRV4 | DMRV3 | DMRV2 | DMRV1 | DMRV0 | 60h |

These registers are used to set the master volume for DACL and DACR. The correspondence between bits and gain settings is shown below. Gain can be set in a range from 0 dB to –46.5 dB, in 1.5 dB steps. The default value is 60h (gain: 0 dB, mute: ON).

- DMLM: DACL output mute control bit
- DMRM: DACR output mute control bit
- DMLV[4:0]: DACL output gain control bits
- DMRV[4:0]: DACR output gain control bits

**Table 2-16. Correspondence of Bits and Gain Settings in DAC Master Volume Registers (14h, 15h)**

| DMLM/DMRM | DMLV[4:0]/DMRV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | 0 dB |
| 0 | 0 0001 | −1.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | −45.0 dB |
| 0 | 1 1111 | −46.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 0000 | Default |

### 2.1.16 MONO output master volume register (16h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 96h | 16h | 0 | SICK | MNMM | MNMV4 | MNMV3 | MNMV2 | MNMV1 | MNMV0 | 60h |

This register is used to set the master volume for MONO output. The correspondence between bits and gain settings is shown below. Gain can be set in a range from 0 dB to –46.5 dB, in 1.5 dB steps. The default value is 60h (gain: 0 dB, mute: ON).

- MNMM: MONO output mute control bit
- MNMV[4:0]: MONO output gain control bits

**Table 2-17. Correspondence of Bits and Gain Settings in MONO Output Master Volume Register (16h)**

| MNMM | MNMV[4:0] | Gain |
|---|---|---|
| 0 | 0 0000 | 0 dB |
| 0 | 0 0001 | –1.5 dB |
| ⋮ | ⋮ | ⋮ |
| 0 | 1 1110 | –45.0 dB |
| 0 | 1 1111 | –46.5 dB |
| 1 | x xxxx | Mute |
| 1 | 0 0000 | Default |

### 2.1.17 Path select register (17h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 97h | 17h | 0 | SICK | 0 | 1 | MIX | MS | MC20 | LPBK | 50h |

This register is used to set internal signal switching. The default value is 50h.

**Table 2-18. Signal Switching Settings in Path Select Register (17h)**

| Bit | MNMV[4:0] | Setting | |
|---|---|---|---|
| MIX | Mono Out Select | 0 | Mixer |
| | | 1 | MIC |
| MS | MIC Select | 0 | MIC1 |
| | | 1 | MIC2 |
| MC20 | MIC Gain Select | 0 | +0 dB |
| | | 1 | +20 dB |
| LPBK | ADC/DAC Analog Loop-back (test mode) | 0 | Off |
| | | 1 | On |

- MIX: This selects input of MONO output master volume, using either monaural signals from the mixer or monaural signals from the MIC.
- MS: This selects either MIC1 or MIC2 as the source for input to the MIC amp.
- MC20: This sets the MIC amp's gain as either 0 dB or 20 dB.
- LPBK: This selects analog loop-back mode. When in analog loop-back mode, the output from ADC is internally input directly to the DAC, which enables the analog circuit's operations and volume settings to be verified.

### 2.1.18 Power down control register (18h)

| Read Address | Write Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 98h | 18h | 0 | SICK | 0 | DIGPD | VREFPD | MIXPD | DACPD | ADCPD | 43h |

This register is used to set the power down mode. When one of its bits is set to "1", the specified block is set to power down mode. The relation between bits and internal circuits set to power down mode are shown in **Figure 2-1 Power Down Mode Block Diagram**. The default value is 40h.

**Table 2-19. Bits in Power Down Control Register (18h) and Power Down Functions**

| Bit | Function |
|---|---|
| DIGPD | Digital block/clock power down |
| VREFPD | Analog block power down |
| MIXPD | Mixer power down (valid when analog block is ON) |
| DACPD | DAC power down |
| ADCPD | ADC power down |

**Table 2-20. Bits in Power Down Control Register (18h) and Internal Circuits Set to Power Down Mode**

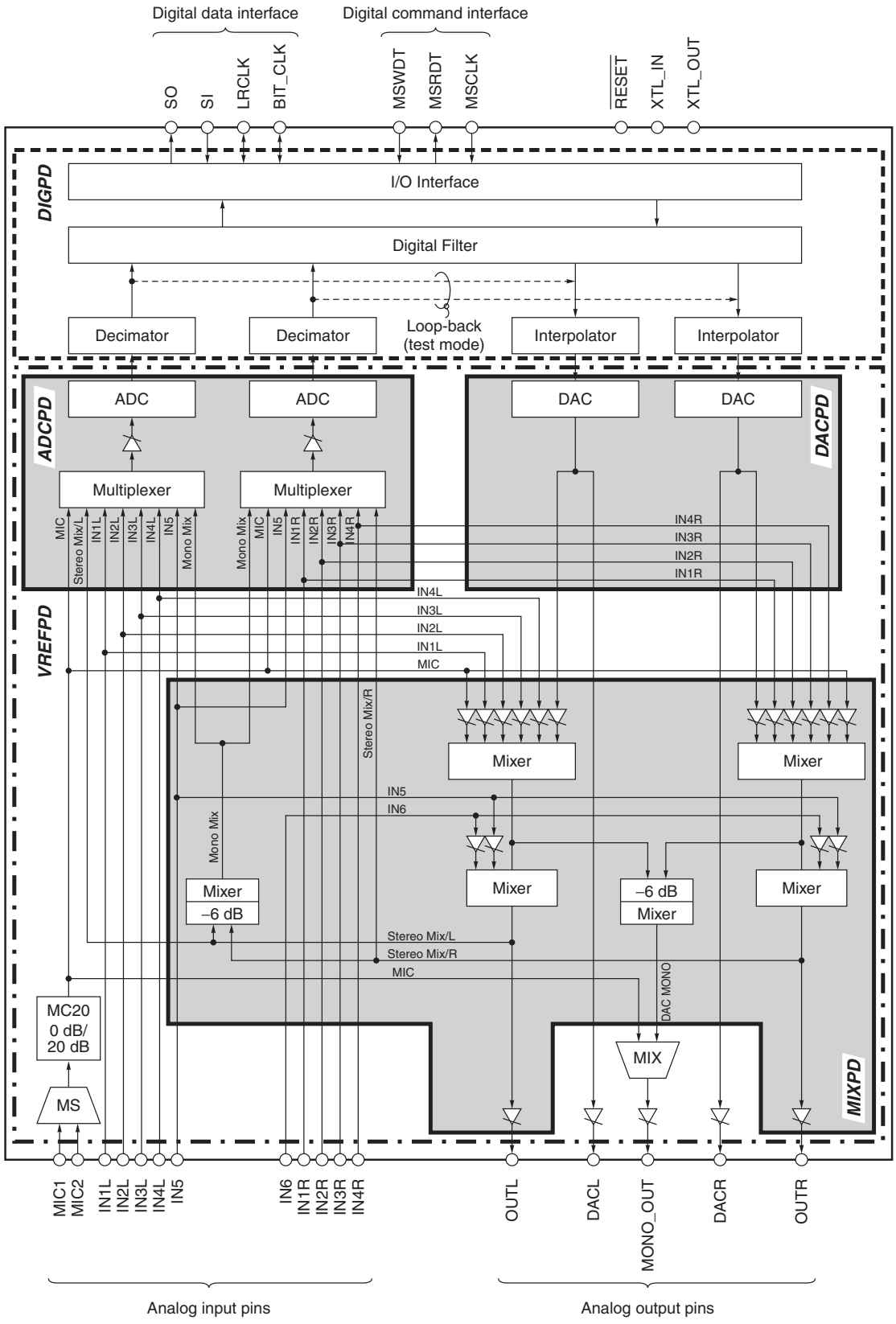
| Bit | ADC | DAC | Mixer Volume | Master Volume | Vref | Interface | Internal Clock |
|---|---|---|---|---|---|---|---|
| DIGPD | PD | PD | x | x | x | PD | PD |
| VREFPD | PD | PD | PD | PD | PD | x | x |
| MIXPD | x | x | PD | PD | x | x | x |
| DACPD | x | PD | x | x | x | x | x |
| ADCPD | PD | x | x | x | x | x | x |

**Cautions 1. When the BIT_CLK and LRCLK I/O settings are set to input, input of the BIT_CLK and LRCLK signals is required before releasing power down mode.**

**2. DIGPD (digital block/clock power down) is released by a cold or warm reset. If a warm reset is executed, the internal registers can be accessed, but because the DIGPD bit remains set to 1, some of the digital circuit operations will not resume. To ensure the resumption of these operations, therefore, set the DIGPD bit to 0 after a warm reset.**

**Remark** x: Normal operation, PD: Power down mode

**Figure 2-1. Power Down Mode Block Diagram**



### 2.1.19 Warm reset register (7Fh)

| Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|
| 7Fh | RW7 | RW6 | RW5 | RW4 | RW3 | RW2 | RW1 | RW0 | 00h |

When FFh is written to this register, the digital interface is initialized. Read access to this register and writing to other than FFh are prohibited.

**Table 2-21. Settings for Warm Reset Register (7Fh)**

| RW [7:0] | Function |
|---|---|
| 1111 1111 | Warm reset execution |

## 3. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Digital block power supply voltage | $DV_{DD}$ | | –0.3 to +4.6 | V |
| Analog block power supply voltage | $AV_{DD}$ | | –0.3 to +4.6 | V |
| Input current | $I_I$ | Pins except power supply and ground | –10 to +10 | mA |
| Digital input voltage | $DV_I$ | All digital input pins | –0.3 to $DV_{DD}$ + 0.3 | V |
| Analog input voltage | $AV_I$ | All analog input pins | –0.3 to $AV_{DD}$ + 0.3 | V |
| Operating ambient temperature | $T_A$ | Device ambient temperature | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | –65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

### Recommended Operation Range ($DV_{SS}$ = $AV_{SS}$ = 0 V, load capacitance = 20 pF)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Digital block power supply voltage | $DV_{DD}$ | | 3.0 | 3.3 | 3.6 | V |
| Analog block power supply voltage | $AV_{DD}$ | | 3.0 | 3.3 | 3.6 | V |
| Operating ambient temperature | $T_A$ | Device ambient temperature | –40 | +25 | +85 | °C |
| Master clock frequency | $f_{MCLK}$ | | 1.024 | – | 24.576 | MHz |
| Master clock duty factor **Note** | $f_{DTY}$ | | 45 | 50 | 55 | % |
| Sampling frequency | $f_S$ | | 0.4 | – | 48 | kHz |
| Digital input voltage (high level) | $V_{IH}$ | | 1.95 | – | – | V |
| Digital input voltage (low level) | $V_{IL}$ | | – | – | 1.26 | V |
| Analog input signal voltage | $V_I$ | | – | 0.7 | – | $V_{r.m.s.}$ |
| Analog output pin load resistance | $R_L$ | Analog output pin | 10 | – | – | kΩ |

**Note** Using a master clock duty factor that is outside the recommended operation range may result in degradation of analog characteristics.

**Digital Block DC Characteristics ($DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C)**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Digital block current consumption | $I_{DV1}$ | During normal operation | – | 10.0 | 15.0 | mA |
| Digital standby current | $I_{DV2}$ | During power down mode | – | 0.0 | 0.1 | mA |
| Input leakage current | $I_{LI}$ | | –10.0 | – | +10.0 | μA |
| Output leakage current | $I_{LO}$ | During high impedance mode | –10.0 | – | +10.0 | μA |
| Input voltage, high | $V_{IH}$ | | 1.95 | – | – | V |
| Input voltage, low | $V_{IL}$ | | – | – | 1.26 | V |
| Output voltage, high | $V_{OH}$ | Output current = –5.0 mA | 2.70 | – | – | V |
| Output voltage, low | $V_{OL}$ | Output current = 5.0 mA | – | – | 0.36 | V |
| Pull-up resistance | $R_{UP}$ | | 20 | 50 | 100 | kΩ |

**Analog Block DC Characteristics ($DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C)**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Analog block current consumption | $I_{AV1}$ | During normal operation | – | 40.0 | 50.0 | mA |
| Analog standby current | $I_{AV2}$ | During power down mode | – | 0.0 | 0.1 | mA |
| Reference voltage | $V_{REF}$ | | 1.35 | 1.4 | 1.45 | V |
| Analog input voltage | $V_{AI}$ | Except for MIC input | – | 0.7 | – | $V_{r.m.s.}$ |
| | $V_{MI0}$ | +20 dB = ON | – | 0.07 | – | $V_{r.m.s.}$ |
| | $V_{MI20}$ | +20 dB = OFF | – | 0.7 | – | $V_{r.m.s.}$ |
| Analog output voltage | $V_{AO}$ | | – | 0.7 | – | $V_{r.m.s.}$ |
| Input impedance | $A_{LB}$ | | 10 | – | – | kΩ |

**AD Block Transmission Characteristics (unless otherwise specified, $DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C, sampling frequency = 48 kHz, bandwidth = 20 Hz to 19.2 kHz, input signal = 1 kHz)**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| AD dynamic range | $DR_X$ | –60 dB input | 75 | 85 | – | dB |
| AD total harmonic distortion | $THD_X$ | –3 dB input | – | 0.01 | 0.02 | % |
| AD absolute gain | $G_X$ | 0 dB input | –1.0 | ±0.5 | +1.0 | dB |
| AD frequency gain characteristic | $GR_X$ | 20 Hz to 19.2 kHz | –0.25 | ±0.1 | +0.25 | dB |
| AD offset voltage | $V_{OFFX}$ | | –50 | ±10 | +50 | mV |
| AD crosstalk | $XTK_X$ | vs. input channel | – | –85 | –70 | dB |
| AD full-scale analog input amplitude **Note** | $VIFS_X$ | | – | 0.7 | – | $V_{r.m.s.}$ |

**Note** The AD full-scale analog input amplitude ($VIFS_X$) indicates the input amplitude of the internal AD converter. Before inputting to the AD converter, calculate the amplitude that does not exceed this value from the setting values of MIC amp and each volume.

**DA Block Transmission Characteristics (unless otherwise specified, $DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C, sampling frequency = 48 kHz, bandwidth = 20 Hz to 19.2 kHz, input signal = 1 kHz)**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| DA dynamic range | $DR_R$ | –60 dB input | 80 | 90 | – | dB |
| DA total harmonic distortion | $THD_R$ | –3 dB input | – | 0.01 | 0.02 | % |
| DA absolute gain | $G_R$ | 0 dB input | –1.0 | ±0.5 | +1.0 | dB |
| DA frequency gain characteristic | $GR_R$ | 20 Hz to 19.2 kHz | –0.25 | ±0.1 | +0.25 | dB |
| DA offset voltage | $V_{OFFR}$ | | –50 | ±10 | +50 | mV |
| DA crosstalk | $XTK_R$ | vs. input channel | – | –85 | –70 | dB |
| DA full-scale analog output amplitude | $VOFS_R$ | | – | 0.7 | – | $V_{r.m.s.}$ |

**MIC Block Transmission Characteristics (unless otherwise specified, $DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C, sampling frequency = 48 kHz, bandwidth = 20 Hz to 19.2 kHz, input signal = 1 kHz)**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| MIC absolute gain | $G_{MC20}$ | –20 dB input, +20 dB = ON | 18 | 20 | 22 | dB |

**Mixer Block Transmission Characteristics (unless otherwise specified, $DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C, sampling frequency = 48 kHz, bandwidth = 20 Hz to 19.2 kHz, input signal = 1 kHz)**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Dynamic range | $DR_A$ | –60 dB input | 85 | 90 | – | dB |
| Total harmonic distortion | $THD_A$ | –3 dB input | – | 0.01 | 0.02 | % |
| Absolute gain | $G_A$ | 0 dB input | –1.0 | ±0.5 | +1.0 | dB |
| Frequency gain characteristic | $GR_A$ | 20 Hz to 19.2 kHz | –0.25 | ±0.1 | +0.25 | dB |
| Offset voltage | $V_{OFFA}$ | | –50 | ±10 | +50 | mV |
| Crosstalk | $XTK_A$ | vs. input channel | – | –80 | –70 | dB |
| Full-scale analog input amplitude | $VIFS_A$ | | – | 0.7 | – | $V_{r.m.s.}$ |
| Full-scale analog output amplitude | $VOFS_A$ | | – | 0.7 | – | $V_{r.m.s.}$ |

**AC Characteristics, Digital Block (unless otherwise specified, $DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C)**

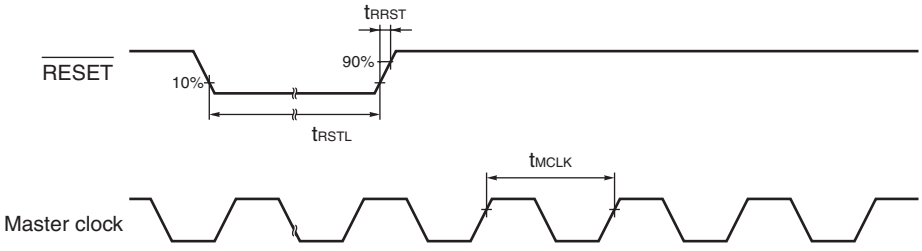
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $\overline{\text{RESET}}$ rise time | $t_{RRST}$ | Time for $V_{DD}$ to change from 10% to 90% | – | – | 1.0 | μs |
| $\overline{\text{RESET}}$ low-level width[Notes 1, 2] | $t_{RSTL}$ | | 4.0 | – | – | μs |
| Master clock frequency[Note 3] | $f_{MCLK}$ | | 1.024 | – | 24.576 | MHz |

**Notes 1.** $t_{RSTL}$ is the time required for initialization of this LSI. When performing a reset, set $\overline{\text{RESET}}$ to active (low level) for $t_{RSTL}$ period.

**2.** The internal reset circuit operates as a trigger for the master clock. The master clock should be input even while executing a reset.

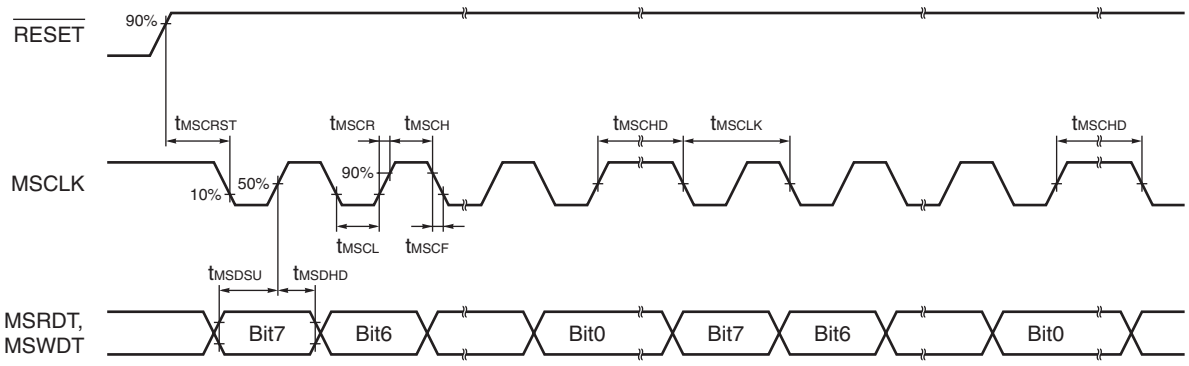
**3.** When using the on-chip clock generator (when a crystal resonator is connected to XTL_OUT or XTL_IN pin), only 24.576 MHz can be selected for $f_{MCLK}$. When using a frequency other than 24.576 MHz, be sure to input an externally generated clock directly to the XTL_IN pin.

★



**AC Characteristics, Serial Command Interface Block (unless otherwise specified, $DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C)**

| | Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | MSCLK cycle | $t_{MSCLK}$ | | 240 | – | – | ns |
| | MSCLK high-level width | $t_{MSCH}$ | | 100 | – | – | ns |
| | MSCLK low-level width | $t_{MSCL}$ | | 100 | – | – | ns |
| | MSCLK rise time | $t_{MSCR}$ | | – | – | 20 | ns |
| | MSCLK fall time | $t_{MSCF}$ | | – | – | 20 | ns |
| ★ | Setup time from $\overline{RESET}$ to MSCLK | $t_{MSCRST}$ | | 8 | – | – | $t_{MCLK}$ |
| ★ | Data I/O start time | $t_{MSCHD}$ | | 8 | – | – | $t_{MCLK}$ |
| | Data setup time | $t_{MSDSU}$ | | 50 | – | – | ns |
| | Data hold time | $t_{MSDHD}$ | | 50 | – | – | ns |

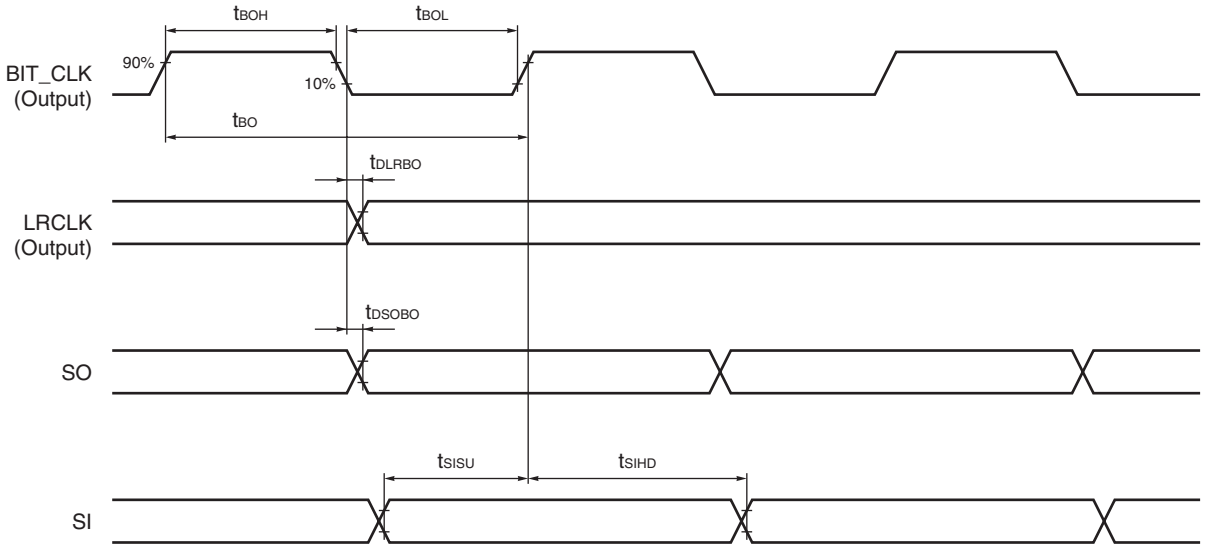


**AC Characteristics, Serial Data Interface Block (unless otherwise specified, $DV_{DD}$ = $AV_{DD}$ = 3.3 V, $DV_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = –40 to +85°C)**

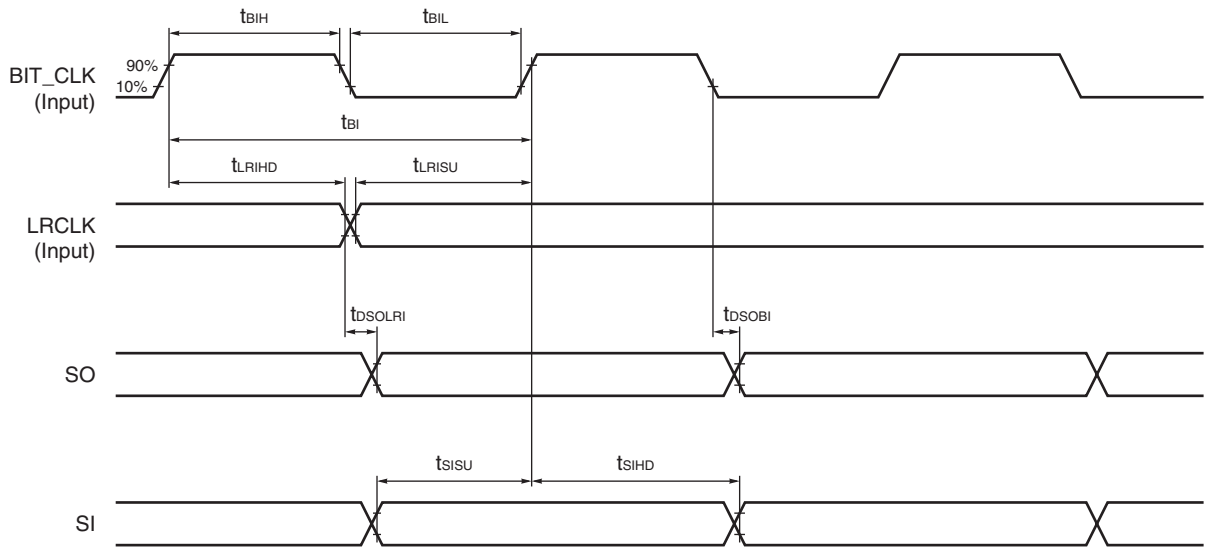
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| BIT_CLK input signal cycle | $t_{BI}$ | During BIT_CLK input | 325.5 | – | – | ns |
| BIT_CLK input signal high-level width | $t_{BIH}$ | During BIT_CLK input | 100 | – | – | ns |
| BIT_CLK input signal low-level width | $t_{BIL}$ | During BIT_CLK input | 100 | – | – | ns |
| BIT_CLK output signal cycle[Note] | $t_{BO}$ | During BIT_CLK output | 325.5 | – | – | ns |
| BIT_CLK output signal high-level width | $t_{BOH}$ | During BIT_CLK output | 125 | – | – | ns |
| BIT_CLK output signal low-level width | $t_{BOL}$ | During BIT_CLK output | 125 | – | – | ns |
| LRCLK-BITCLK setup time | $t_{LRISU}$ | During LRCLK input | 50 | – | – | ns |
| LRCLK-BITCLK hold time | $t_{LRIHD}$ | During LRCLK input | 50 | – | – | ns |
| Delay time from LRCLK to SO 1 | $t_{DSOLRI}$ | During LRCLK input | – | – | 70 | ns |
| Delay time from LRCLK to SO 2 | $t_{DLRBO}$ | During LRCLK output | –40 | – | +65 | ns |
| Delay time from BIT_CLK fall to SO 1 | $t_{DSOBI}$ | During BIT_CLK input | – | – | 70 | ns |
| BIT_CLK fall to SO 2 | $t_{DSOBO}$ | During BIT_CLK output | –40 | – | +65 | ns |
| SI setup time | $t_{SISU}$ | | 50 | – | – | ns |
| SI hold time | $t_{SIHD}$ | | 50 | – | – | ns |

**Note** When the number of bit clocks per frame in the serial data format is set to 48 according to the internal BIT_CLK generator configuration, the BIT_CLK output signal duty factor is not constant; some variation of master clock cycle may occur.

**Serial Data I/O Timing (BIT_CLK and LRCLK input)**

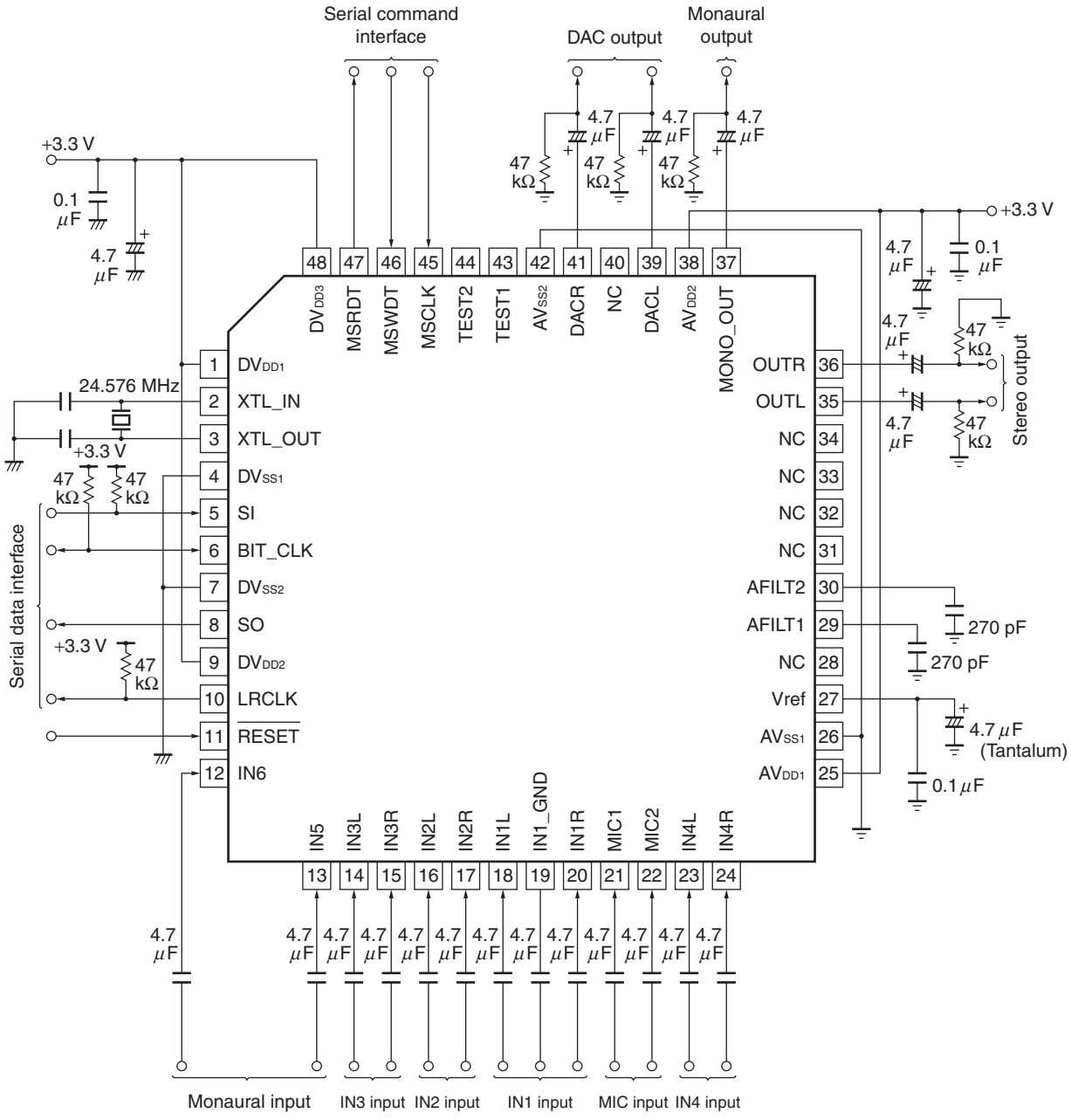


**Serial Data Output Timing (BIT_CLK and LRCLK output)**



## 4. APPLICATION CIRCUIT EXAMPLE

**Figure 4-1. Application Circuit Example**



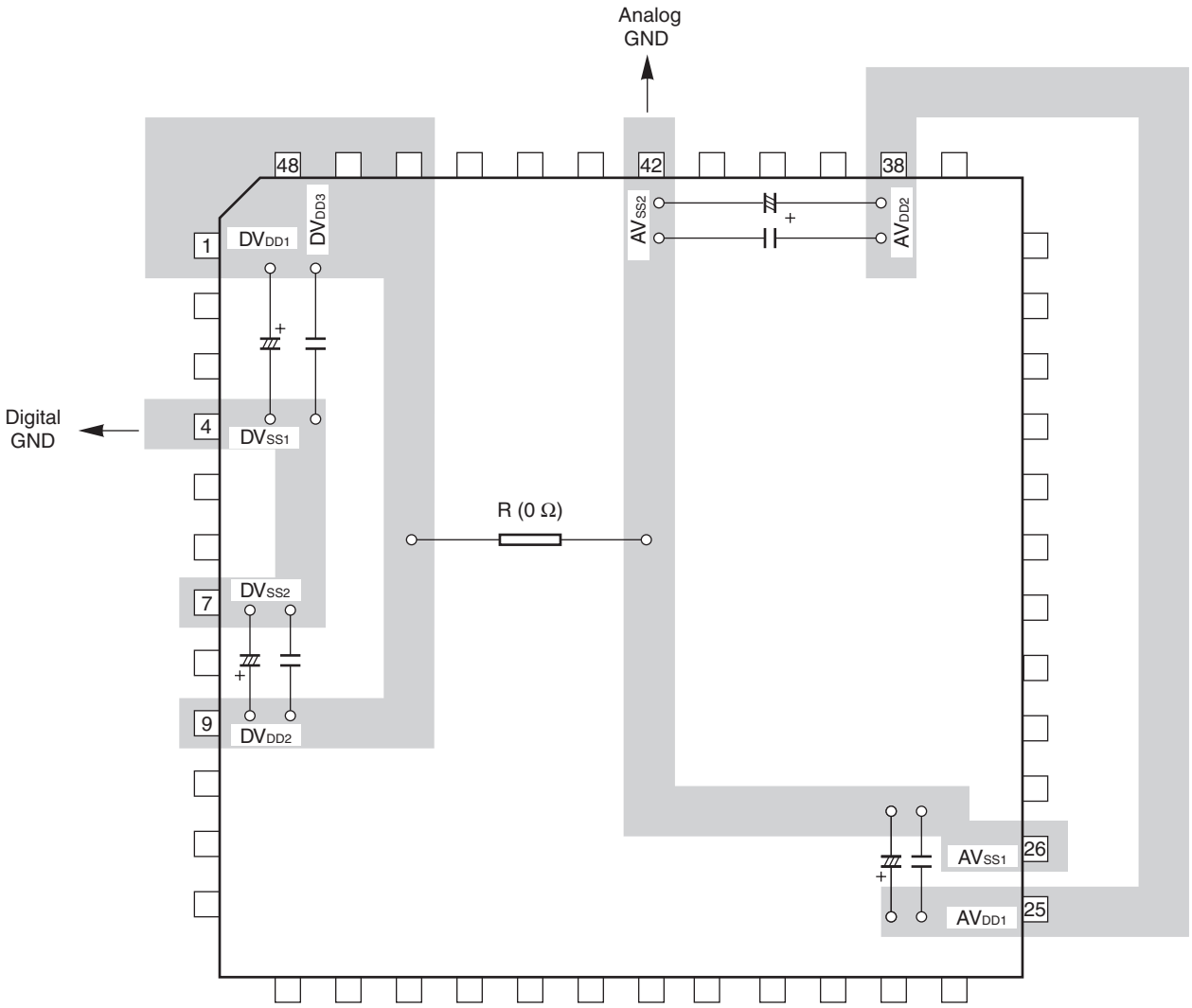

**Remark** ⏚ : Analog ground

⏚ : Digital ground

## 5. RECOMMENDED LAND PATTERN

Refer to the figure below for details of power supply and ground line wiring and the placement of bypass capacitors on the board. It is recommended to place bypass capacitors as close as possible to pins by utilizing the underside of the board, or by some other means.

**Figure 5-1. Recommended Land Pattern**



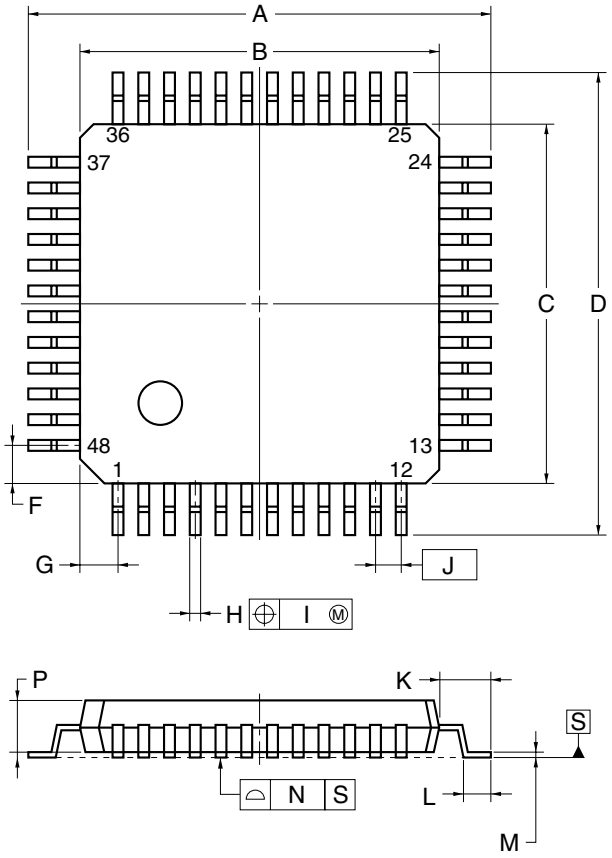

**Caution R (0 Ω) : Connect analog and digital GND at one point immediately below or adjacent to the codec.**

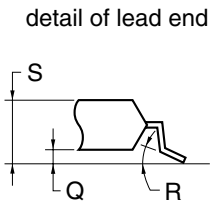
**Remark** (4.7 μF) : Tantalum capacitor

(0.1 μF) : Chip ceramic capacitor

## 6. PACKAGE DRAWING

## 48-PIN PLASTIC TQFP (FINE PITCH) (7x7)




**NOTE**

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 9.0±0.2 |
| B | 7.0±0.2 |
| C | 7.0±0.2 |
| D | 9.0±0.2 |
| F | 0.75 |
| G | 0.75 |
| H | $0.22^{+0.05}_{-0.04}$ |
| I | 0.10 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | $0.145^{+0.055}_{-0.045}$ |
| N | 0.10 |
| P | 1.0±0.1 |
| Q | 0.1±0.05 |
| R | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |
| S | 1.27 MAX. |

**S48GA-50-9EU-2**

## 7. RECOMMENDED SOLDERING CONDITIONS

The μPD63335 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

**Table 6-1. Surface Mounting Type Soldering Conditions**

- μPD63335GA-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: three times or less, Exposure limit Note: 3 days (after that, prebaking is necessary at 125°C for 10 hours) | IR35-103-3 |
| VSP | Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: three times or less, Exposure limit Note: 3 days (after that, prebaking is necessary at 125°C for 10 hours) | VP15-103-3 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | – |

**Note** The number of days for storage after the dry pack has been opened. Storage conditions are 25°C and 65% RH max.

**Caution Do not use different soldering methods together (except for partial heating).**

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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