## FEATURES

- Superior Performance: 400 Mb/s
- Operating Range: 0° to +70° C
- Power Dissipation: 9.4 Watts (Nominal), 14.7 Watts (Max)
- Clocked or Flow-Through Operation
- ECL 100K Compatible Inputs and Outputs
- Clocked Mode Output-to-Output Skew: < 1100 ps
- Single Power Supply: -2 V ± 5%
- Full Diagnostic Monitors

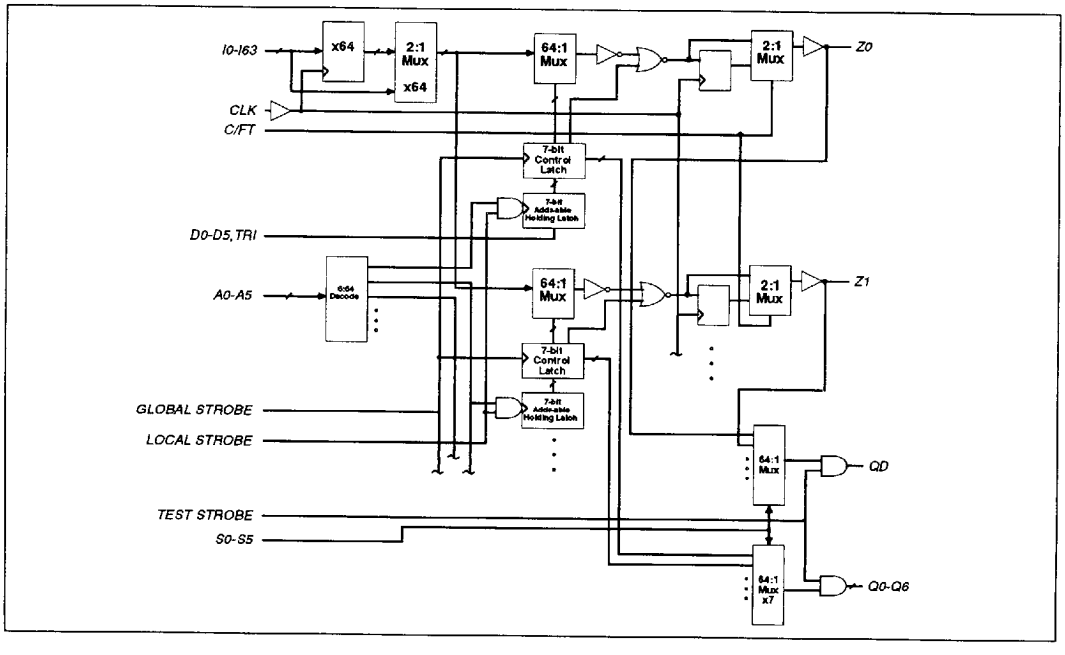


## INTRODUCTION

The VSC864A-4 is a 64 x 64 crosspoint switch intended for digital communications applications requiring up to 400 Mb/s performance. The VSC864A-4 allows any of its 64 data inputs to be multiplexed to any, some, or all of its 64 data outputs. For example, broadcast mode sends a single specified data input to all 64 data outputs. In clocked mode, any two outputs will exhibit less than 1100 ps of skew.

The VSC864A-4 crosspoint switch is ideal for digital applications including data distribution for telecommunications, computer network and multiprocessor switching, test equipment, and video switching. In a telecommunications SONET application, for example, the VSC864A-4 can be used as an STS-3 protection switch, or in the fabric of a large switching system.

## FUNCTIONAL BLOCK DIAGRAM



The VSC864A-4 can be operated either in asynchronous flow-through or synchronous clocked mode by use of internal input and output registers. In flow-through mode, the data propagation delay is less than 5 ns. The individual address latches are double buffered and a local strobe signal is used to load an individual address for each output pin while a global broadcast strobe is used to simultaneously activate all 64 destination addresses. The VSC864A-4 incorporates a separate diagnostic bus, Q-bus, to allow observation of individual internal multiplexer address latches.

The VSC864A-4 is implemented using Vitesse's proprietary H-GaAs II process which offers much better speed power performance than silicon alternatives. At 400 Mb/s, nominal power dissipation is 9.4 W. The input and output signal levels are compatible with industry standard ECL 100K signal levels and the part operates off of a single -2 V power supply. This product is packaged in a 344-pin ceramic leaded chip carrier (LDCC) which has been designed for optimal electrical and thermal performance.

## FUNCTIONAL DESCRIPTION

The VSC864A-4 may be used to connect any one of 64 inputs to any combination of 64 output channels, according to a user defined bit pattern stored in each channel's control latch.

During normal operation, signals flow from inputs ($\mathbf{I_0}$ - $\mathbf{I_{63}}$) to output channels ($\mathbf{Z_0}$ - $\mathbf{Z_{63}}$) through sixty-four, 64:1 multiplexers. The traffic pattern is controllable by data previously stored in sixty-four 7-bit control latches with each latch corresponding to an output channel. The first 6 least significant bits in each control latch are reserved for designating the MUX input which will be connected to its corresponding output, the most significant bit is used to tri-state this output if desired. The 6 LSBs are a binary numerical representation of the input channel selected (i.e., 000000 corresponds to $\mathbf{I_0}$, 000001 corresponds to $\mathbf{I_1}$, etc.).

The Write mode is used to alter any one or all signal paths. During Write mode, inputs $\mathbf{A_0}$ - $\mathbf{A_5}$ select which output channel's control latch will be altered (also by a binary numerical representation). Inputs $\mathbf{D_0}$- $\mathbf{D_5}$ describe the new input signal to be selected for that channel. When a high pulse is applied to **LOCAL STROBE**, $\mathbf{D_0}$- $\mathbf{D_5}$ and the **TRI** bit is transferred into a holding latch. After some or all control latches are programmed, a high pulse is applied to **GLOBAL STROBE** to transfer the information from the holding latches into all the control latches. In this way the entire crosspoint switch can be reconfigured simultaneously.

The Read mode is a diagnostic feature used to examine the data stored in any one control latch and its corresponding 64:1 multiplexer output. The control latch to be examined is selected by inputs $\mathbf{S_0}$- $\mathbf{S_5}$ (by a binary numerical representation). When a high pulse is applied to the **TEST STROBE**, the contents of the selected control latch will be displayed at the $\mathbf{Q_0}$- $\mathbf{Q_6}$ outputs and the corresponding 64:1 mux output will appear at the **QD** output. When **TEST STROBE** is "low" the Q bus has all low outputs (which is equivalent to being tri-stated).

The VSC864A-4 can be configured to run in either synchronous clocked mode or asynchronous flow-through mode. This feature is controlled by the **C/FT** input. When **C/FT** is high, the chip is in clocked mode and will require an input clock at its **CK** pin. In this mode all input and output data is registered. When **C/FT** is low the chip is in flow-through mode and will ignore the **CK** input. In clocked mode, the outputs on the monitor bus ($\mathbf{Q_0}$- $\mathbf{Q_6}$, and **QD**), and input data ($\mathbf{I_0}$ - $\mathbf{I_{63}}$) are registered by the master clock (**CK**).

## ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage (ECL), $V_{TT}$ potential to GND ..... -3.0V to +0.5V
Input Voltage Applied, $V_{ECLIN}$ ..... -2.5V to +0.5V
Output Current, $I_{OUT}$,(DC, output HI) ..... 100 mA
Case Temperature Under Bias, $T_C$ ..... -55° to +125°C
Storage Temperature (ambient), $T_{STG}$ ..... -65°C to +150°C

## RECOMMENDED OPERATING CONDITIONS

ECL Supply Voltage, $V_{TT}$ ..... -2.0V ± 0.1V
Commercial Operating Temperature Range, $T$ (2) ..... 0° to 70°C

*NOTES:* *(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
*(2) Lower limit of specification is ambient temperature and upper limit is case temperature.*

2

## DC CHARACTERISTICS

### ECL Inputs/Outputs

*(Over recommended commercial operating conditions. $V_{CC} = V_{CCA} = GND$, Output load 50Ω to $V_{TT}$.)*

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | -1020 | -850 | -700 | mV | $V_{IN} = V_{IH}$ (max) |
| $V_{OL}$ | Output LOW voltage | $V_{TT}$ | — | -1620 | mV | or $V_{IL}$ (min), $V_{TT}$ = -2.0V |
| $V_{IH}$ | Input HIGH voltage | -1100 | — | -700 | mV | Guaranteed HIGH for all inputs |
| $V_{IL}$ | Input LOW voltage | $V_{TT}$ | — | -1540 | mV | Guaranteed LOW for all inputs |
| $I_{IH}$ | Input HIGH current | — | — | 200 | µA | $V_{IN} = V_{IH}$ max |
| $I_{IL}$ | Input LOW current | -50 | — | — | µA | $V_{IN} = V_{IL}$ min |
| $I_{TT}$ | Supply current | — | 4.7 | 7 | A | $V_{TT}$ = -2.10V |

## FLOW-THROUGH AND CLOCKED MODE AC TIMING CHARACTERISTICS

*(Over recommended operating conditions. $V_{CC} = V_{CCA}$= GND. Output load 50Ω to $V_{TT}$.)*

### Flow-Through Mode

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $PW$ | Minimum data valid time | 2.0 | — | ns | ≤20% Duty Cycle Distortion; 50% input Duty Cycle |
| $t_{DR}$ | Propagation delay (rising) | 2.8 | 4.8 | ns | — |
| $t_{DF}$ | Propagation delay (falling) | 2.8 | 4.8 | ns | — |
| skew | Output to output skew | — | 1.8 | ns | On a given part |
| BER | Bit Error Rate | — | $10^{-13}$ | — | Note (2) |

*NOTES:* *(1) Duty cycle distortion* = $\frac{\text{duty cycle out - duty cycle in}}{\text{duty cycle in}}$ x 100%

*(2) Based on limited measurement time, not device performance limitations.*

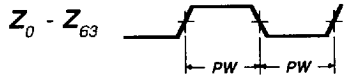
### Clocked Mode

| *Parameters* | *Description* | *Min* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum clock rate | — | 400 | MHz | — |
| $t_{ISU}$ | Input data set-up time | 0 | — | ns | — |
| $t_{IH}$ | Input data hold time | 1.5 | — | ns | — |
| $t_{CZR}$ | Clock to output delay (rising) | 2.0 | 3.5 | ns | — |
| $t_{CZF}$ | Clock to output delay (falling) | 2.0 | 3.5 | ns | — |
| skew | Output to output skew | — | 1.1 | ns | On a given part |

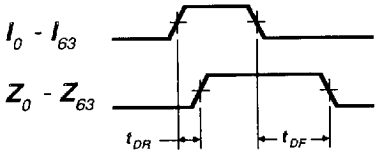
## FLOW-THROUGH AND CLOCKED MODE AC TIMING WAVEFORMS

**Flow-Through Mode**

Minimum Data Valid Time, ***PW***

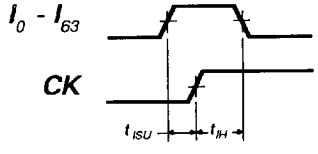



Propagation Delay

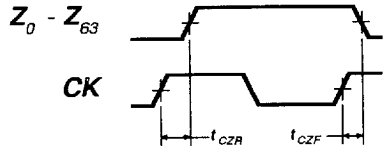



**Clocked Mode**

Input Data Set-up & Hold Times




Clock to Output Delay



## WRITE AND READ MODE AC TIMING CHARACTERISTICS

*(Over recommended commercial operating conditions. $V_{CC} = V_{CCA} = GND$.*

### Write Mode

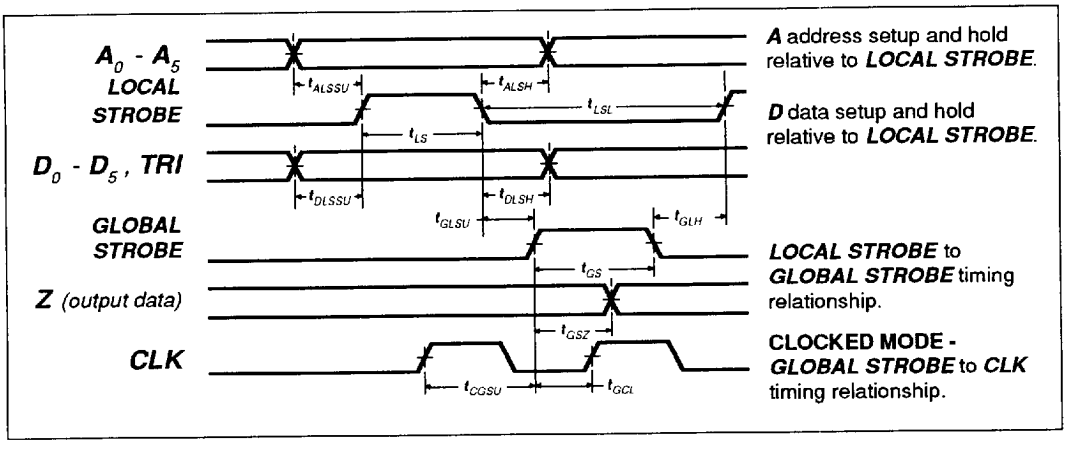
| Parameters | Description | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| $t_{RECON}$ | Reconfiguration time | 650 | 1300 | — | ns | 64 channel reconfig |
| $t_{ALSSU}$ | A bus to ***LOCAL STROBE*** set-up time | 300 | — | — | ps | — |
| $t_{ALSH}$ | A bus to ***LOCAL STROBE*** hold time | 0 | — | — | ps | — |
| $t_{DLSSU}$ | D bus to ***LOCAL STROBE*** set-up time | 400 | — | — | ps | — |
| $t_{DLSH}$ | D bus to ***LOCAL STROBE*** hold time | 2 | — | — | ns | — |
| $t_{GLSU}$ | ***GLOBAL STROBE*** to ***LOCAL STROBE*** set-up time | 5 | — | — | ns | — |
| $t_{GS}$, $t_{LS}$, | ***GLOBAL STROBE*** and ***LOCAL STROBE*** pulse widths | 5 | — | — | ns | Recommended local strobe frequency = 50 MHz |
| $t_{LSL}$ | ***LOCAL STROBE*** low time | 5 | — | — | ns | — |
| $t_{GLH}$ | ***GLOBAL STROBE*** to ***LOCAL STROBE*** hold time | 0 | — | — | ps | — |
| $t_{GSZ}$ | ***GLOBAL STROBE*** to valid output (flow-thrrough mode) | 2.7 | — | 5.6 | ns | — |
| $t_{CGSU}$ | ***CLK*** to ***GLOBAL STROBE*** set-up time (clocked mode) | 200 | — | — | ps | Data being clocked in at this time is invalid |
| $t_{GCL}$ | ***GLOBAL STROBE*** to ***CLK*** hold time (clocked mode) | 3.5 | — | — | ns | |

### Read Mode

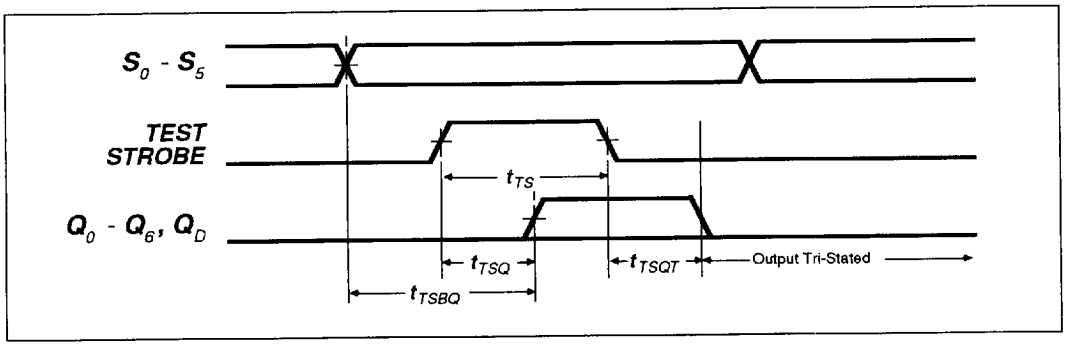
| Parameters | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $t_{TS}$ | ***TEST STROBE*** pulse width | 6.5 | — | — | ns | — |
| $t_{TSQ}$ | ***TEST STROBE*** to valid Q output | — | — | 7.1 | ns | — |
| $t_{TSBQ}$ | S bus to valid output | — | — | 7.1 | ns | — |
| $t_{TSQT}$ | ***TEST STROBE*** to tri-state condition on Q | — | — | 6.5 | ns | — |

## WRITE AND READ MODE AC TIMING WAVEFORMS

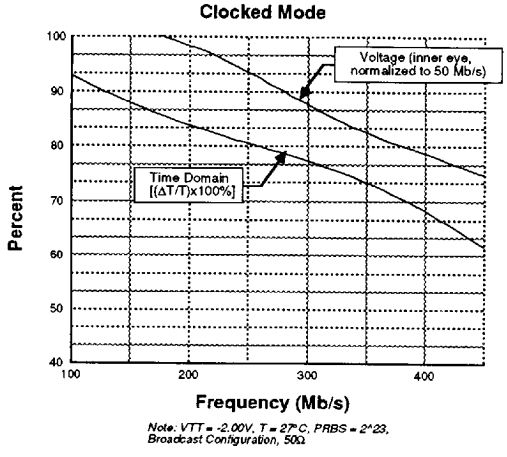
### Write Mode

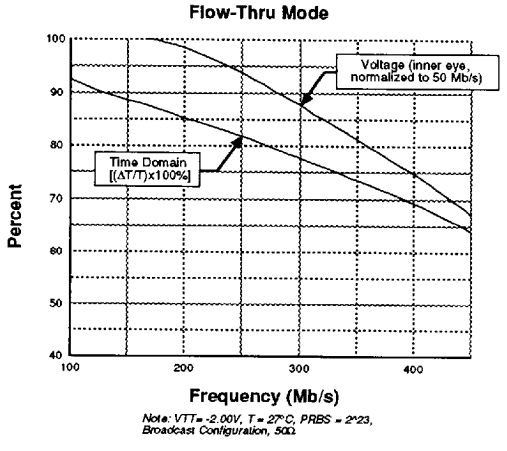



### Read Mode



## AC PERFORMANCE MEASUREMENTS (Percent Recoverable "Eye" vs Frequency)




### Typical Error-Free Area

The above graphs show the typical error-free area of a $2^{23}$ Pseudo-Random Bit Stream "eye" pattern in Clocked and Flow-Thru modes. The percent eye opening data was measured with the VSC864A-4 switching one input, **I1**, to all 64 outputs (broadcast configuration). Virtually no degradation of the data eye was seen below 50 Mb/s.

While switching all 64 data outputs simultaneously, a typical eye pattern of one of these outputs, **Z9**, was analyzed to obtain the percent eye opening vs. data rate curves.

For the time domain, the error-free region of the data eye ($\Delta$**T**) was measured and compared to the total data bit period (**T**). The percent eye opening curves in the time domain were then calculated using the following formula:

$$(\Delta T/T) \times 100\%$$

Voltage values were referenced to an initial inner eye measurement at 50 Mb/s. Subsequent percentage values were computed using the following formula:

$$V_{INNER} \times 100/V_{INNER} @ 50 \text{ Mb/s}$$

## PIN DESCRIPTION

| Pin # | Name | I/O | Description |
|---|---|---|---|
| 12-16, 20-30, 35-45, 49-53, 184-188, 192- 202, 207-217, 221-225 | $I_0$ - $I_{63}$ | I | The 64 ECL signal inputs. |
| 11 | ***TRI*** | I | ECL input containing Tristate data to be loaded into a 64:1 Mux holding latch. (Tristate = HIGH) Combined with a control register's destination address. Used to tristate the corresponding output. |
| 5-10 | $D_0$ - $D_5$ | I | ECL inputs containing the destination address to be loaded into the 64:1 Mux holding latch. |
| 178-183 | $A_0$ - $A_5$ | I | ECL inputs containing the address of the 64:1 Mux holding/control latch to be programmed. |
| 177 | ***LOCAL STROBE*** | I | Active HIGH, ECL input used to load the D0-D5 and TRI data into the 64:1 Mux holding latch. |
| 34 | ***GLOBAL STROBE*** | I | Active HIGH, ECL input used to load destination addresses to all 64:1 Mux control latches simultaneously from the data contained in their corresponding holding latches. |
| 54-59 | $S_0$ - $S_5$ | I | ECL inputs containing the address of the control latch to be observed at the QD output when the TEST STROBE is HIGH. |
| 60 | ***TEST STROBE*** | I | Active HIGH, ECL input used to enable Test Mode and observation of a selected 64:1 Mux control latch's destination address. |
| 206 | ***C/FT*** | I | ECL input used to enable Clocked or Flow-through Mode (Clocked = HIGH / Flow-Thru = LOW). |
| 203 | ***CK*** | I | ECL clock input for Clocked Mode. |
| 68, 71, 73, 78, 80, 83, 85, 88, 92, 95, 97, 100, 102, 107, 109, 112, 126, 129, 131, 136, 138, 141,143, 148, 150, 153, 155,158, 162, 165, 167, 170, 240, 243, 245, 250, 252, 255, 257, 260, 264, 267, 269, 272, 274, 279, 281, 284, 298, 301, 303, 308, 310, 313, 315, 320, 322, 325, 327, 330, 334, 337, 339, 342 | $Z_0$ - $Z_{63}$ | O | The 64 ECL signal outputs. |
| 296 | ***QD*** | O | ECL output used to observe the output of a selected 64:1 Mux in Test Mode. |
| 114, 117, 121, 124, 286, 289, 293 | $Q_0$ - $Q_6$ | O | ECL outputs containing the selected 64:1 Mux control register's destination address and TRI bit in Test Mode. |
| 3, 17, 32, 47, 61, 76, 90, 104, 118, 132, 146, 160, 175, 189, 204, 219, 233, 248, 262, 276, 290, 304, 318, 332 | $V_{CC}$ | | ØV ground connection for internal logic. |
| 2, 63, 69, 74, 81, 86, 93, 98, 103, 110, 115, 122, 127, 134, 139, 144, 151, 156, 163, 168, 174, 235, 241, 246, 253, 258, 265, 270, 275, 282, 287, 294, 299, 306, 311, 316, 323, 328, 335, 340 | $V_{CCA}$ | | ØV 'dirty' ground connection for outputs. |

## PIN DESCRIPTION (CONT.)

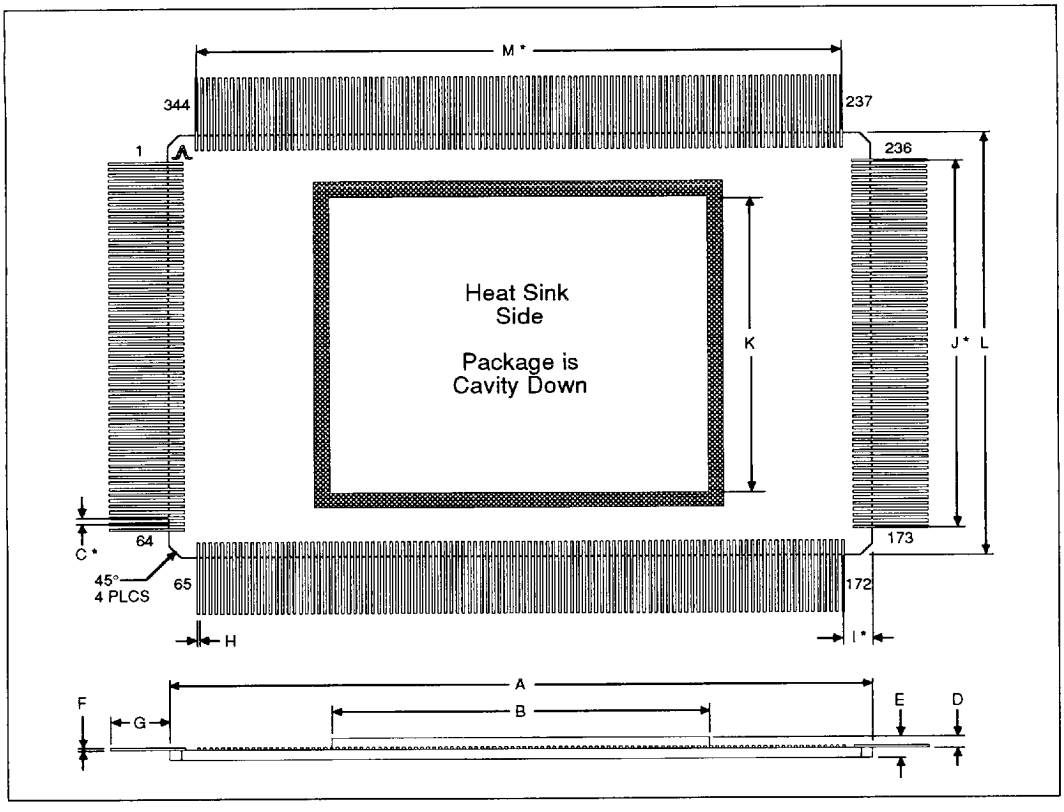
| Pin # | Name | I/O | Description |
|---|---|---|---|
| 4, 18, 33, 48, 62, 77, 91, 105, 119, 133, 147, 161, 176, 190, 205, 220, 234, 249, 263, 277, 305, 319, 333 | $V_{TT}$ | | -2V supply connection. |
| 291 | $V_{SUB}$ | | -2V supply connection to substrate (most negative supply). |
| 1, 19, 31, 46, 64-67, 70, 72, 75, 79, 82, 84, 87, 89, 94, 96, 99, 101, 106, 108, 111, 113, 116, 120, 123, 125, 128, 130, 135, 137, 140, 142, 145, 149, 152, 154, 157, 159, 164, 166, 169, 171-173, 191, 218, 226-232, 236-239, 242, 244, 247, 251, 254, 256, 259, 261, 266, 268, 271, 273, 278, 280, 283, 285, 288, 292, 295, 297, 300, 302, 307, 309, 312, 314, 317, 321, 324, 326, 329, 331, 336, 338, 341, 343, 344 | NC | | No connection |

2

## PIN IDENTIFICATION

| Name | Pin # | Name | Pin # | Name | Pin # | Name | Pin # | Name | Pin # | Name | Pin# | Name | Pin # |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_0$ | 12 | $I_{22}$ | 26 | $I_{44}$ | 41 | $D_2$ | 7 | $Z_6$ | 85 | $Z_{28}$ | 162 | $Z_{50}$ | 303 |
| $I_1$ | 225 | $I_{23}$ | 211 | $I_{45}$ | 196 | $D_3$ | 8 | $Z_7$ | 88 | $Z_{29}$ | 165 | $Z_{51}$ | 308 |
| $I_2$ | 13 | $I_{24}$ | 27 | $I_{46}$ | 42 | $D_4$ | 9 | $Z_8$ | 92 | $Z_{30}$ | 167 | $Z_{52}$ | 310 |
| $I_3$ | 224 | $I_{25}$ | 210 | $I_{47}$ | 195 | $D_5$ | 10 | $Z_9$ | 95 | $Z_{31}$ | 170 | $Z_{53}$ | 313 |
| $I_4$ | 14 | $I_{26}$ | 28 | $I_{48}$ | 43 | $A_0$ | 183 | $Z_{10}$ | 97 | $Z_{32}$ | 240 | $Z_{54}$ | 315 |
| $I_5$ | 223 | $I_{27}$ | 209 | $I_{49}$ | 194 | $A_1$ | 182 | $Z_{11}$ | 100 | $Z_{33}$ | 243 | $Z_{55}$ | 320 |
| $I_6$ | 15 | $I_{28}$ | 29 | $I_{50}$ | 44 | $A_2$ | 181 | $Z_{12}$ | 102 | $Z_{34}$ | 245 | $Z_{56}$ | 322 |
| $I_7$ | 222 | $I_{29}$ | 208 | $I_{51}$ | 193 | $A_3$ | 180 | $Z_{13}$ | 107 | $Z_{35}$ | 250 | $Z_{57}$ | 325 |
| $I_8$ | 16 | $I_{30}$ | 30 | $I_{52}$ | 45 | $A_4$ | 179 | $Z_{14}$ | 109 | $Z_{36}$ | 252 | $Z_{58}$ | 327 |
| $I_9$ | 221 | $I_{31}$ | 207 | $I_{53}$ | 192 | $A_5$ | 178 | $Z_{15}$ | 112 | $Z_{37}$ | 255 | $Z_{59}$ | 330 |
| $I_{10}$ | 20 | $I_{32}$ | 35 | $I_{54}$ | 49 | $S_0$ | 54 | $Z_{16}$ | 126 | $Z_{38}$ | 257 | $Z_{60}$ | 334 |
| $I_{11}$ | 217 | $I_{33}$ | 202 | $I_{55}$ | 188 | $S_1$ | 55 | $Z_{17}$ | 129 | $Z_{39}$ | 260 | $Z_{61}$ | 337 |
| $I_{12}$ | 21 | $I_{34}$ | 36 | $I_{56}$ | 50 | $S_2$ | 56 | $Z_{18}$ | 131 | $Z_{40}$ | 264 | $Z_{62}$ | 339 |
| $I_{13}$ | 216 | $I_{35}$ | 201 | $I_{57}$ | 187 | $S_3$ | 57 | $Z_{19}$ | 136 | $Z_{41}$ | 267 | $Z_{63}$ | 342 |
| $I_{14}$ | 22 | $I_{36}$ | 37 | $I_{58}$ | 51 | $S_4$ | 58 | $Z_{20}$ | 138 | $Z_{42}$ | 269 | $Q_0$ | 114 |
| $I_{15}$ | 215 | $I_{37}$ | 200 | $I_{59}$ | 186 | $S_5$ | 59 | $Z_{21}$ | 141 | $Z_{43}$ | 272 | $Q_1$ | 117 |
| $I_{16}$ | 23 | $I_{38}$ | 38 | $I_{60}$ | 52 | $Z_0$ | 68 | $Z_{22}$ | 143 | $Z_{44}$ | 274 | $Q_2$ | 121 |
| $I_{17}$ | 214 | $I_{39}$ | 199 | $I_{61}$ | 185 | $Z_1$ | 71 | $Z_{23}$ | 148 | $Z_{45}$ | 279 | $Q_3$ | 124 |
| $I_{18}$ | 24 | $I_{40}$ | 39 | $I_{62}$ | 53 | $Z_2$ | 73 | $Z_{24}$ | 150 | $Z_{46}$ | 281 | $Q_4$ | 286 |
| $I_{19}$ | 213 | $I_{41}$ | 198 | $I_{63}$ | 184 | $Z_3$ | 78 | $Z_{25}$ | 153 | $Z_{47}$ | 284 | $Q_5$ | 289 |
| $I_{20}$ | 25 | $I_{42}$ | 40 | $D_0$ | 5 | $Z_4$ | 80 | $Z_{26}$ | 155 | $Z_{48}$ | 298 | $Q_6$ | 293 |
| $I_{21}$ | 212 | $I_{43}$ | 197 | $D_1$ | 6 | $Z_5$ | 83 | $Z_{27}$ | 158 | $Z_{49}$ | 301 | | |

## 344 PIN CERAMIC LDCC PACKAGE DIMENSIONS




| Item | mm (Min/Max) | In (Min/Max) | Item | mm (Min/Max) | In (Min/Max) |
|---|---|---|---|---|---|
| A | 58.93/59.94 | 2.320/2.340 | H | 0.15/0.25 | 0.006/0.010 |
| B | 35.54 TYP | TYP 1.36 SQ | I* | REF 2.54 TYP | REF 0.100 TYP |
| C* | 0.51 TYP | 0.020 TYP | J* | 32.00 TYP | 1.26 TYP |
| D | 0.38/0.63 | 0.015/0.025 | K | 39.46 TYP | 1.08 TYP |
| E | 2.16/2.92 | 0.085/0.115 | L | 36.57/37.59 SQ | 1.440/1.480 |
| F | 0.09/0.216 | 0.004/0.008 | M* | 54.36 TYP | 2.140 TYP |
| G | 5.08/7.62 | 0.200/0.300 | – | – | – |

** At package body*

*NOTES:*
*1) Drawing not to scale.*
*2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating*

## ORDERING INFORMATION

The order number for this product is formed by a combination of the device number , the package type, the temperature range, and the speed grade as shown below: