MOTOROLA

Quad 2-Port Register/With Inverting And Non-Inverting Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/35001

Military 54F398

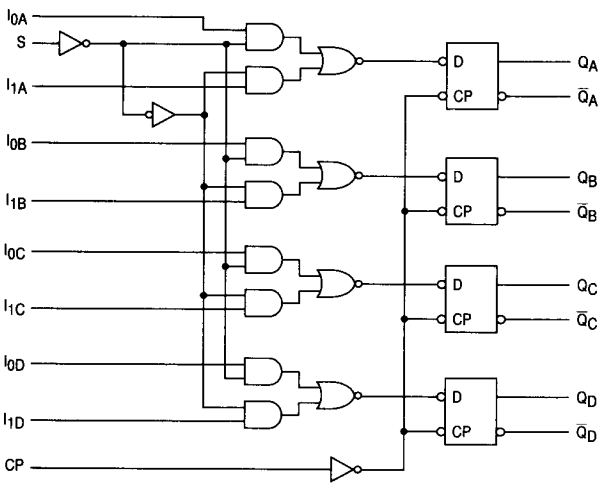
AVAILABLE AS:

1) JAN: JM38510/35001BXA
2) SMD: N/A
3) 883: 54F398/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Outputs	
S	I_0	I_1	Q	$\overline{Q}$
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
S	1	1	2	CP3
Q_A	2	2	3	V_{CC}
$\overline{Q}_A$	3	3	4	V_{CC}
I_{0A}	4	4	5	GND
I_{1A}	5	5	7	V_{CC}
I_{1B}	6	6	8	V_{CC}
I_{0B}	7	7	9	GND
$\overline{Q}_B$	8	8	10	V_{CC}
Q_B	9	9	12	V_{CC}
GND	10	10	13	GND
CP	11	11	14	CP1
Q_C	12	12	15	V_{CC}
$\overline{Q}_C$	13	13	17	V_{CC}
I_{0C}	14	14	18	GND
I_{1C}	15	15	19	V_{CC}
I_{1D}	16	16	20	V_{CC}
I_{0D}	17	17	17	GND
$\overline{Q}_D$	18	18	18	V_{CC}
Q_D	19	19	19	V_{CC}
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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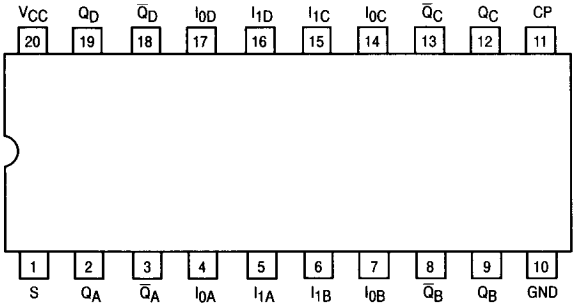
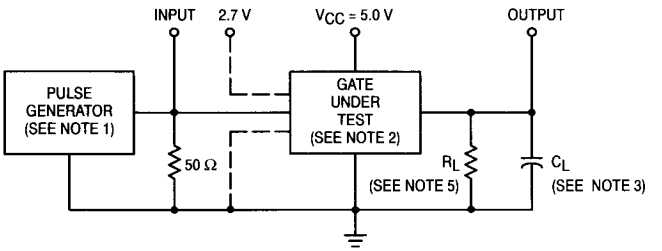
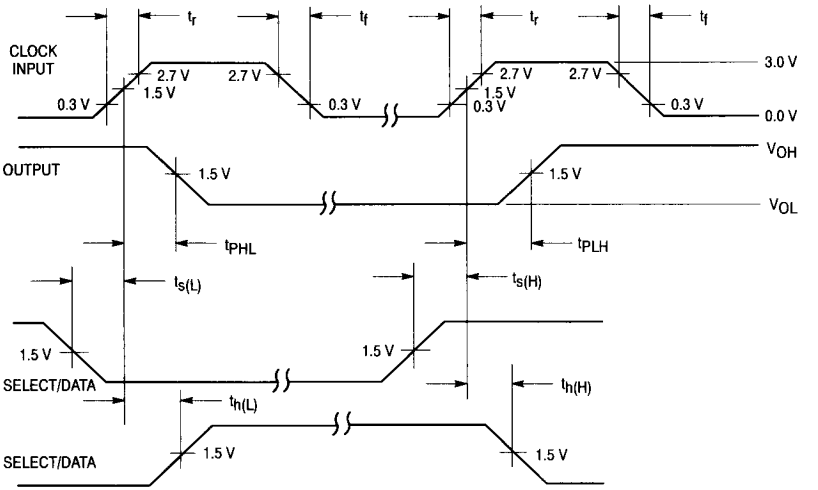
LOGIC DIAGRAM



TEST CIRCUIT AND WAVEFORM

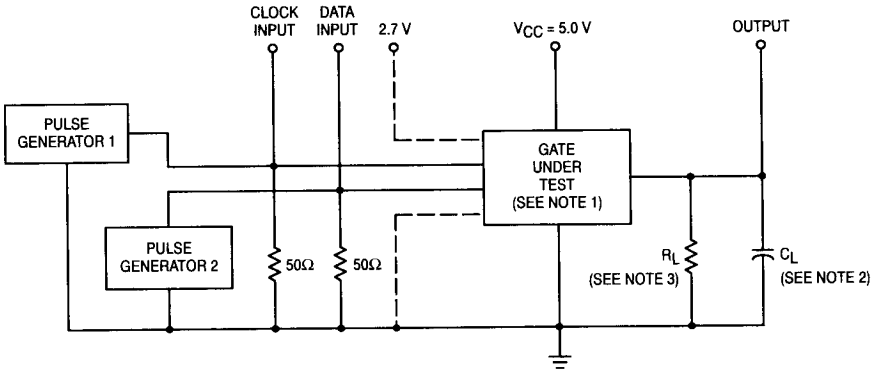


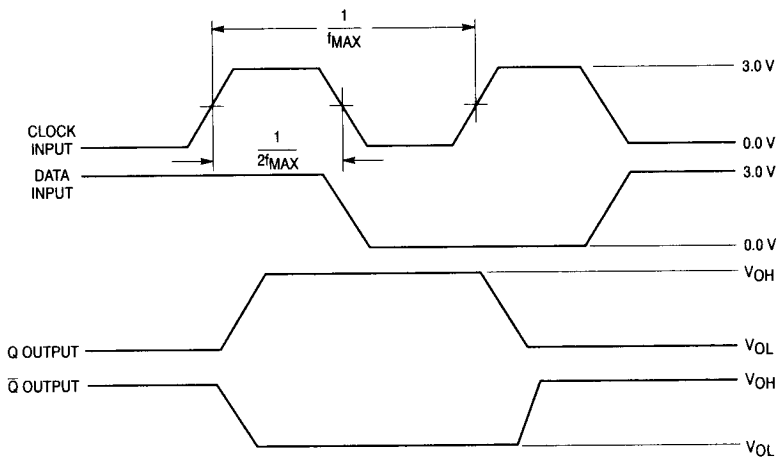


NOTES:

1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high $\geq$ 2.0 V, low $\leq$ 0.8 V, or open).
3. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. R_L = 500 Ω ± 5.0%.

TEST CIRCUIT AND WAVEFORM





NOTES:
1. Terminal conditions (pins may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
2. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance, without package in test fixture.
3. R_L = 500 Ω ± 5.0%.
4. f_{MAX} output is 1/2 of the input frequency.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V or 5.5 V, V_{IL} = 0.8 V, S = 0.8 V or 2.0 V, CP = (See Note 1).
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OH} = 20 mA, V_{IH} = 2.0 V or 5.5 V, V_{IL} = 0.8 V, S = 0.8 V or 2.0 V, CP = (See Note 1).
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, (other inputs are open), S = 0 V or (2.7 V).
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, (other inputs are open), S = 0 V or (7.0 V).
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open, V_{OUT} = 0 V, CP = (See Note 1).
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open, S = 0 V, 5.5 V, or (0.5 V).
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, V_{IN} = 0 V, CP = (See Note 1), V_{out} = 2.5 V.
I_{CC}	Power Supply Current Off		38		38		38	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), CP = (See Note 1).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**), V_{CC} = 5.5 V, V_{INL} = 0.5 V, V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output High-Low	1.5	9.5	1.5	11.5	1.5	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH1}	Propagation Delay /Data-Output Low-High	1.5	7.5	1.5	9.5	1.5	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
f_{MAX}	Maximum Clock Frequency	100		80		80		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.

NOTES:
1. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to CP then make measurements.