REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27						
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thanh V. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess	
	APPROVED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, CMOS, 32-BIT RISC MICROPROCESSOR, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 98-04-22	
	REVISION LEVEL	SIZE **A** / CAGE CODE **67268** / **5962-97608**
		SHEET 1 OF 27

DSCC FORM 2233
APR 97

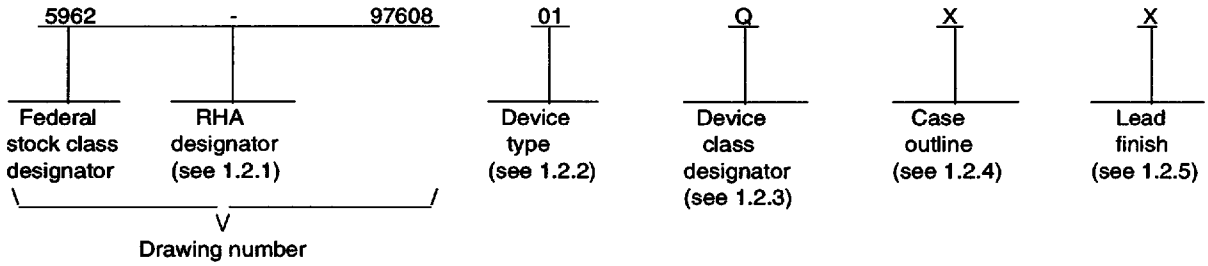
5962-E046-98

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	PC603E-80	32-bit RISC microprocessor
02	PC603E-100	32-bit RISC microprocessor
03	PC603E-120	32-bit RISC microprocessor
04	PC603E-133	32-bit RISC microprocessor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	240	Ceramic leaded chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +4.0 V dc
DC input voltage range (V_{IN})	-0.3 V dc to +5.5 V dc
Maximum power dissipation at (P_D)	5.3 W
Storage temperature range (T_{STG})	-55°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	2.2°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+3.135 V dc to +3.465 V dc
Logic high input voltage range (V_{IH})	2.4 V dc to 5.5 V dc
Logic low input voltage range (V_{IL})	GND to 0.8 V dc
System clock input high voltage (CV_{IH})	2.4 V dc to 5.5 V dc
System clock input low voltage (CV_{IL})	GND to 0.4 V dc
Minimum high level output voltage (V_{OH})	2.4 V dc
Maximum low level output voltage (V_{OL})	0.4 V dc
Frequency of operation (f_{OP}):	
Device type 01	80 MHz
Device type 02	100 MHz
Device type 03	120 MHz
Device type 04	133 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Maximum operating junction temperature (T_J)	+137°C
Minimum operating case temperature (T_C)	-55°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are tose listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documentrs cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timimg waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance interface. The boundary-scan interface of the device is a fully compliant implementation of the IEEE 1149.1 standard.

3.11.1 Test access port. The device has five dedicated JTAG signals which are described in the following table. The TDI and TDO scan ports are used to scan instructions as well as data into the various scan registers for JTAG operations. The scan operation is controlled by the test access port (TAP) controller which in turn is controlled by the TMS input sequence. The scan data is latched in at the rising edge of TCK.

IEEE interface pin descriptions

Signal name	Input/Output	Weak pullup provided	IEEE 1149.1 function
TDI	Input	Yes	Serial scan input signal
TDO	Output	No	Serial scan output signal
TMS	Input	Yes	TAP controller mode signal
TCK	Input	Yes	Scan clock
$\overline{\text{TRST}}$	Input	Yes	TAP controller reset

$\overline{\text{TRST}}$ is a JTAG optional signal which is used to reset the TAP controller asynchronously. The $\overline{\text{TRST}}$ signal assures that the JTAG logic does not interfere with the normal operation of the chip, and can be asserted coincident with the $\overline{\text{HRESET}}$.

3.11.2 TAP controller. The TAP (Tap Access Port) controller is a state machine that controls the JTAG scan protocol. The TAP controller implements 16 states specified by the IEEE 1149.1 specification. The TAP controller state machine is clocked by TCK and the state transitions are controlled by the TMS input.

3.11.3 JTAG instructions. The device supports the three required JTAG instructions: BYPASS, SAMPLE/PRELOAD, and EXTEST which are controlled by an 8-bit instruction register. These instructions are scanned in serially (LSB first) via the TDI pin. The table of the JTAG instructions for the device is given below.

JTAG instructions

Instruction	Encoding	Test data register accessed
BYPASS	11111111	Bypass register
SAMPLE/PRELOAD	11000000	Boundary-scan register
EXTEST	00000000	Boundary-scan register

The BYPASS instruction. The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path between the TDI and the TDO pins of a component when no test operation of that component is required. This allows more rapid movement of test data to and from other components on a board that are required to perform test operations.

The SAMPLE/PRELOAD instruction. The mandatory SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register prior to selection of the other boundary-scan test instructions.

The EXTEST instruction. The mandatory EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.

NOTE: Following use of the EXTEST instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., nontest) operation.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions -55°C ≤ Tc ≤ +125°C +3.135 V ≤ Vcc ≤ +3.465 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input high voltage (all inputs except SYSCLK)	V_{IH}		All	1,2,3	2.4	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}		All	1,2,3	0.0	0.8	
SYSCLK input high voltage	CV_{IH}		All	1,2,3	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}		All	1,2,3	0.0	0.4	
Output high voltage	V_{OH}	I_{OH} = -9 mA	All	1,2,3	2.4		V
Output low voltage	V_{OL}	I_{OL} = 14 mA	All	1,2,3		0.4	
Input leakage current 1/	I_{IN}	V_{IN} = 3.465 V	All	1,2,3		10	µA
		V_{IN} = 5.5 V	All	1,2,3		245	
High-Z (off-state) leakage current 1/	I_{TSI}	V_{IN} = 3.465 V	All	1,2,3		10	µA
		V_{IN} = 5.5 V	All	1,2,3		245	
Input capacitance (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{IN1}	V_{IN} = 0.0 V, f = 1 MHz See 4.4.1c	All	4		10.0	pF
Input capacitance (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{IN2}	V_{IN} = 0.0 V, f = 1 MHz See 4.4.1c	All	4		15.0	pF
Functional test		See 4.4.1b	All	7,8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions -55°C ≤ Tc ≤ +125°C +3.135 V ≤ Vcc ≤ +3.465 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Clock AC timing specifications							
Processor frequency		2/	01	9,10,11	40	80	MHz
			02		50	100	
			03		60	120	
			04		60	133.3	
VCO frequency		2/	01	9,10,11	80	200	MHz
			02		100	200	
			03		120	240	
			04		133.3	266.6	
SYSCLK (bus) frequency			All	9,10,11	16.67	66.67	MHz
SYSCLK cycle time	1		All	9,10,11	15.0	60.0	ns
SYSCLK rise and fall time	2,3	3/	All	9,10,11		2.0	ns
SYSCLK duty cycle measured at 1.4 V	4	4/	All	9,10,11	40.0	60.0	%
SYSCLK jitter	8	5/	All	9,10,11		±150	ps
Device internal PLL relock time	9	4/ 6/	All	9,10,11		100	µs
Input AC timing specifications 7/							
Address/data/transfer attribute inputs valid to SYSCLK (input setup)	10a	8/	All	9,10,11	4.0		ns
All other inputs valid to SYSCLK (input setup)	10b	9/	All	9,10,11	5.0		ns
Mode select inputs valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$)	10c	10/ 11/ 12/ 13/	All	9,10,11	8 x t_{SYS}		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions -55°C ≤ Tc ≤ +125°C +3.135 V ≤ Vcc ≤ +3.465 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input AC timing specifications - Continued 7/							
SYSCLK to address/ data/transfer attribute inputs invalid (input hold)	11a	8/	All	9,10,11	1.0		ns
SYSCLK to all other inputs invalid (input hold)	11b	9/	All	9,10,11	1.0		ns
$\overline{\text{HRESET}}$ to mode select inputs invalid (input hold) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$)	11c	10/ 12/ 13/	All	9,10,11	0.0		ns
Output AC timing specifications 14/ 15/							
SYSCLK to output driven (output enable time)	12	C_L = 50 pF	All	9,10,11	1.0		ns
SYSCLK to output valid (5.5 V to 0.8 V - $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	13a	C_L = 50 pF 16/	All	9,10,11		11.0	ns
SYSCLK to output valid ($\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	13b	C_L = 50 pF 17/	All	9,10,11		10.0	ns
SYSCLK to output valid (5.5 V to 0.8 V - all except $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	14a	C_L = 50 pF 16/	All	9,10,11		13.0	ns
SYSCLK to output valid (all except $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	14b	C_L = 50 pF 17/	All	9,10,11		11.0	ns
SYSCLK to output invalid (output hold)	15	C_L = 50 pF 18/	All	9,10,11	0.5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions -55°C ≤ Tc ≤ +125°C +3.135 V ≤ Vcc ≤ +3.465 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output AC timing specifications - Continued 14/ 15/							
SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	16	C_L = 50 pF	All	9,10,11		9.5	ns
SYSCLK to $\overline{ABB}$, $\overline{DBB}$ high impedance after precharge	17	C_L = 50 pF 19/ 20/	All	9,10,11		1.2	t_{sys}
SYSCLK to $\overline{ARTRY}$ high impedance before precharge	18	C_L = 50 pF	All	9,10,11		9.0	ns
SYSCLK to $\overline{ARTRY}$ precharge enable	19	C_L = 50 pF 18/ 19/ 21/	All	9,10,11	0.2 t_{sys} + 1.0		ns
Maximum delay to $\overline{ARTRY}$ precharge	20	C_L = 50 pF 19/ 21/	All	9,10,11		1.2	t_{sys}
SYSCLK to $\overline{ARTRY}$ high impedance after precharge	21	C_L = 50 pF 19/ 21/	All	9,10,11		2.25	t_{sys}
JTAG AC timing specifications (independent of SYSCLK)							
TCK frequency of operation		C_L = 50 pF	All	9,10,11	0.0	16.0	MHz
TCK cycle time	22	C_L = 50 pF	All	9,10,11	62.5		ns
TCK clock pulse width measured at 1.4 V	23	C_L = 50 pF	All	9,10,11	25.0		ns
TCK rise and fall times	24	C_L = 50 pF	All	9,10,11	0.0	3.0	ns
$\overline{TRST}$ setup time to TCK rising edge	25	C_L = 50 pF 22/	All	9,10,11	13.0		ns
$\overline{TRST}$ assert time	26	C_L = 50 pF	All	9,10,11	40.0		ns
Boundary scan input data setup time	27	C_L = 50 pF 23/	All	9,10,11	6.0		ns
Boundary scan input data hold time	28	C_L = 50 pF 23/	All	9,10,11	27.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions -55°C ≤ Tc ≤ +125°C +3.135 V ≤ Vcc ≤ +3.465 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
JTAG AC timing specifications (independent of SYSCLK) - Continued							
TCK to output data valid	29	C_L = 50 pF 24/	All	9,10,11	4.0	25.0	ns
TCK to output high impedance	30	C_L = 50 pF 24/	All	9,10,11	3.0	24.0	ns
TMS, TDI data setup time	31	C_L = 50 pF	All	9,10,11	0.0		ns
TMS, TDI data hold time	32	C_L = 50 pF	All	9,10,11	25.0		ns
TCK to TDO data valid	33	C_L = 50 pF	All	9,10,11	4.0	24.0	ns
TCK to TDO high impedance	34	C_L = 50 pF	All	9,10,11	3.0	15.0	ns

1/ Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2/ Caution: The SYSCLK frequency and PLL_CFG0-PLL_CFG3 settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
3/ Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4V.
4/ Timing is guaranteed by design and characterization, and is not tested.
5/ Cycle-to-cycle jitter, and is guaranteed by design.
6/ PLL relock time is the maximum amount of time required for PLL lock after a stable Vcc and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled duting sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
7/ All inputs specifications are measured from the TTL level (0.8 V or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin.
8/ Address/data/transfer attribute input signals are composed of the following: A0-A3, AP0-AP3, TT0-TT4, TC0-TC1, $\overline{\text{TBST}}$, TSIZ0-TSIZ2, $\overline{\text{GBL}}$, DH0-DH31, DL0-DL31, DP0-DP7.
9/ All other input signals are composed of the following: $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
10/ The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
11/ t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds.
12/ These values are guaranteed by design, and are not tested.
13/ This specification is for configuration mode only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
14/ All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin.
15/ All maximum timing specifications assume C_L = 50 pF.
16/ SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vcc to 0.8 V (5.0 V CMOS levels instead of 3.3 V CMOS levels).
17/ Output signal transitions from GND to 2.0 V or Vcc to 0.8 V.
18/ This minimum timing parameter assumes C_L = 0 pF.

TABLE I. Electrical performance characteristics - Continued.

19/ t_{sys} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
20/ Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.
21/ Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.
22/ $\overline{TRST}$ is an asynchronous signal. The setup time is for test purposes only.
23/ Non-test signal input timing with respect to TCK.
24/ Non-test signal output timing with respect to TCK.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

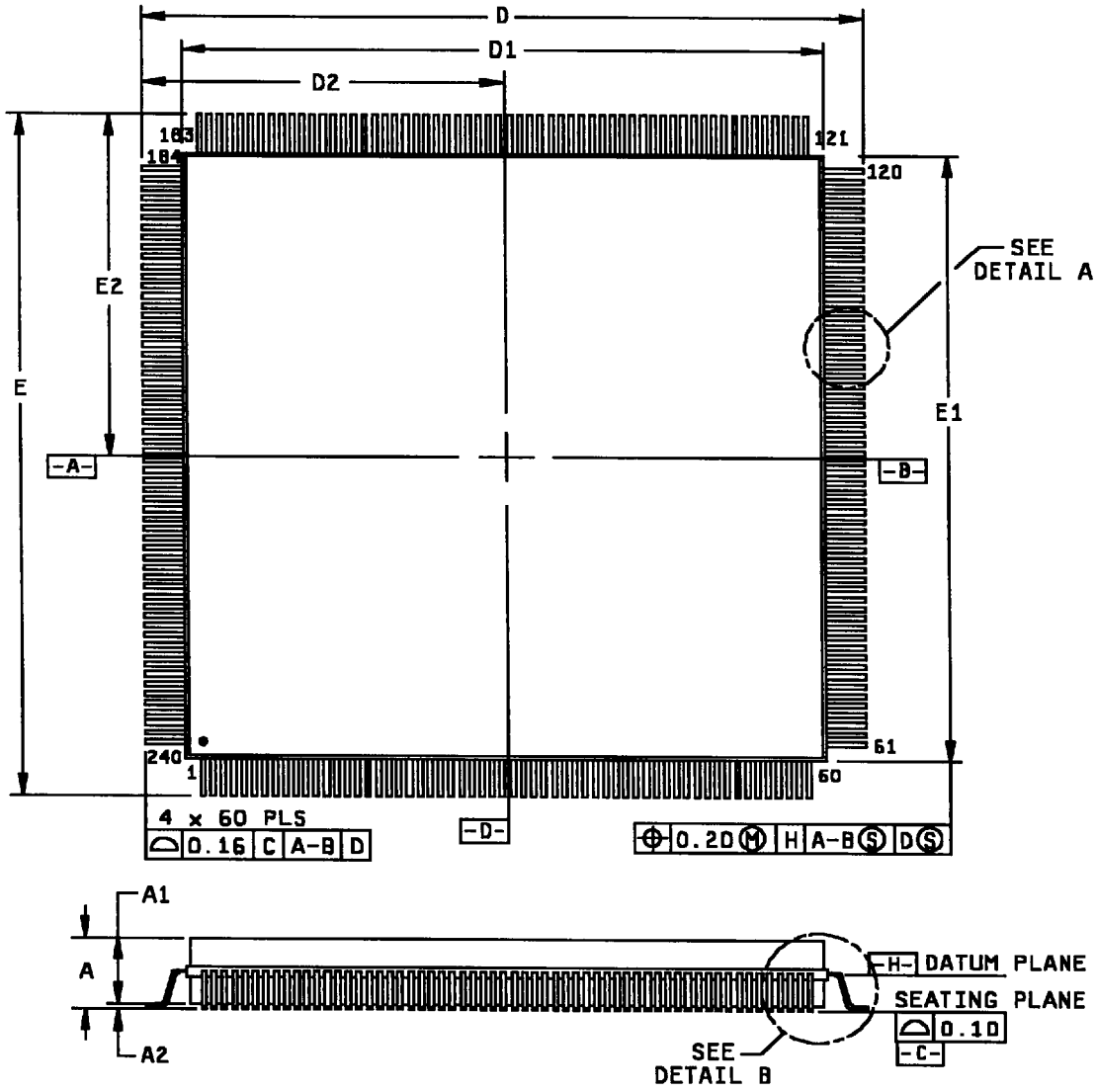
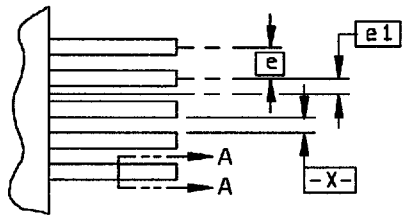


FIGURE 1. Case outline.

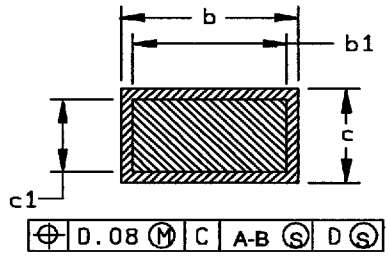
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97608
		REVISION LEVEL	SHEET 13

DSCC FORM 2234
APR 97

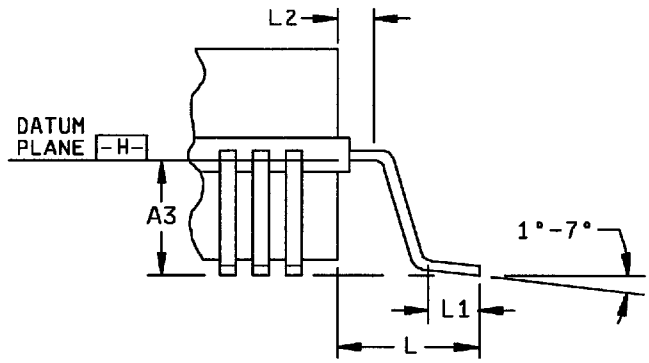
9004708 0035940 687



DETAIL A



SECTION A-A
240 PLS



DETAIL B

FIGURE 1. Case outline - Continued.

Symbol	Millimeters	
	Min	Max
A	3.67	4.15
A1	3.10	3.90
A2	0.25	0.75
A3	2.025	2.175
b	0.185	0.270
b1	0.175	0.225
c	0.130	0.175
c1	0.122	0.132
D	34.41	34.75
D1	30.86	31.75
D2	17.20	17.40
e	0.50 BSC	
e1	0.25 BSC	
E	34.41	34.75
E1	30.86	31.75
E2	17.20	17.40
L	1.80 REF	
L1	0.45	0.55
L2	0.95 REF	

FIGURE 1. Case outline - Continued.

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	$\overline{GBL}$	31	$\overline{QREQ}$	61	OV_{CC}	91	DH12
2	A1	32	$\overline{ARTRY}$	62	DL29	92	DH11
3	A3	33	OGND	63	DL30	93	DH10
4	V_{CC}	34	V_{CC}	64	DL31	94	DH9
5	A5	35	OV_{CC}	65	GND	95	OGND
6	A7	36	$\overline{ABB}$	66	DH31	96	OV_{CC}
7	A9	37	A31	67	DH30	97	DH8
8	OGND	38	DP0	68	DH29	98	DH7
9	GND	39	GND	69	OGND	99	DH6
10	OV_{CC}	40	DP1	70	OV_{CC}	100	DL22
11	A11	41	DP2	71	DH28	101	DL21
12	A13	42	DP3	72	DH27	102	DL20
13	A15	43	OGND	73	DH26	103	OGND
14	V_{CC}	44	V_{CC}	74	DH25	104	OV_{CC}
15	A17	45	OV_{CC}	75	DH24	105	DL19
16	A19	46	DP4	76	DH23	106	DL18
17	A21	47	DP5	77	OGND	107	DL17
18	OGND	48	DP6	78	DH22	108	DH5
19	GND	49	GND	79	OV_{CC}	109	DH4
20	OV_{CC}	50	DP7	80	DH21	110	DH3
21	A23	51	DL23	81	DH20	111	OGND
22	A25	52	DL24	82	DH19	112	OV_{CC}
23	A27	53	OGND	83	DH18	113	DH2
24	V_{CC}	54	OV_{CC}	84	DH17	114	DH1
25	$\overline{DBWO}$	55	DL25	85	DH16	115	DH0
26	$\overline{DBG}$	56	DL26	86	OGND	116	GND
27	$\overline{BG}$	57	DL27	87	DH15	117	DL16
28	$\overline{AACK}$	58	DL28	88	OV_{CC}	118	DL15
29	GND	59	V_{CC}	89	DH14	119	DL14
30	A29	60	OGND	90	DH13	120	OGND

FIGURE 2. Terminal connections.

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
121	OV_{CC}	151	A28	181	OGND	211	PLL_CFG1
122	V_{CC}	152	GND	182	GND	212	SYSCLK
123	DL13	153	$\overline{DBDIS}$	183	OV_{CC}	213	PLL_CFG0
124	DL12	154	$\overline{TEA}$	184	TT3	214	$\overline{HRESET}$
125	DL11	155	$\overline{TA}$	185	TT2	215	$\overline{CKSTP\_IN}$
126	DL10	156	$\overline{DRTRY}$	186	$\overline{MCP}$	216	$\overline{CKSTP\_OUT}$
127	OGND	157	V_{CC}	187	$\overline{SMI}$	217	$\overline{DPE}$
128	OV_{CC}	158	A26	188	$\overline{INT}$	218	$\overline{APE}$
129	DL9	159	A24	189	$\overline{SRESET}$	219	$\overline{BR}$
130	DL8	160	A22	190	TT1	220	OGND
131	DL7	161	OGND	191	TT0	221	CLK_OUT
132	GND	162	GND	192	$\overline{TBST}$	222	OV_{CC}
133	DL6	163	OV_{CC}	193	OGND	223	TC1
134	DL5	164	A20	194	OV_{CC}	224	TC0
135	DL4	165	A18	195	TSIZ2	225	CSE0
136	OGND	166	A16	196	TSIZ1	226	AP3
137	V_{CC}	167	V_{CC}	197	TSIZ0	227	AP2
138	OV_{CC}	168	A14	198	TDO	228	OGND
139	DL3	169	A12	199	TDI	229	OV_{CC}
140	DL2	170	A10	200	TMS	230	AP1
141	DL1	171	OGND	201	TCK	231	AP0
142	GND	172	GND	202	$\overline{TRST}$	232	$\overline{RSRV}$
143	DL0	173	OV_{CC}	203	L2_TSTCLK	233	$\overline{TLBISYNC}$
144	A30	174	A8	204	L1_TSTCLK	234	TBEN
145	$\overline{DBB}$	175	A6	205	$\overline{LSSD\_MODE}$	235	$\overline{QACK}$
146	OGND	176	A4	206	GND	236	$\overline{WT}$
147	V_{CC}	177	V_{CC}	207	V_{CC}	237	$\overline{CI}$
148	OV_{CC}	178	A2	208	PLL_CFG3	238	OGND
149	$\overline{TS}$	179	A0	209	AV_{CC}	239	GND
150	CSE1	180	TT4	210	PLL_CFG2	240	OV_{CC}

FIGURE 2. Terminal connections - Continued.

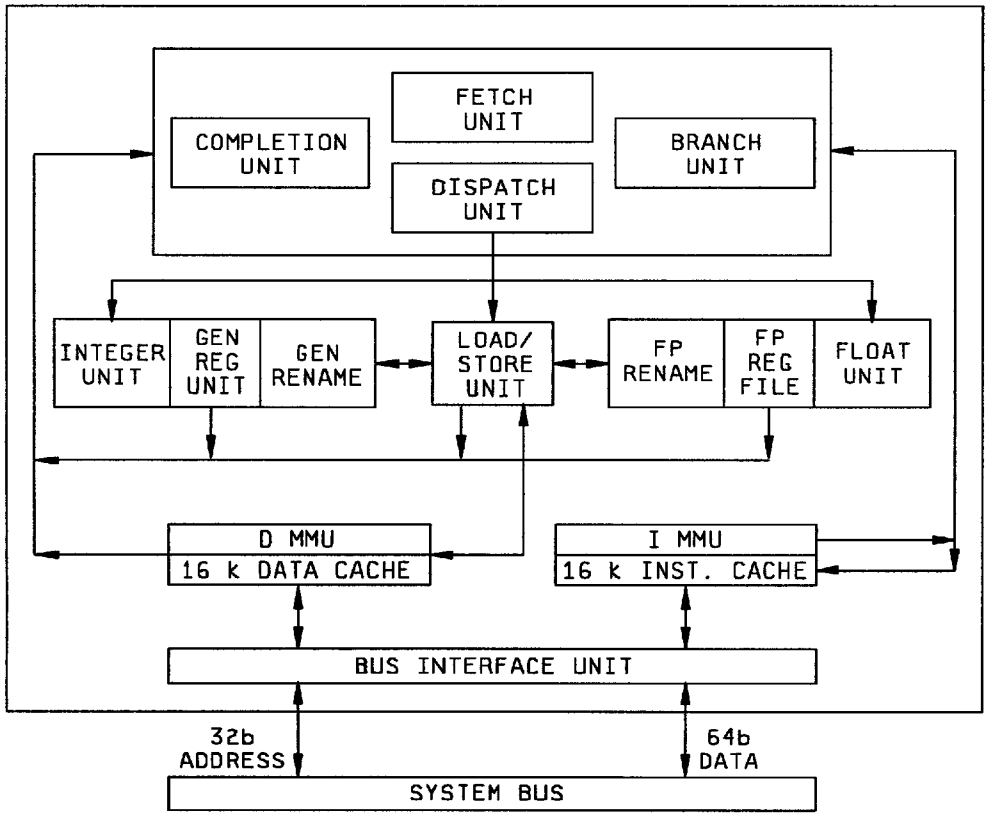
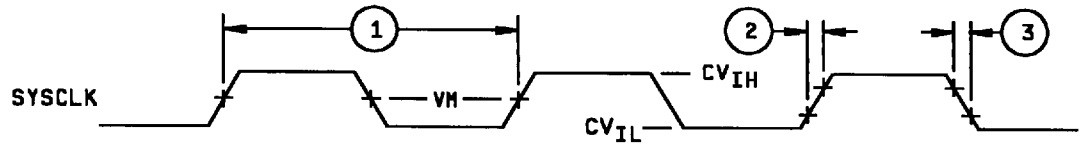
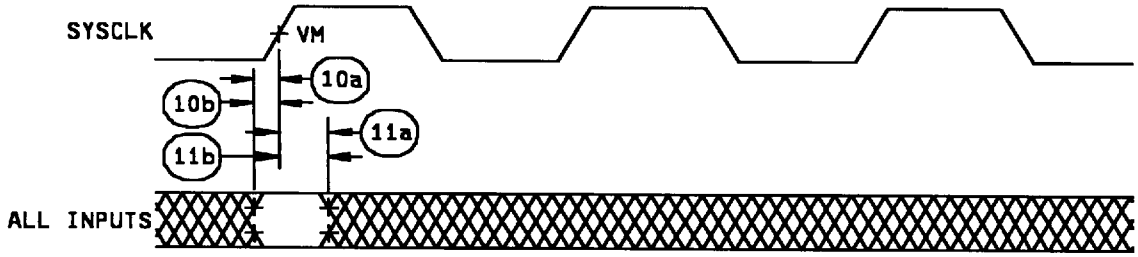


FIGURE 3. Block diagram.

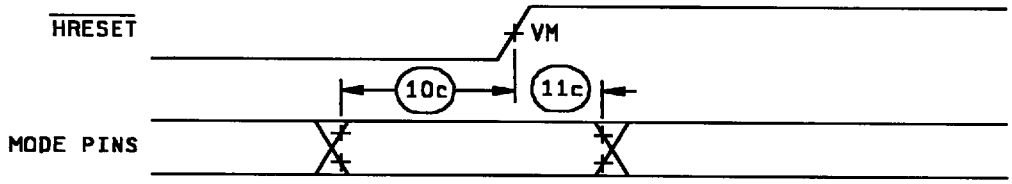
SYSCLK INPUT TIMING DIAGRAM



INPUT TIMING DIAGRAM



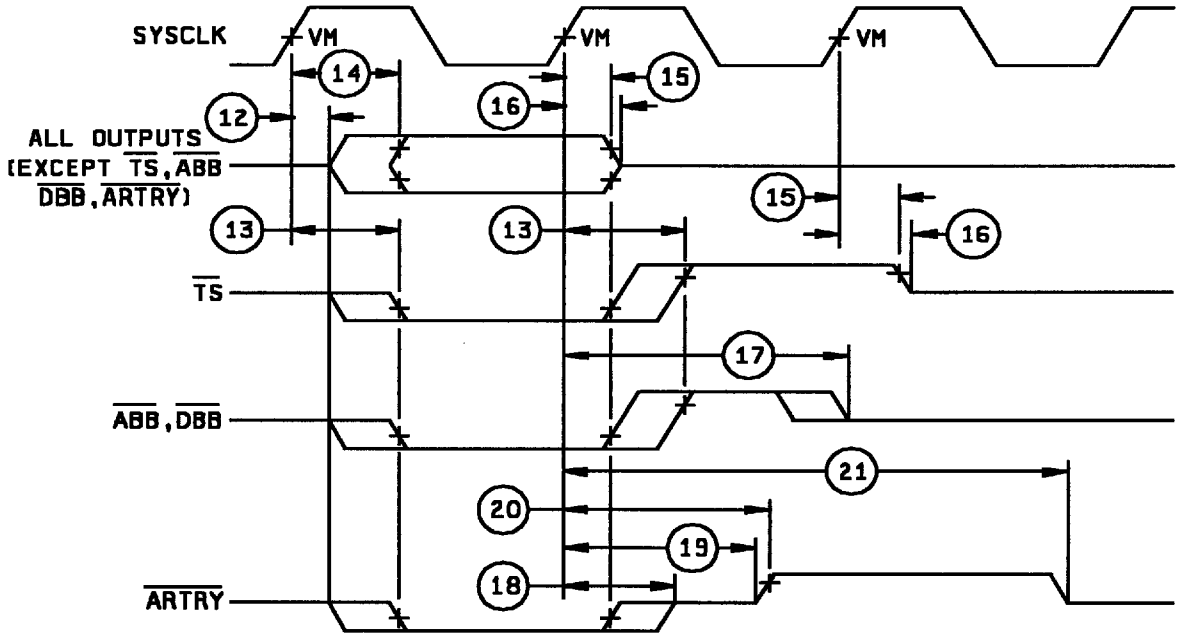
MODE SELECT INPUT TIMING DIAGRAM



NOTE: VM = 1.4 V.

FIGURE 4. Timing waveforms.

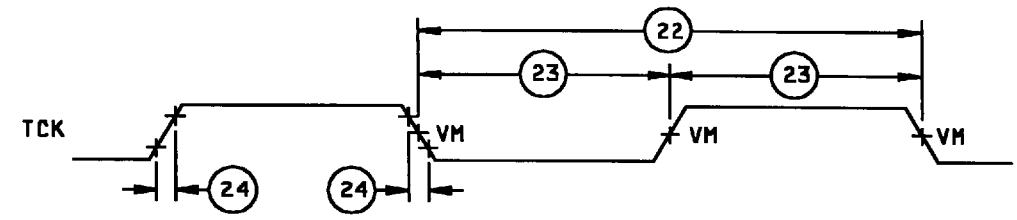
Output timing diagram



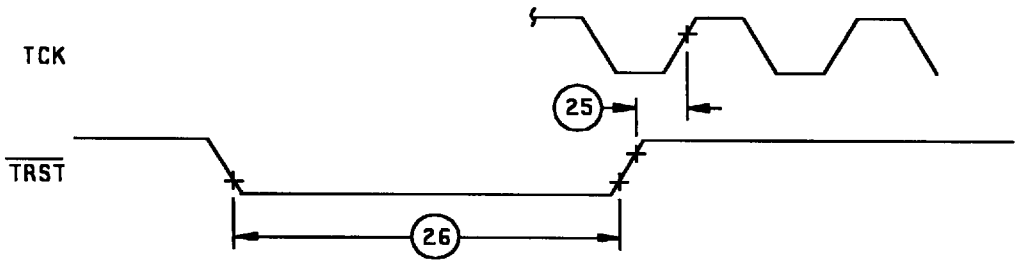
NOTE: VM = 1.4 V.

FIGURE 4. Timing waveforms - Continued.

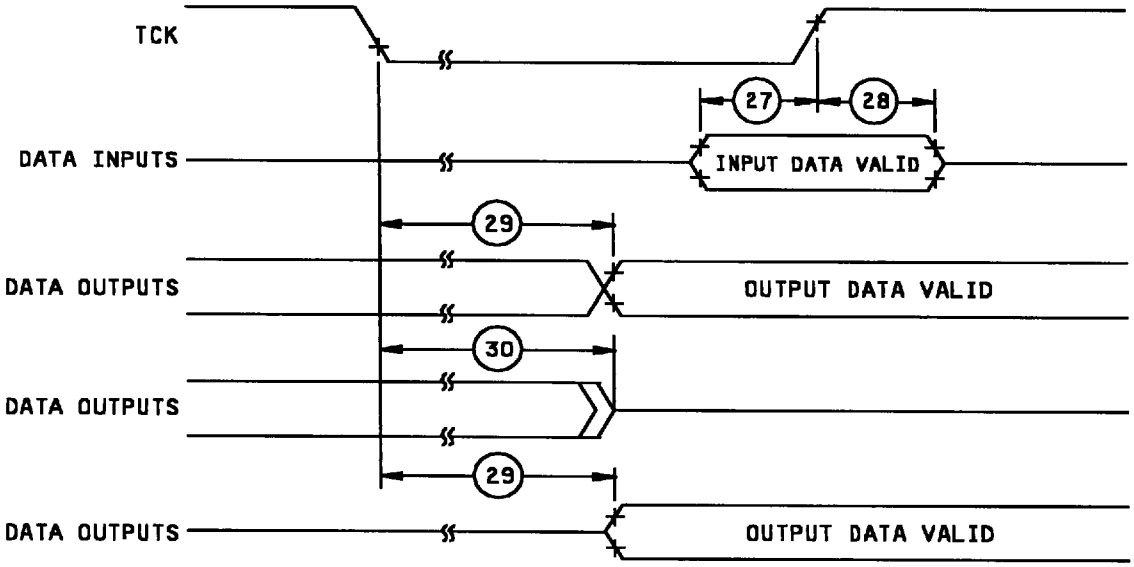
CLOCK INPUT TIMING DIAGRAM



$\overline{\text{TRST}}$ TIMING DIAGRAM



BOUNDRY-SCAN TIMING DIAGRAM



NOTE: VM = 1.4 V.

FIGURE 4. Timing waveforms - Continued.

TEST ACCESS PORT TIMING DIAGRAM

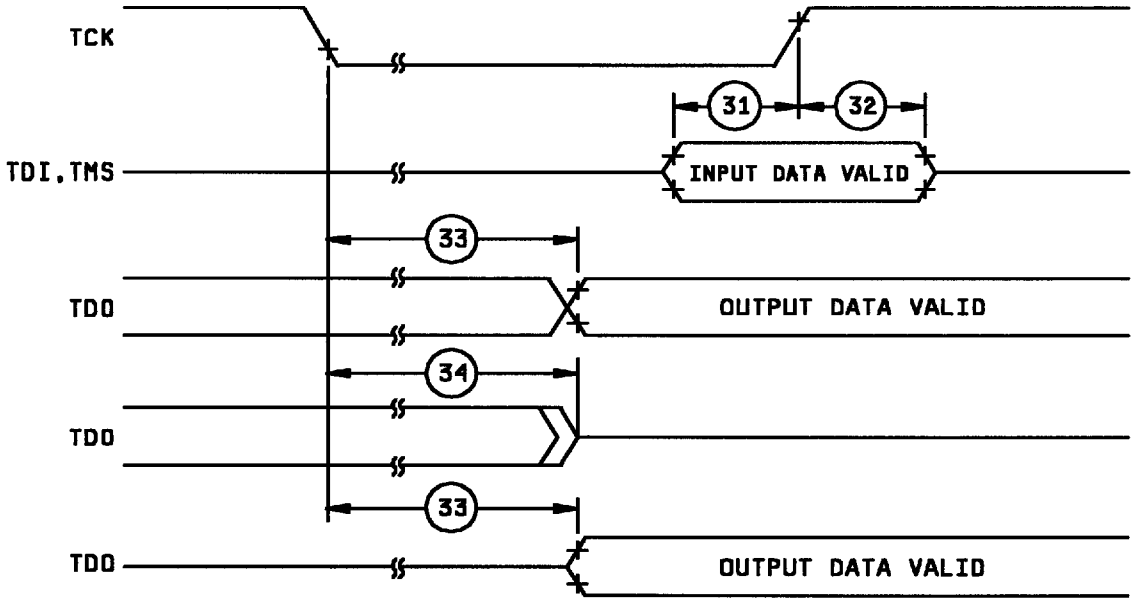


FIGURE 4. Timing waveforms - Continued.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25° C ±5° C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

TABLE III. Pin description.

Symbol	Signal name	Signal function
A0-A31	Address Bus	
$\overline{\text{AACK}}$	Address Acknowledge	The address phase of a transaction is complete
$\overline{\text{ABB}}$	Address Bus Busy	If output, the device is the address bus master. If input, the address bus is in use
AP0-AP3	Address Bus Parity	If output, represents odd parity for each of 4 bytes of the physical address for a transaction. If input, represents odd parity for each of 4 bytes of the physical address for snooping operations
$\overline{\text{APE}}$	Address Parity Error	Incorrect address bus parity detected on a snoop
$\overline{\text{ARTRY}}$	Address Retry	If output, detects a condition in which a snooped address tenure must be retried. If input, must retry the preceding address tenure
$\overline{\text{BG}}$	Bus Grant	May, with the proper qualification, assume mastership of the address bus
$\overline{\text{BR}}$	Bus Request	Request mastership of the address bus
$\overline{\text{CI}}$	Cache Inhibit	A single-beat transfer will not be cached
CLK_OUT	Test Clock	Provides PLL clock output for PLL testing and monitoring
$\overline{\text{CKSTP\_IN}}$	Checkstop Input	Must terminate operation by internally gating off all clocks, and release all outputs
$\overline{\text{CKSTP\_OUT}}$	Checkstop Output	Has detected a checkstop condition and has ceased operation
CSE0-CSE1	Cache Set Entry	Cache replacement set element for the current transaction reloading into or writing out of the cache
$\overline{\text{DBB}}$	Data Bus Busy	If output, the device is the data bus master. If input, another device is bus master
$\overline{\text{DBDIS}}$	Data Bus Disable	(For a write transaction) must release data bus and the data bus parity to high impedance during the following cycle
$\overline{\text{DBG}}$	Data Bus Grant	May, with the proper qualification, assume mastership of the data bus
$\overline{\text{DBWO}}$	Data Bus Write Only	May run the data bus tenure
DH0-DH31	Data Bus	
DL0-DL31	Data Bus	
DP0-DP7	Data Bus Parity	If output, odd parity for each of 8 bytes of data write transactions. If input, odd parity for each byte of read data
$\overline{\text{DPE}}$	Data Parity Error	Incorrect data bus parity
$\overline{\text{DRTRY}}$	Data Retry	Must invalidate the data from the previous read operation
$\overline{\text{GBL}}$	Global	If output, a transaction is global. If input, a transaction must be snooped by the device
$\overline{\text{HRESET}}$	Hard Reset	Initiates a complete hard reset operation

TABLE III. Pin description - Continued.

Symbol	Signal name	Signal function
$\overline{INT}$	Interrupt	Initiates an interrupt if bit EE of MSR register is set
$\overline{LSSD\_MODE}$		LSSD test control signal for factory use only
L1_TSTCLK		LSSD test control signal for factory use only
L2_TSTCLK		LSSD test control signal for factory use only
$\overline{MCP}$	Machine Check Interrupt	Initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set
PLL_CFG0-PLL_CFG3	PLL Configuration	Configures the operation of the PLL and the internal processor clock frequency
$\overline{QACK}$	Quiescent Acknowledge	All bus activity has terminated and the device may enter a quiescent (or low power) state
$\overline{QREQ}$	Quiescent Request	Is requesting all bus activity normally to enter a quiescent (low power) state
$\overline{RSRV}$	Reservation	Represents the state of the reservation coherency bit in the reservation address register
$\overline{SMI}$	System Management Interrupt	Initiates a system management interrupt operation if the bit EE of MSR register is set
$\overline{SRESET}$	Soft Reset	Initiates processing for a reset exception
SYSCLK	System Clock	Represents the primary clock input for the device, and the bus clock frequency for device bus operation
$\overline{TA}$	Transfer Acknowledge	A single-beat data transfer completed successfully or a data beat in a burst transfer completed successfully
TBEN	Timebase Enable	The timebase should continue clocking
$\overline{TBST}$	Transfer Burst	If output, a burst transfer is in progress. If input, when snooping for single-beat reads
TC0-TC1	Transfer Code	Special encoding for the transfer in progress
TCK	Test Clock	Clock signal for the IEEE P1149.1 test access port (TAP)
TDI	Test Data Input	Serial data input for the TAP
TDO	Test Data Output	Serial data output for the TAP
$\overline{TEA}$	Transfer Error Acknowledge	A bus error occurred
$\overline{TLBISYNC}$	TLBI Sync	Instruction execution should stop after execution of a **tlbsync** instruction
TMS	Test Mode Select	Selects the principal operation of the test-support circuitry
$\overline{TRST}$	Test Reset	Provides an asynchronous reset of the TAP controller
TSIZ0-TSIZ2	Transfer Size	For memory accesses, these signals along with $\overline{TBST}$ indicate the data transfer size for the current bus operation

TABLE III. Pin description - Continued.

Symbol	Signal name	Signal function
$\overline{TS}$	Transfer Start	If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid. If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$)
TT0-TT4	Transfer Type	Type of transfer in progress
$\overline{WT}$	Write-Through	A single-beat transaction is write-through

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-04-22

Approved sources of supply for SMD 5962-97608 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9760801QXA	18778	TSPC603EMAB/C2L
5962-9760802QXA	18778	TSPC603EMAB/C3L
5962-9760803QXA	18778	TSPC603EMAB/C4L
5962-9760804QXA	18778	TSPC603EMAB/C5L

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18778	Thomson Components and Tubes Corporation 40G Commerce Way Totowa, NJ 07511

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.