



# STS5N150

## N-CHANNEL 150V - 0.045 $\Omega$ - 5A SO-8 LOW GATE CHARGE STripFET™ POWER MOSFET

TARGET DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS5N150	150 V	<0.06 $\Omega$	5 A

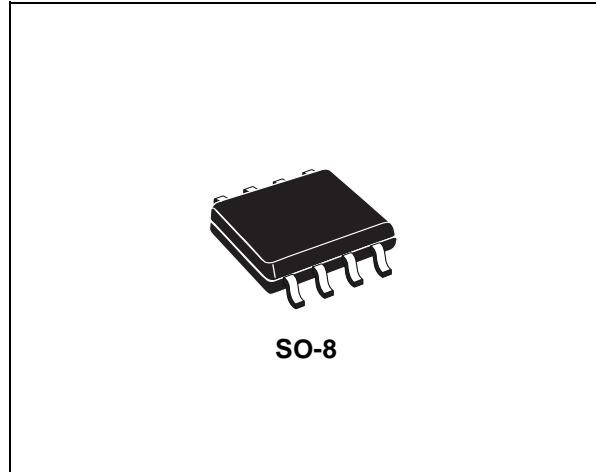
- TYPICAL R<sub>DS(on)</sub> = 0.045  $\Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- EXTREMELY LOW GATE CHARGE

### DESCRIPTION

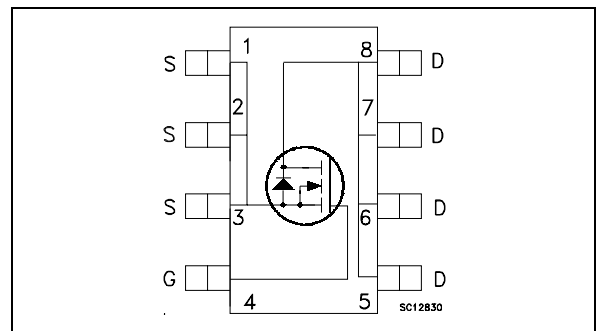
This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

### APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL



### INTERNAL SCHEMATIC DIAGRAM



### Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS5N150	S5N150	SO-8	TAPE & REEL

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	150	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	150	V
V <sub>GS</sub>	Gate- source Voltage	$\pm 20$	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	5	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	3	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	20	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2.5	W
T <sub>stg</sub>	Storage Temperature	-55 to 150	°C
T <sub>j</sub>	Operating Junction Temperature		

(●) Pulse width limited by safe operating area.

# STS5N150

## THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient	Max	50	°C/W
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(\*) When Mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz of Cu and  $t \leq 10$  sec.

## ELECTRICAL CHARACTERISTICS ( $T_{case} = 25$ °C unless otherwise specified)

### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	150			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating } T_C = 125^\circ C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			$\pm 100$	nA

### ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS} \quad I_D = 250 \mu A$	2			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 V \quad I_D = 2.5 A$		0.045	0.06	$\Omega$

## DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (*)	Forward Transconductance	$V_{DS} = 75 V \quad I_D = 5 A$		TBD		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		TBD TBD TBD		pF pF pF

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 75\text{ V}$ $I_D = 2.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		TBD TBD		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 120\text{ V}$ $I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}$ (see test circuit, Figure 2)		TBD TBD TBD	28	nC nC nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 75\text{ V}$ $I_D = 2.5\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		TBD TBD		ns ns

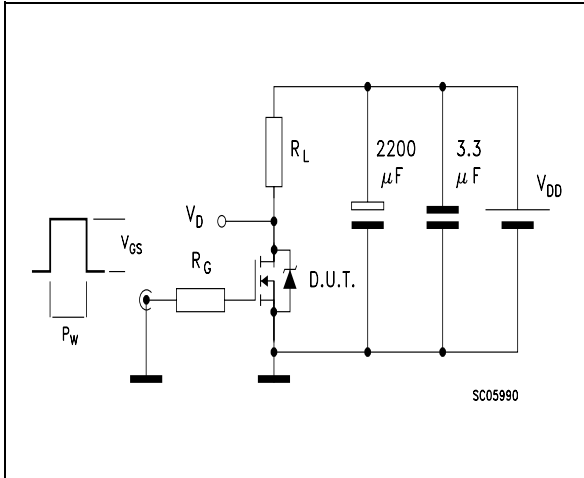
**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				5 20	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 5\text{ A}$ $V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		TBD TBD TBD		ns nC A

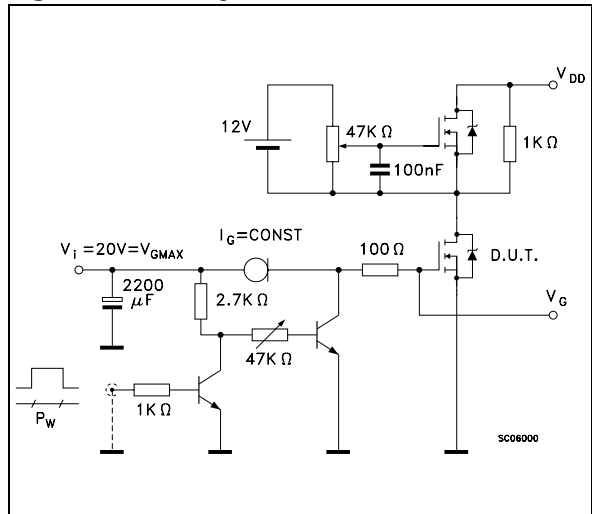
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

( $\bullet$ ) Pulse width limited by safe operating area.

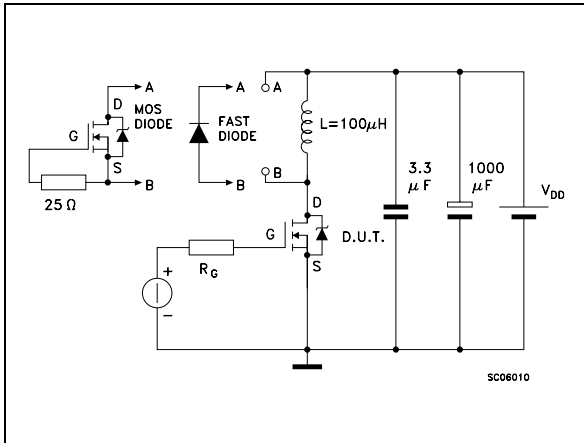
**Fig. 1: Switching Times Test Circuits For Resistive Load**



**Fig. 2: Gate Charge test Circuit**

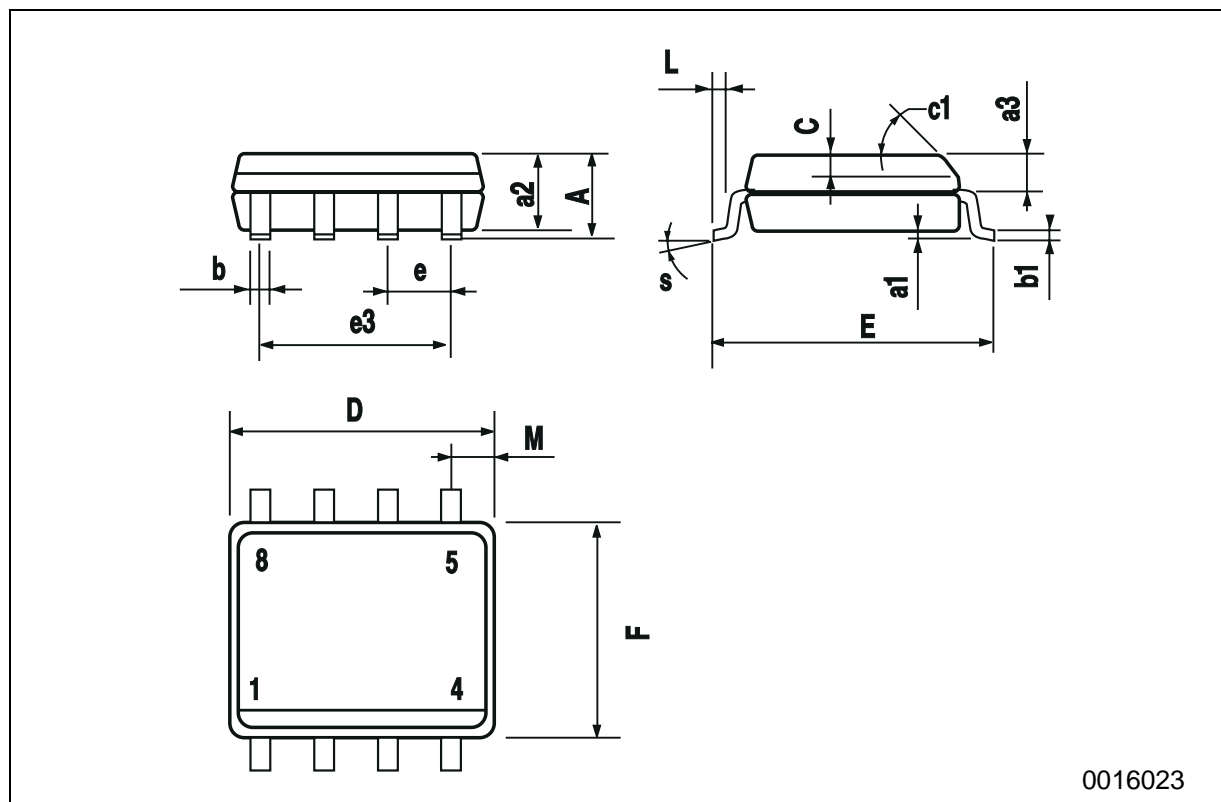


**Fig. 3: Test Circuit For Diode Recovery Behaviour**



**SO-8 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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