ADVANCED LINEAR DEVICES

ALD4706A/ALD4706B
ALD4706

T-79-08

QUAD ULTRA MICROPOWER RAIL TO RAIL CMOS OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD 4706 is a quad monolithic CMOS ultra micropower high slew-rate operational amplifier intended for a broad range of analog applications using ±1V to ±6V dual power supply systems, as well as +2V to +12V battery operated systems. All device characteristics are specified for +5V single supply or ±2.5V dual supply systems. Total supply current for four operational amplifiers is 200µA maximum at 5V supply voltage. It is manufactured with Advanced Linear Devices' enhanced A CMOS silicon gate CMOS process.

The ALD 4706 is designed to offer a tradeoff of performance parameters providing a wide range of desired specifications. It offers the popular industry pin configuration of LM324 and ICL 7641 types.

The ALD 4706 has been developed specifically for the +5V single supply or ±1V to ±6V dual supply user. Several important characteristics of the device make application easier to implement at these voltages. First, each operational amplifier can operate with rail to rail input and output voltages. This means the signal input voltage and output voltage can be equal to or near to the positive and negative supply voltages. This feature allows numerous analog serial stages and flexibility in input signal bias levels. Secondly, each device was designed to accommodate mixed applications where digital and analog circuits may operate off the same power supply or battery. Thirdly, the output stage can typically drive up to 50pF capacitive and 20KΩ resistive loads. These features, combined with extremely low input currents, high open loop voltage gain of 100V/mV, useful bandwidth of 200KHz, a slew rate of 0.17V/µs, low power dissipation of 0.5mW, low offset voltage and temperature drift, make the ALD 4706 a versatile, ultra micropower quad operational amplifier.

The ALD 4706, designed and fabricated with silicon gate CMOS technology, offers 0.1pA typical input bias current. Due to low voltage and low power operation, reliability and operating characteristics, such as input bias currents and warm up time, are greatly improved.

ORDERING INFORMATION

	Operating Temperature Range		
	-55°C to +125°C	0°C to +70°C	0°C to +70°C
+25°C V_{OS} (mV)	14-Pin CERDIP Package	24-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package
2.0	ALD 4706A DB	ALD 4706A SF	ALD 4706A PB
5.0	ALD 4706B DB	ALD 4706B SF	ALD 4706B PB
10.0	ALD 4706 DB	ALD 4706 SF	ALD 4706 PB

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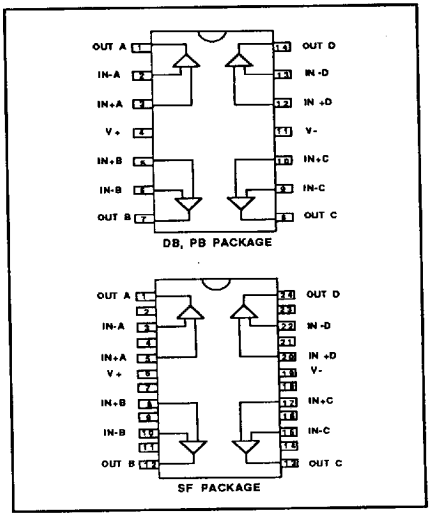
PIN CONFIGURATION



FEATURES

- All parameters specified for + 5V single supply or ± 2.5V dual supply systems
- Rail to rail input and output voltage ranges
- Unity gain stable
- Extremely low input bias currents – 0.1pA
- High source impedance applications
- Dual power supply ±1.0V to ±6.0V
- Single power supply +2V to +12V
- High voltage gain
- Output short circuit protected
- Unity gain bandwidth of 0.2MHz
- Slew rate of 0.17V/µs
- Power dissipation of 20µA per op amp
- Symmetrical output drive

APPLICATIONS

- Voltage follower/buffer/amplifier
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter

QUAD ULTRA MICROPOWER RAIL TO RAIL CMOS OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD} — 13.2V
Differential input voltage range — -0.3V to V_{DD} +0.3V
Power dissipation — 600 mW
Operating temperature range 4706XPB/4706XSF — 0°C to +70°C
4706XDB — -55°C to +125°C
Storage temperature range — -65°C to +150°C
Lead temperature, 10 seconds — +300°C

DC AND OPERATING ELECTRICAL CHARACTERISTICS

T_A = 25°C V_{DD} = 5.0V (V_S = ±2.5V in dual supply operation) unless otherwise specified

Parameter	Symbol	4706A			4706B			4706			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Supply Voltage	V_S	±1.0		±6.0	±1.0		±6.0	±1.0		±6.0	V	Dual Supply
	V_{DD}	2.0		12.0	2.0		12.0	2.0		12.0	V	Single Supply
Input Offset Voltage	V_{OS}			2.0			5.0			10.0	mV	R_S≤100KΩ
				2.8			5.8			11.0	mV	0°C≤T_A≤+70°C
Input Offset Current	I_{OS}		0.1	20		0.1	20		0.1	20	pA	T_A = 25°C
				200			200			200	pA	0°C≤T_A≤+70°C
Input Bias Current	I_B		0.1	20		0.1	20		0.1	20	pA	T_A = 25°C
				200			200			200	pA	0°C≤T_A≤+70°C
Input Voltage Range	V_{IR}	0.0		5.0	0.0		5.0	0.0		5.0	V	V_{DD} = +5V
		-2.5		+2.5	-2.5		+2.5	-2.5		+2.5	V	V_S = ±2.5V
Input Resistance	R_{IN}		10^{13}			10^{13}			10^{13}		Ω	
Input Offset Voltage Drift	TCV_{OS}		7			7			10		µV/°C	R_S≤100KΩ
Power Supply Rejection Ratio	PSRR	65	83		65	83		60	83		dB	R_S≤100KΩ
		65	83		65	83		60	83		dB	0°C≤T_A≤+70°C
Common Mode Rejection Ratio	CMRR	65	83		65	83		60	83		dB	R_S≤100KΩ
		65	83		65	83		60	83		dB	0°C≤T_A≤+70°C
Large Signal Voltage Gain	A_V	10	60		10	60		7	50		V/mV	R_L=100KΩ
			300			300			300		V/mV	R_L≥1MΩ
		10			10			7			V/mV	R_L=100KΩ
Output Voltage Range	V_O low		0.001	0.01		0.001	0.01		0.001	0.01	V	R_L=1MΩ V_{DD}=5V
	V_O high	4.99	4.999		4.99	4.999		4.99	4.999		V	0°C≤T_A≤+70°C
	V_O low		-2.40	-2.25		-2.40	-2.25		-2.40	-2.25	V	R_L=100KΩ V_S=±2.5V
	V_O high	2.25	2.40		2.25	2.40		2.25	2.40		V	0°C≤T_A≤+70°C
Output Short Circuit Current	I_{SC}		200			200			200		µA	
Supply Current	I_S		120	200		120	200		120	200	µA	V_{IN}=0V No Load
Power Dissipation	P_D			1.0			1.0			1.0	mW	All amplifiers V_S=±2.5V

DC AND OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	4706A			4706B			4706			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Capacitance	C_{IN}		1			1			1		pF	
Bandwidth	B_W		200			200			200		KHz	
Slew Rate	S_R		0.17			0.17			0.17		V/µS	R_L=100KΩ A_V=+1
Rise time	t_r		1.0			1.0			1.0		µS	R_L=100KΩ
Overshoot Factor			20			20			20		%	R_L= 100KΩ C_L= 50pF
Settling Time	t_s		10.0			10.0			10.0		µS	0.1% A_V=1 C_L= 50pF R_L=100KΩ
Channel Separation	cs		140			140			140		dB	A_V=100

T_A = 25°C V_S = ±1.0V unless otherwise specified

Parameter	Symbol	4706A			4706B			4706			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Power Supply Rejection Ratio	PSRR		80			80			80		dB	R_S≤1MΩ
Common Mode Rejection Ratio	CMRR		80			80			80		dB	R_S≤1MΩ
Large Signal Voltage Gain	A_V		50			50			50		V/mV	R_L=1MΩ
Output Voltage Range	V_O low V_O high	 0.90	-0.95 0.95	-.90	 0.90	-0.95 0.95	-0.90	 0.90	-0.95 0.95	-0.90	V V	R_L=1MΩ
Bandwidth	B_W		200			200			200		KHz	
Slew Rate	S_R		0.1			0.1			0.1		V/µS	A_V=+1 C_L=50pF

V_S = ±2.5V –55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameter	Symbol	4706A DB			4706B DB			47016DB			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V_{os}			3.0			6.0			15.0	mV	R_S≤1MΩ
Input Offset Current	I_{os}		1	4		1	4		1	4	nA	
Input Bias Current	I_B		1	4		1	4		1	4	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		60	75		dB	R_S≤1MΩ
Common Mode Rejection Ratio	CMRR	60	83		60	83		60	83		dB	R_S≤1MΩ
Large Signal Voltage Gain	A_V	10	50		10	50		7	50		V/mV	R_L=1MΩ
Output Voltage Range	$V_O$low $V_O$high	 2.25	-2.40 2.40	-2.25	 2.25	-2.40 2.40	-2.25	 2.25	-2.40 2.40	-2.25	V V	R_L=MΩ

Design & Operating Notes:

1. The ALD 4706 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accomodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD 4706 is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency.

2. The ALD 4706 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5 V below the positive supply voltage. Since offset voltage trimming on the 4706 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions above this switching point. The user should however, be aware that this switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision in his design to allow for input offset voltage variations.

3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 0.1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than $10^{13}\ \Omega$ would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

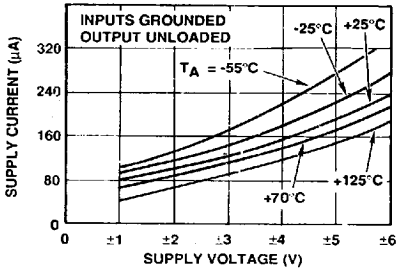
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.

5. The ALD 4706 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.

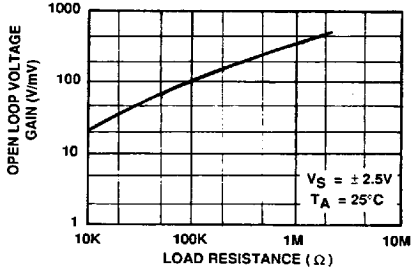
6. The ALD 4706, with its ultra micropower operation, offers numerous benefits in reduced power supply requirements, less noise coupling and current spikes, less thermally induced drift, better overall reliability due to lower self heating, and lower input bias current. It requires practically no warm up time as the chip junction heats up to only 0.1° C above ambient temperature under most operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

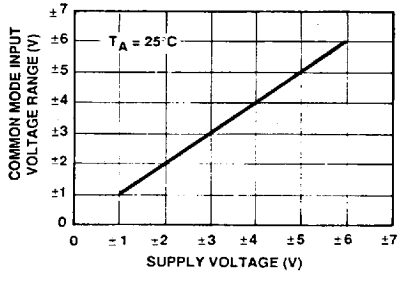
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



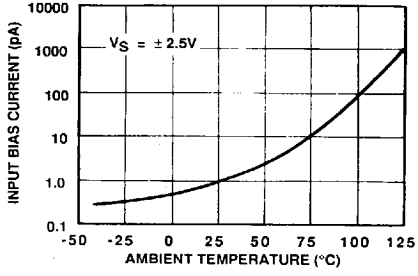
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

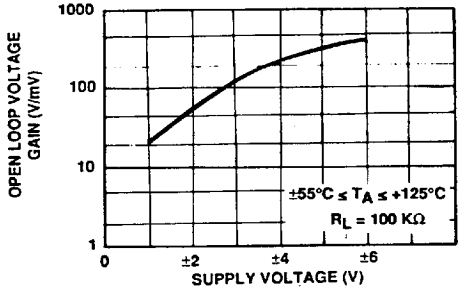


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

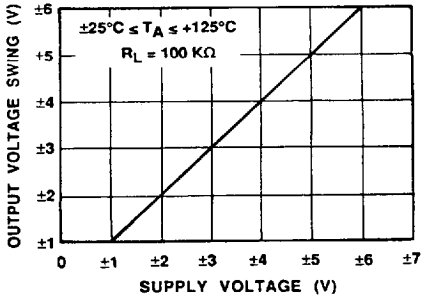


TYPICAL PERFORMANCE CHARACTERISTICS

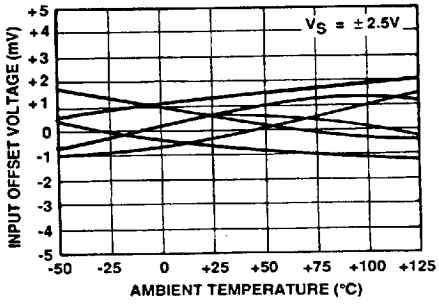
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



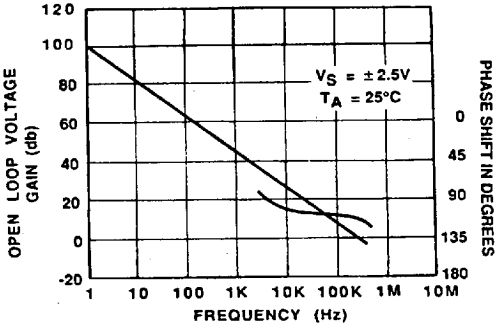
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



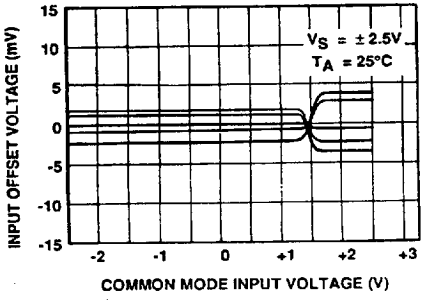
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE REPRESENTATIVE UNITS



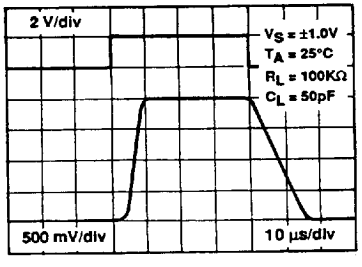
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



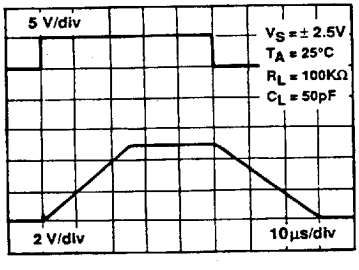
INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE



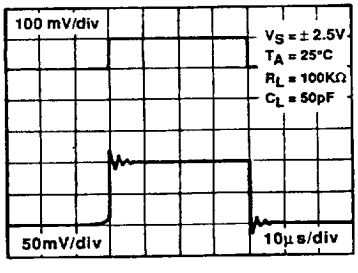
LARGE-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE

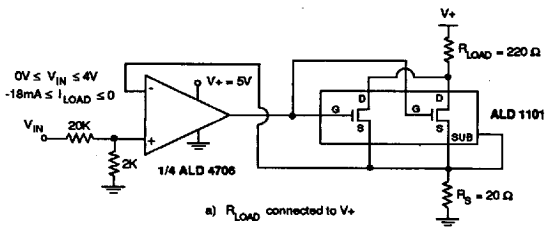


SMALL-SIGNAL TRANSIENT RESPONSE

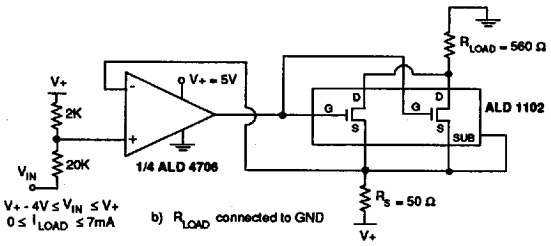


TYPICAL APPLICATIONS

V TO I AMPLIFIER



a) R_{LOAD} connected to V+



b) R_{LOAD} connected to GND

RAIL TO RAIL VOLTAGE FOLLOWER/BUFFER

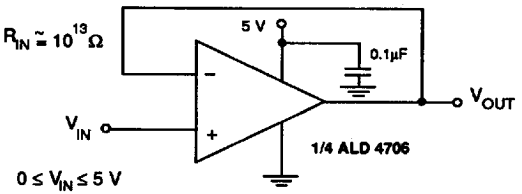
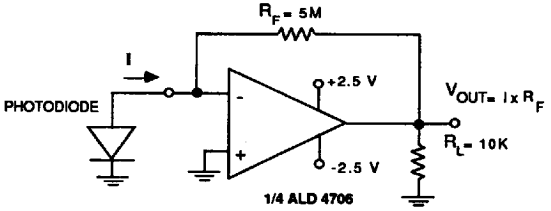
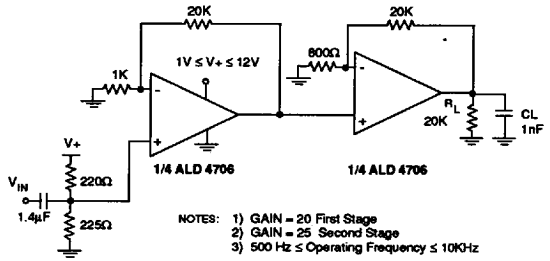


PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER

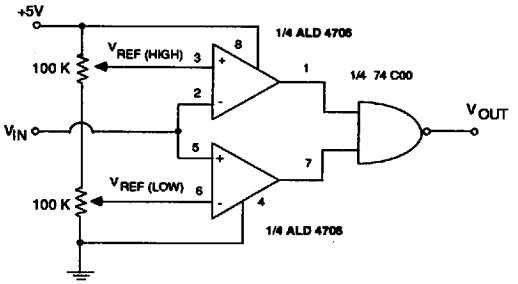


TWO STAGE HIGH GAIN AMPLIFIER



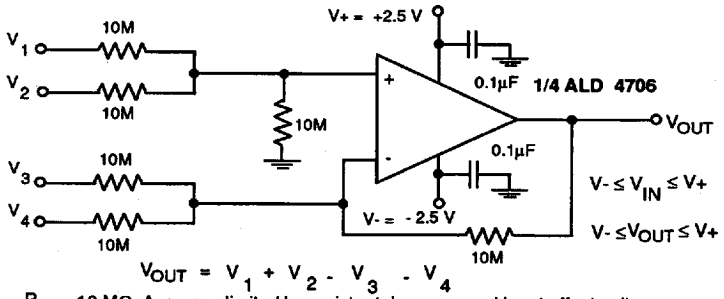
NOTES: 1) GAIN = 20 First Stage
2) GAIN = 25 Second Stage
3) 500 Hz ≤ Operating Frequency ≤ 10KHz

RAIL TO RAIL WINDOW COMPARATOR



V_{OUT} Low for $V_{REF (LOW)} < V_{IN} < V_{REF (HIGH)}$

HIGH INPUT IMPEDANCE RAIL TO RAIL PRECISION DC SUMMING AMPLIFIER



$V_{OUT} = V_1 + V_2 - V_3 - V_4$

R_{IN} = 10 MΩ Accuracy limited by resistor tolerances and input offset voltage