1M×16 CMOS EDO DRAM

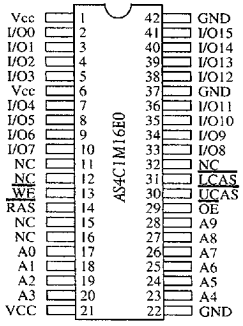
Preliminary information

Features

- Organization: 1,048,576 words × 16 bits
- High speed
  - 50/60/70 ns $\overline{RAS}$ access time
  - 25/30/35 ns column address access time
  - 13/15/18 ns $\overline{CAS}$ access time
- Low power consumption
  - Active: 1.0725 W max (4C1M16E0-50)
  - Standby: 5.5 mW max, CMOS I/O
- Extended data out
- 1024 refresh cycles, 16 ms refresh interval
  - $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Read-modify-write
- TTL-compatible, three-state I/O
- JEDEC standard package and pinout
  - 400 mil, 42-pin SOJ
- 5V power supply (4C1M16E0)
- 3.3V power supply (4LC1M16E0)
- Latch-up current ≥ 200 mA
- ESD ≥ 2000 volts

Pin arrangement

SOJ



Pin designation

Pin(s)	Description
A0 to A9	Address inputs
$\overline{RAS}$	Row address strobe
I/O0 to I/O15	Input/output
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{UCAS}$	Column address strobe, upper byte
$\overline{LCAS}$	Column address strobe, lower byte
V_{CC}	Power
GND	Ground

DRAM

Selection guide

	Symbol	4C1M16E0-50	4C1M16E0-60	4C1M16E0-70	Unit
Maximum $\overline{RAS}$ access time	t_{RAC}	50	60	70	ns
Maximum column address access time	t_{CAA}	25	30	35	ns
Maximum $\overline{CAS}$ access time	t_{CAC}	13	15	18	ns
Maximum output enable ($\overline{OE}$) access time	t_{OEA}	13	15	18	ns
Minimum read or write cycle time	t_{RC}	90	110	130	ns
Minimum fast page mode cycle time	t_{PC}	35	40	45	ns
Maximum operating current	I_{CC1}	195	180	165	mA
Maximum CMOS standby current	I_{CC5}	1.0	1.0	1.0	mA

Shaded areas contain advance information.

Functional description

The AS4C1M16E0 is a high performance 16-megabit CMOS Dynamic Random Access Memory (DRAM) organized as 1,048,576 words × 16 bits. The AS4C1M16E0 is fabricated using advanced CMOS technology and innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels. The Alliance 16Mb DRAM family is optimized for use as main memory in PC, workstation, router and switch applications.

The AS4C1M16E0 features a high speed page mode operation where read and write operations within a single row (or page) can be executed at very high speed (15 ns from $\overline{xCAS}$ or 30 ns from address for the 1M16E0-60 device) by toggling column addresses within that row. Row and column addresses are alternately latched into input buffers using the falling edge of $\overline{RAS}$ and $\overline{xCAS}$ inputs respectively. Also, $\overline{RAS}$ is used to make the column address latch transparent, enabling application of column addresses prior to $\overline{xCAS}$ assertion. The AS4C1M16 provides dual $\overline{UCAS}$ and $\overline{LCAS}$ for independent byte control of read and write access.

Extended data out (EDO) read mode enables 60MHz operation using 60ns devices. In contrast to 'fast page mode' devices, data remains active on outputs after $\overline{xCAS}$ is de-asserted high, giving system logic more time to latch the data. Use $\overline{OE}$ and $\overline{WE}$ to control output impedance and prevent bus contention during read-modify-write and shared bus applications. Outputs also go to high impedance at the last occurrance of $\overline{RAS}$ and $\overline{xCAS}$ going high.

Refresh on the 1024 address combinations of A0 to A9 must be performed every 16 ms using:

- $\overline{RAS}$-only refresh: $\overline{RAS}$ is asserted while $\overline{xCAS}$ is held high. Each of the 1024 rows must be strobed. Outputs remain high impedence.
- Hidden refresh: $\overline{xCAS}$ is held low while $\overline{RAS}$ is toggled. Refresh address is generated internally. Outputs remain low impedence with previous valid data.
- $\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR): At least one $\overline{xCAS}$ is asserted prior to $\overline{RAS}$. Refresh address is generated internally. Outputs are high-impedence ($\overline{OE}$ and $\overline{WE}$ are don't care).
- Normal read or write cycles refresh the row being accessed.

The AS4C1M16E0 and AS4LC1M16E0 are available in the standard 42-pin plastic SOJ package. The 4C1M16 device operates with a single power supply of 5V ± 0.5V and the 4LC1M16 operates at 3.3V ± 0.3V. Both provide TTL compatible inputs and outputs.

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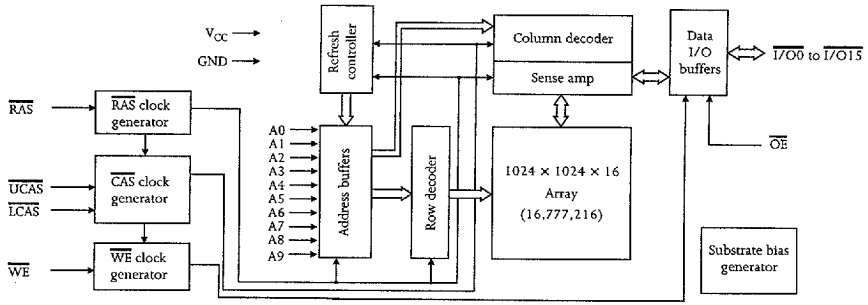
Logic block diagram



Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage	4C1M16E0	V_{CC}	4.5	5.0	5.5	V
	4LC1M16E0	V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage	4C1M16E0	V_{IH}	2.4	–	V_{CC}	V
	4LC1M16E0	V_{IH}	2.0	–	V_{CC}	V
		V_{IL}	−0.5†	–	0.8	V
Ambient operating temperature		T_A	0		70	°C

†V_{IL} min -3.0V for pulse widths less than 5 ns.

Recommended operating conditions apply throughout this document unlesss otherwise specified.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{in}	-1.0	+7.0	V
Input voltage (I/Os)	$V_{I/O}$	-1.0	V_{CC} + 0.5	V
Power supply voltage	V_{CC}	-1.0	+7.0	V
Storage temperature (plastic)	T_{STG}	-55	+150	°C
Soldering temperature × time	T_{SOLDER}	–	260 × 10	°C × sec
Power dissipation	P_D	–	1	W
Short circuit output current	I_{out}	–	50	mA
Latch-up current		200	–	mA

DC electrical characteristics

			-50		-60		-70			
Parameter	Symbol	Test conditions	Min	Max	Min	Max	Min	Max	Unit	Notes
Input leakage current	I_{IL}	$0V \le V_{in} \le +5.5V$, Pins not under test = 0V	-10	+10	-10	+10	-10	+10	µA	
Output leakage current	I_{OZ}	D_{OUT} disabled, $0V \le V_{out} \le +5.5V$	-10	+10	-10	+10	-10	+10	µA	
Operating power supply current	I_{CC1}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling; t_{RC}=min	–	195	–	180	–	165	mA	1,2
TTL standby power supply current	I_{CC2}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} \ge V_{IH}$	–	2.0	–	2.0	–	2.0	mA	
Average power supply current, $\overline{RAS}$ refresh mode or CBR	I_{CC3}	$\overline{RAS}$ cycling, $\overline{UCAS} = \overline{LCAS} \ge V_{IH}$, t_{RC} = min of $\overline{RAS}$ low after $\overline{XCAS}$ low.	–	195	–	180	–	165	mA	1
Fast page mode average power supply current	I_{CC4}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IL}$, Address cycling: t_{SC} = min	–	110	–	100	–	90	mA	1, 2
CMOS standby power supply current	I_{CC5}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{CC}$ - 0.2V	–	1.0	–	1.0	–	1.0	mA	
Self ref. power supply current	I_{CC6}	$\overline{RAS}$, $\overline{XCAS}$, < 0.2 V, measured after min. T_{RASS}	–	1.0	-	1.0	–	1.0	mA	1
Output voltage	V_{OH}	I_{OUT} = -5.0 mA (5V), -2.0mA (3.3 V)	2.4	–	2.4	–	2.4	–	V	
	V_{OL}	I_{OUT} = 4.2 mA (5V), -2.0mA (3.3 V)	–	0.4	–	0.4	–	0.4	V	
Refresh current: extended (BBU refresh)	I_{CC7}	T_{RC} = 125 µs (1024 rows @125 µs = 128 ms)	–	1	-	1	-	1	mA	

Shaded areas contain advance information.

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AC parameters common to all waveforms

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{RC}	Random read or write cycle time	90	–	110	–	130	–	ns	
t_{RP}	$\overline{RAS}$ precharge time	30	–	40	–	50	–	ns	
t_{RAS}	$\overline{RAS}$ pulse width	50	10K	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ pulse width	13	–	15	–	18	–	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	15	37	15	45	20	52	ns	6
t_{RAD}	$\overline{RAS}$ to column address delay time	15	25	15	30	15	35	ns	7
$t_{RSH(R)}$	$\overline{CAS}$ to $\overline{RAS}$ hold time (Read cycle)	13	–	15	–	18	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CAS}$ hold time	50	–	60	–	70	–	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	5	–	5	–	ns	
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns	
t_{RAH}	Row address hold time	10	–	10	–	10	–	ns	
t_T	Transition time (rise and fall)	2	50	2	50	2	50	ns	4,5
t_{REF}	Refresh period	–	16	–	16	–	16	ms	3
t_{CLZ}	$\overline{CAS}$ to output in Low Z	0	–	0	–	0	–	ns	8

Read cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{RAC}	Access time from $\overline{RAS}$	–	50	–	60	–	70	ns	6
t_{CAC}	Access time from $\overline{CAS}$	–	13	–	15	–	18	ns	6,13
t_{AA}	Access time from address	–	25	–	30	–	35	ns	7,13
$t_{AR(R)}$	Column add hold from $\overline{RAS}$	40	–	45	–	55	–	ns	
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns	
t_{RCH}	Read command hold time to $\overline{CAS}$	0	–	0	–	0	–	ns	9
t_{RRH}	Read command hold time to $\overline{RAS}$	0	–	0	–	0	–	ns	9
t_{RAL}	Column address to $\overline{RAS}$ lead time	25	–	30	–	35	–	ns	
t_{CPN}	$\overline{CAS}$ precharge time	10	–	10	–	10	–	ns	
t_{OFF}	Output buffer turn-off time	0	15	0	15	0	18	ns	8,10

Write cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns	
t_{CAH}	Column address hold time	10	–	10	–	15	–	ns	
t_{AWR}	Column address hold time to $\overline{RAS}$	40	–	45	–	55	–	ns	
t_{WCS}	Write command setup time	0	–	0	–	0	–	ns	11
t_{WCH}	Write command hold time	10	–	10	–	15	–	ns	11
t_{WCR}	Write command hold time to $\overline{RAS}$	40	–	45	–	55	–	ns	
t_{WP}	Write command pulse width	10	–	10	–	15	–	ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	13	–	15	–	18	–	ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	13	–	15	–	118	–	ns	
t_{DS}	Data-in setup time	0	–	0	–	0	–	ns	12
t_{DH}	Data-in hold time	10	–	10	–	15	–	ns	12
t_{DHR}	Data-in hold time to $\overline{RAS}$	40	–	45	–	55	–	ns	

Read-modify-write cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{RWC}	Read-write cycle time	131	–	155	–	181	–	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay time	73	–	85	–	98	–	ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay time	36	–	40	–	46	–	ns	11
t_{AWD}	Column address to $\overline{WE}$ delay time	48	–	55	–	63	–	ns	11
$t_{RSH(W)}$	$\overline{CAS}$ to $\overline{RAS}$ hold time (write)	13	–	15	–	18	–	ns	
$t_{CAS(W)}$	$\overline{CAS}$ pulse width (write)	13	–	15	–	18	–	ns	

Fast page mode cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{PC}	Read or write cycle time	35	–	40	–	45	–	ns	14
t_{CPA}	Access time from $\overline{CAS}$ precharge	–	30	–	35	–	40	ns	13
t_{CP}	$\overline{CAS}$ precharge time	10	–	10	–	10	–	ns	
t_{PCM}	Fast page mode RMW cycle	76	–	85	–	96	–	ns	
t_{CRW}	Page mode $\overline{CAS}$ pulse width (RMW)	54	–	60	–	69	–	ns	
t_{RASP}	$\overline{RAS}$ pulse width	50	100K	60	100K	70	100K	ns	

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Refresh cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$)	10	–	10	–	10	–	ns	3
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$)	10	–	15	–	15	–	ns	3
t_{RPC}	$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ precharge time (CBR counter test)	10	–	10	–	10	–	ns	

Self-refresh cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{RASS}	$\overline{RAS}$ Pulse Width (CBR Self Refresh)	100K	–	100K	–	100K	–	ns	
t_{RPS}	$\overline{RAS}$ Precharge Time (CBR Self Refresh)	85	–	100	–	120	–	ns	
t_{CHD}	$\overline{CAS}$ Hold Time (CBR Self Refresh)	15	–	15	–	15	–	ns	

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EDO cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{DOH}	Previous data hold time from $\overline{CAS}$	3	–	3	15	3	18	ns	
t_{REZ}	Output buffer turn off delay from $\overline{RAS}$	3	13	3	15	3	18	ns	
t_{CEZ}	Output buffer turn off delay from $\overline{CAS}$	3	13	3	15	3	18	ns	
t_{WEZ}	Output buffer turn off delay from $\overline{WE}$	3	13	3	15	3	18	ns	
t_{OEZ}	Output buffer turn off delay from $\overline{OE}$	3	13	3	15	3	18	ns	
t_{HPC}	Hyper page mode cycle time	–	20	–	25	–	30	ns	
t_{WPZ}	$\overline{WE}$ pulse width to turn off output buffer	3	–	3	–	3	–	ns	
t_{OPZ}	$\overline{OE}$ pulse width to turn off output buffer	3	–	3	–	3	–	ns	
t_{HPRWC}	Hyper page mode RMW cycle	–	43	–	56	–	71	ns	

Output enable

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10	–	10	–	10	–	ns	
t_{OEA}	$\overline{OE}$ access time	–	13	–	15	–	18	ns	
t_{OED}	$\overline{OE}$ to data delay	13	–	15	–	18	–	ns	
t_{OEZ}	Output buffer turnoff delay from $\overline{OE}$	–	13	–	15	–	18	ns	8
t_{OEH}	$\overline{OE}$ command hold time	13	–	15	–	18	–	ns	

Notes

1 I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on frequency.

2 I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

3 An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).

4 AC Characteristics assume t_T = 5 ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF, V_{IL} (min) ≥ GND and V_{IH} (max) ≤ V_{CC}.

5 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

6 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

7 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

8 Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).

9 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10 t_{OFF} (max) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels. t_{OFF} is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

11 t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.

12 These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-write cycles.

13 Access time is determined by the longest of t_{CAA} or t_{CAC} or t_{CPA}

14 $t_{ASC} \geq t_{CP}$ to achieve t_{PC} (min) and t_{CPA} (max) values.

15 These parameters are sampled and not 100% tested.

16 These characteristics apply to AS4C1M16E0 5V devices. The 3.3V AS4LC1M16E0 functions similarly.

AC test conditions

- Access times are measured with output reference levels of V_{OH} = 2.4V and V_{OL} = 0.4V
- Input rise and fall times: 5 ns

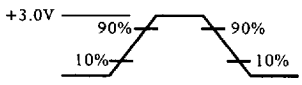


Figure A: Input waveform

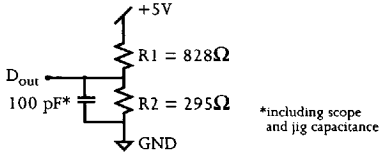


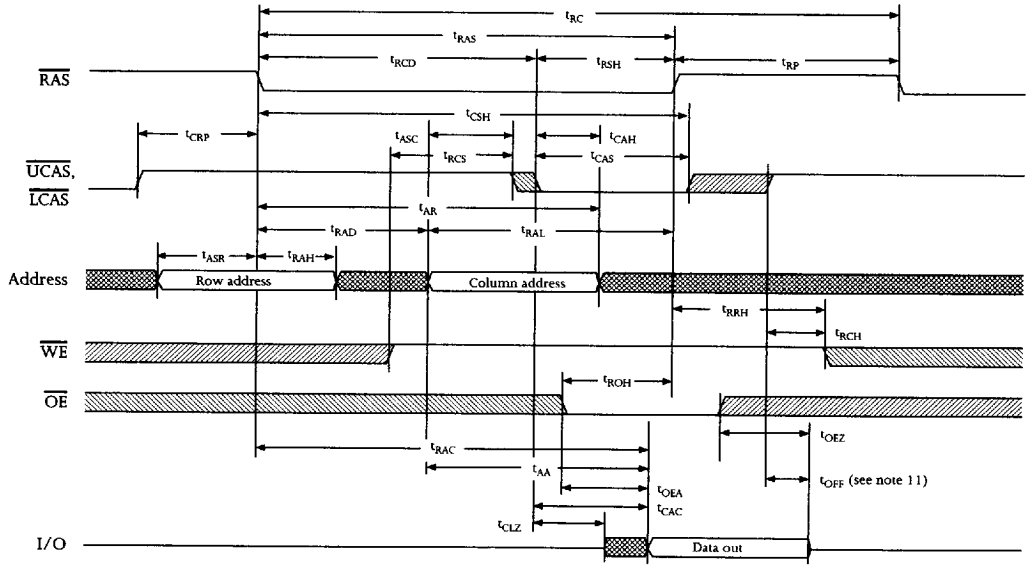
Figure B: Equivalent output load

Key to switching waveforms

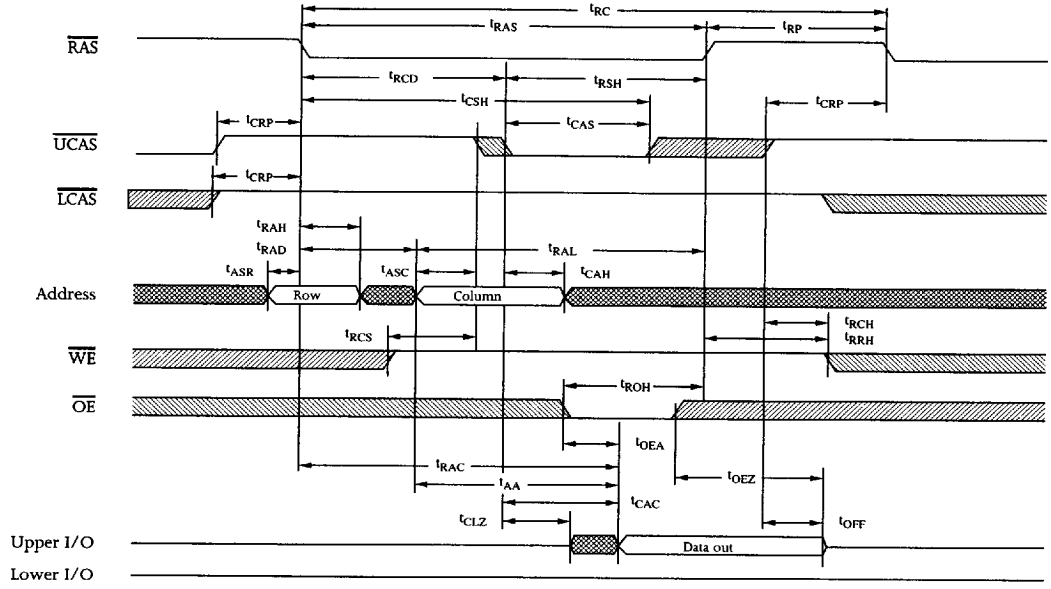
Rising input Falling input Undefined output/don't care

DRAM

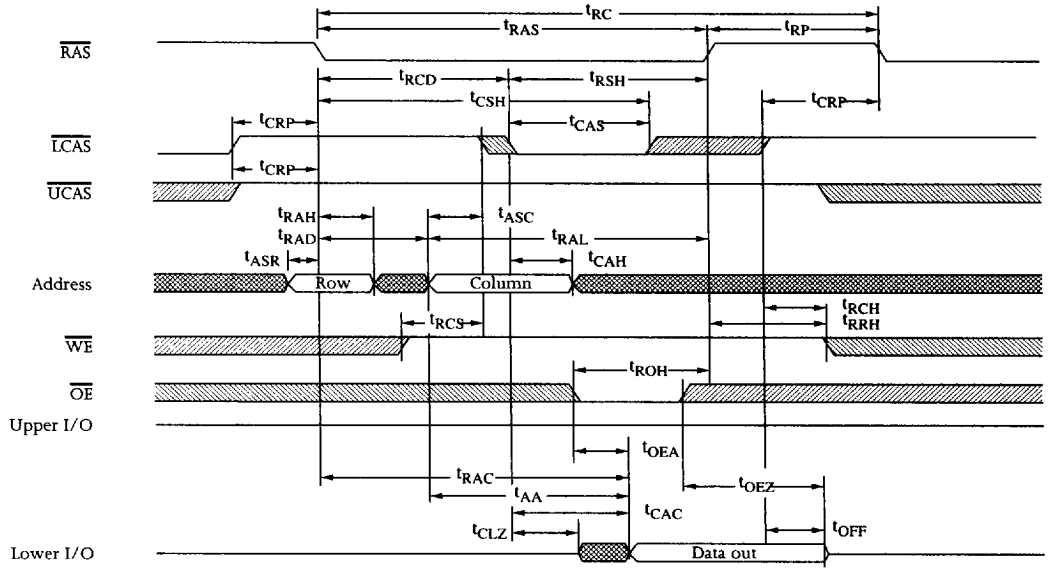
Read waveform



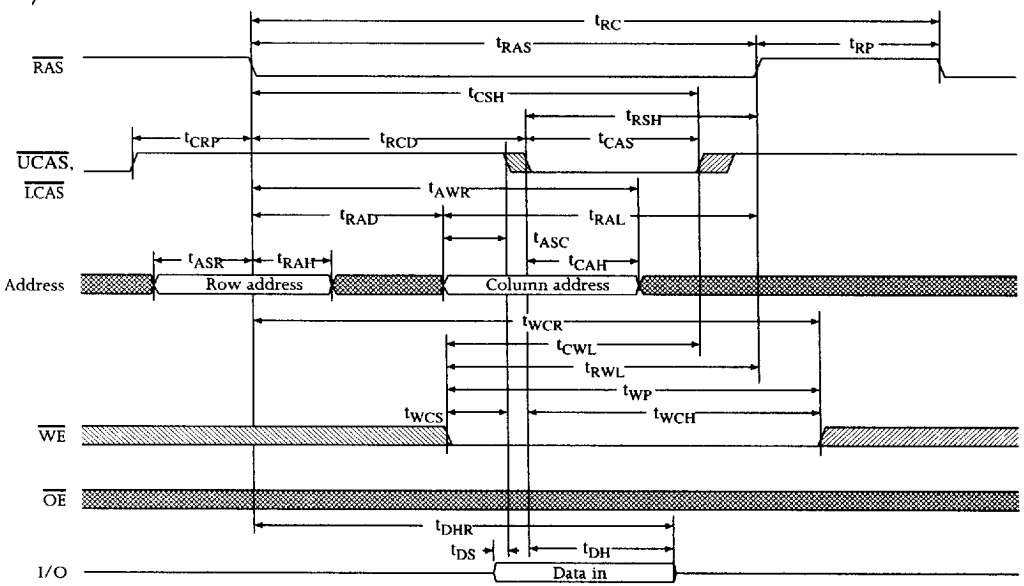
Upper byte read waveform



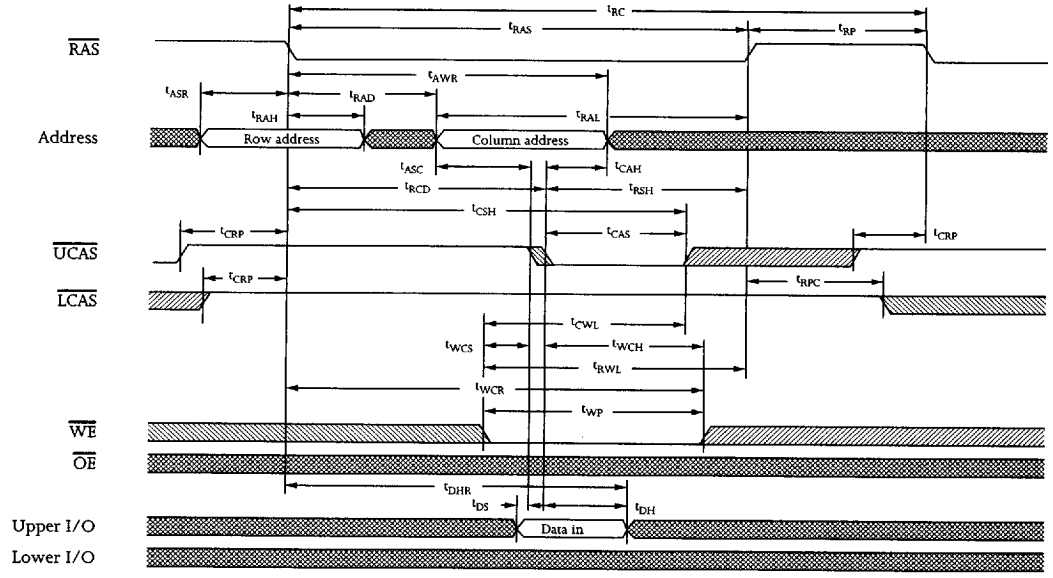
Lower byte read waveform



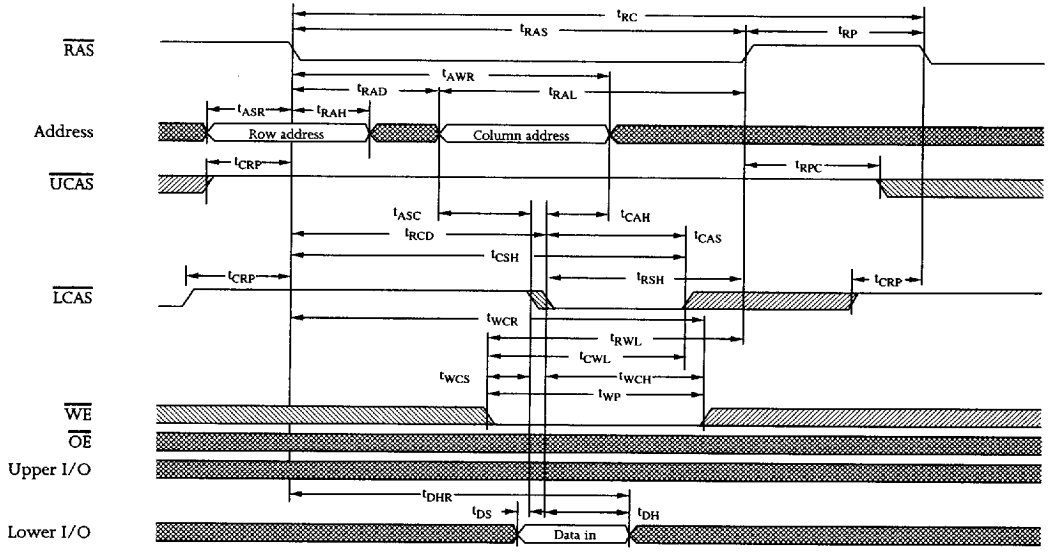
Early write waveform



Upper byte early write waveform

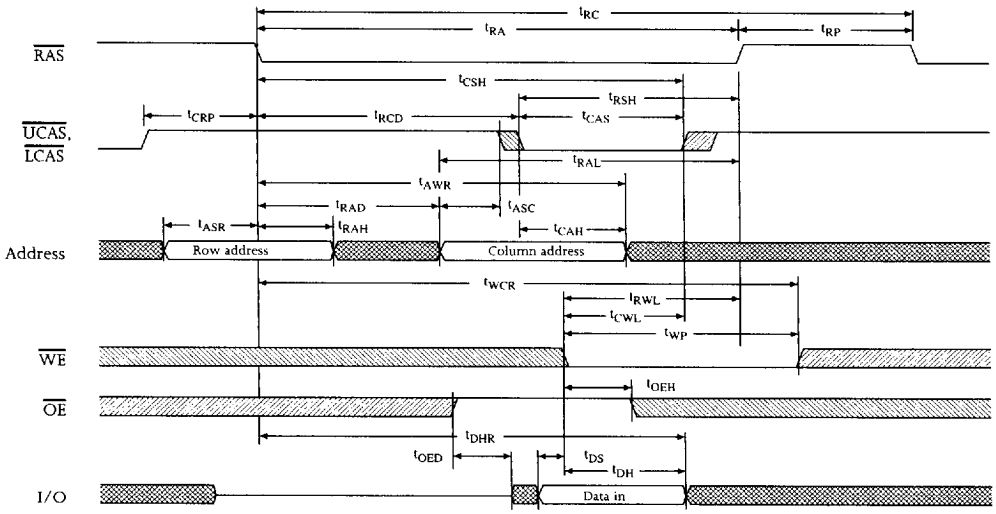


Lower byte early write waveform



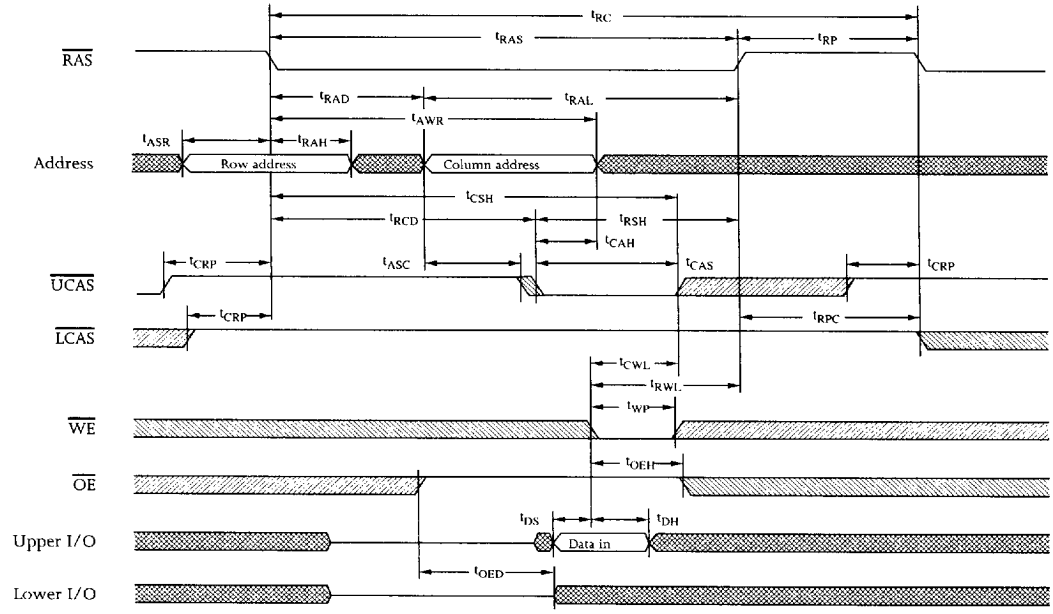
Write waveform

$\overline{OE}$ controlled



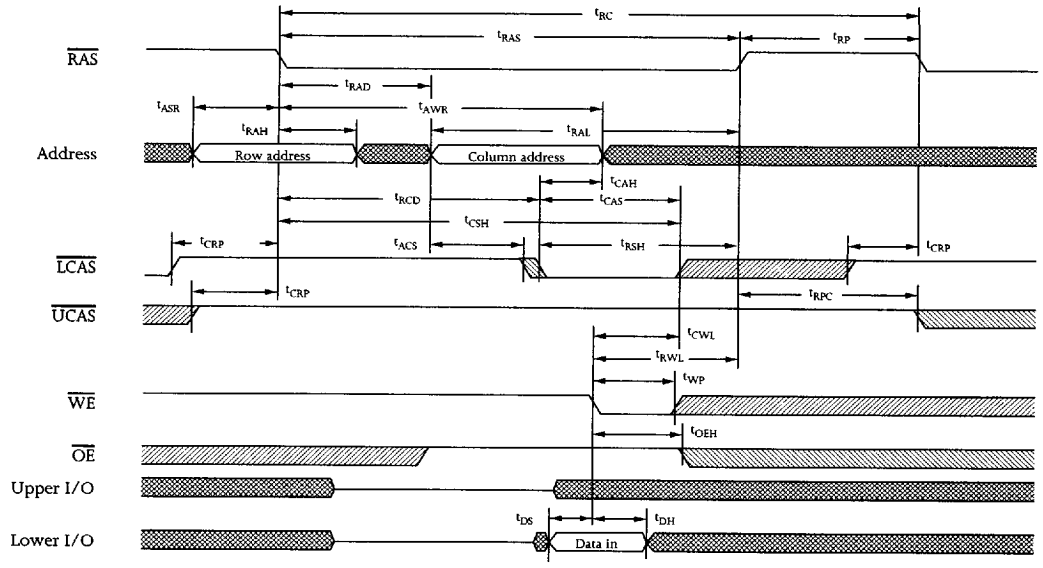
Upper byte write waveform

$\overline{OE}$ controlled

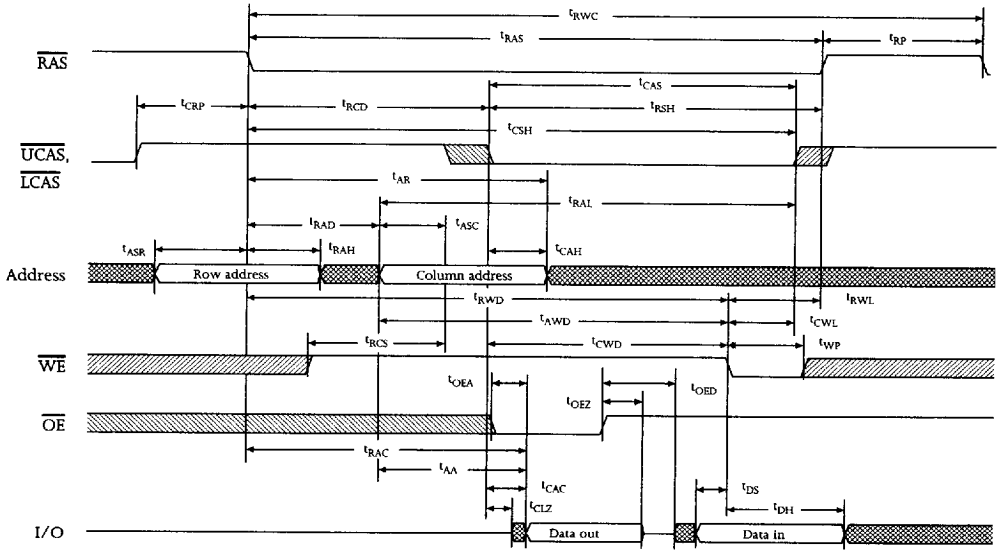


Lower byte write waveform

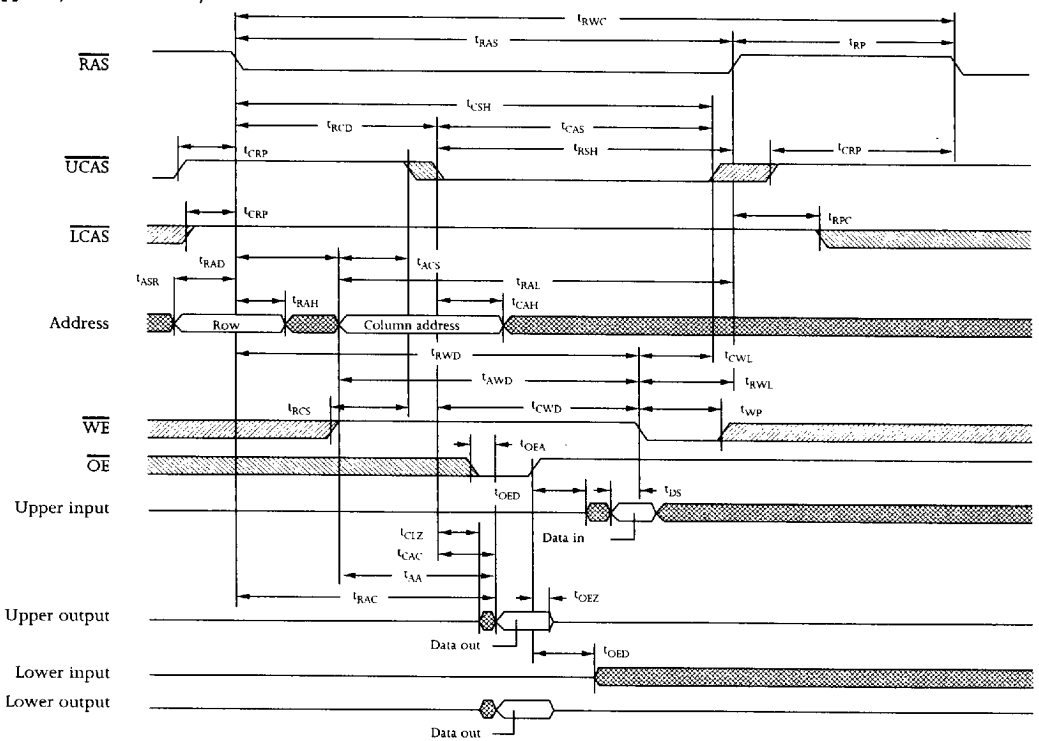
$\overline{OE}$ controlled



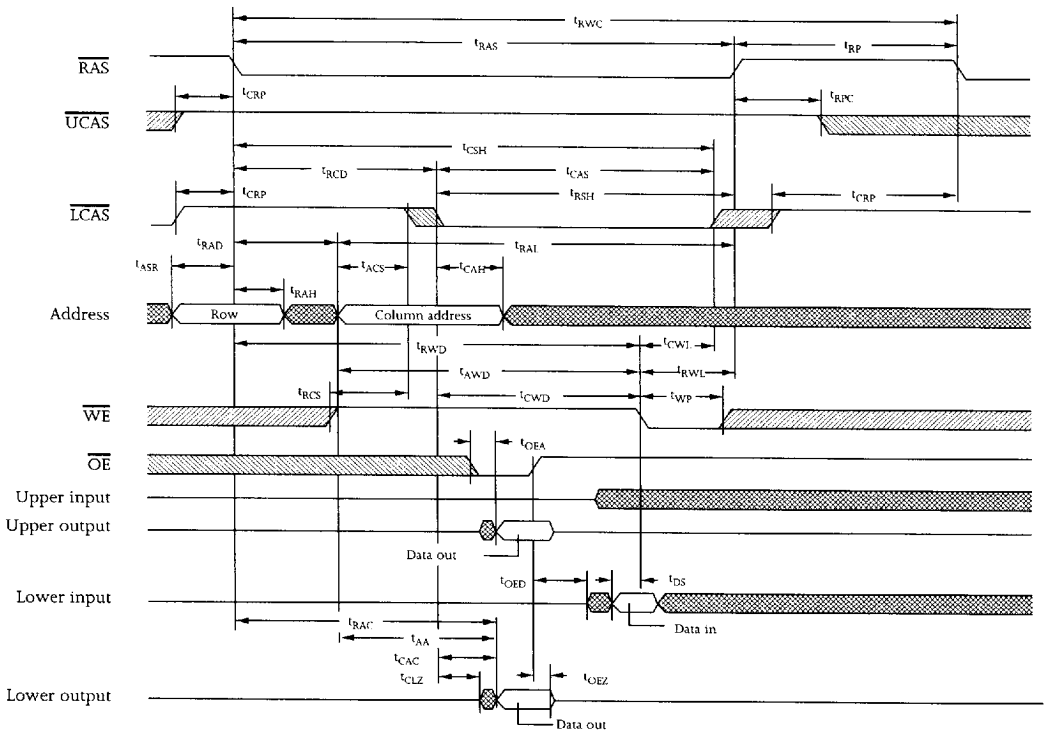
Read-modify-write waveform



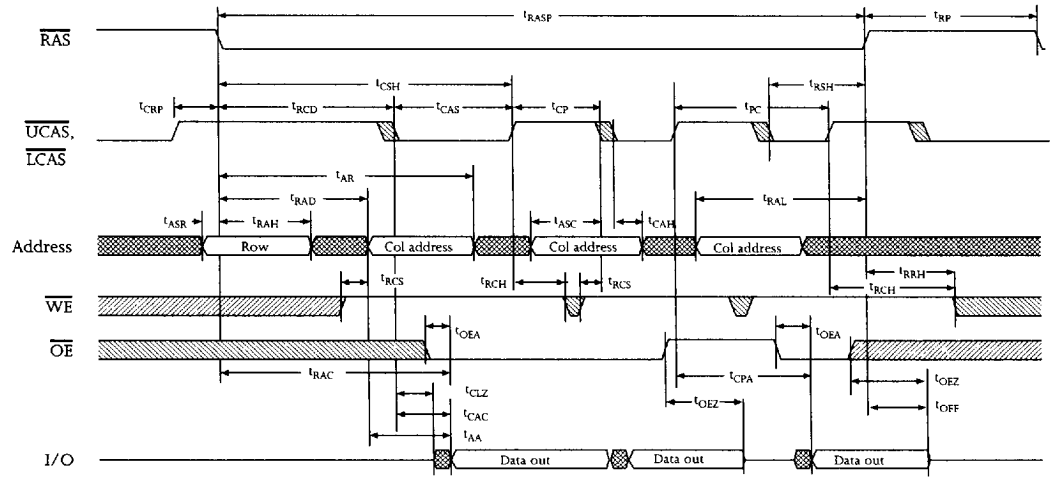
Upper byte read-modify-write waveform



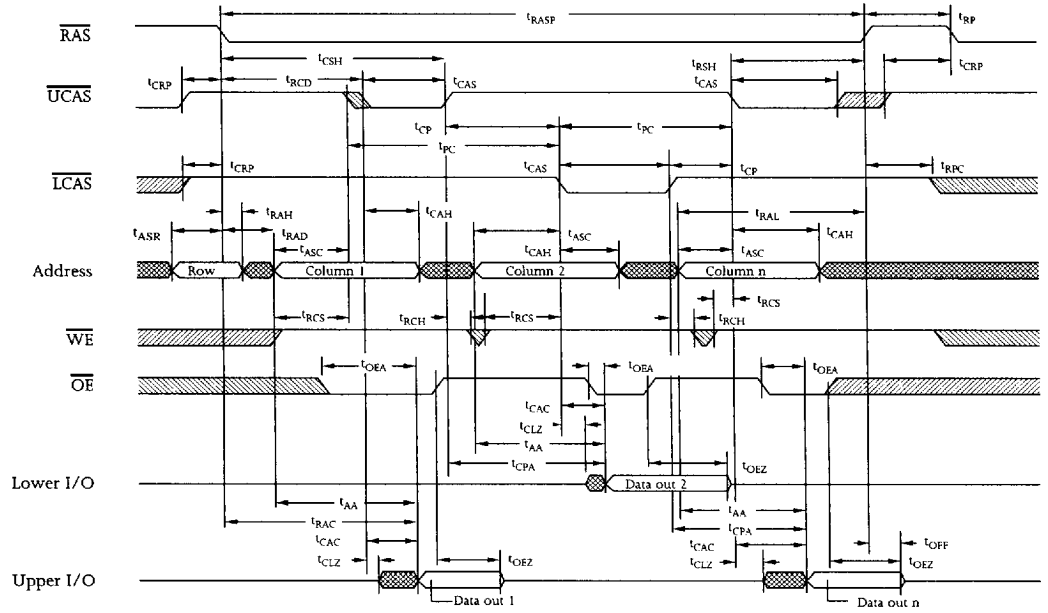
Lower byte read-modify-write waveform



EDO page mode read waveform

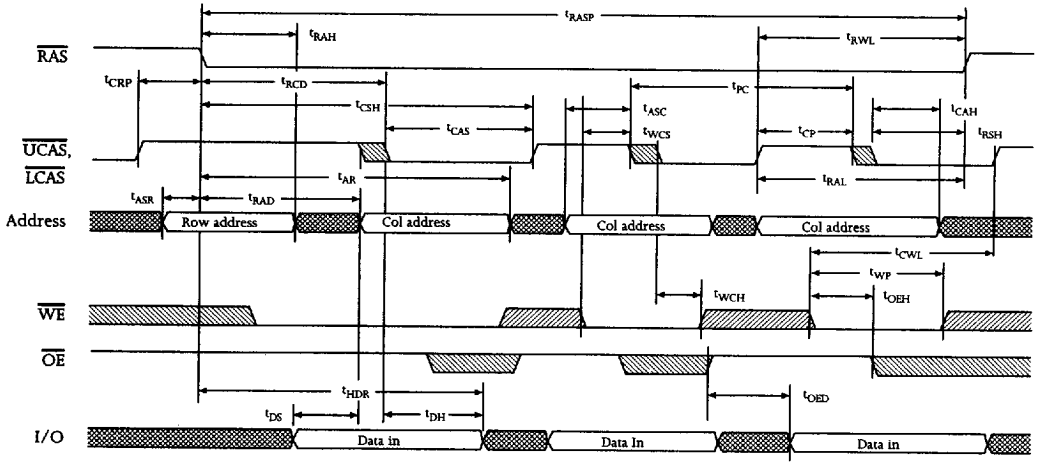


EDO page mode byte read waveform

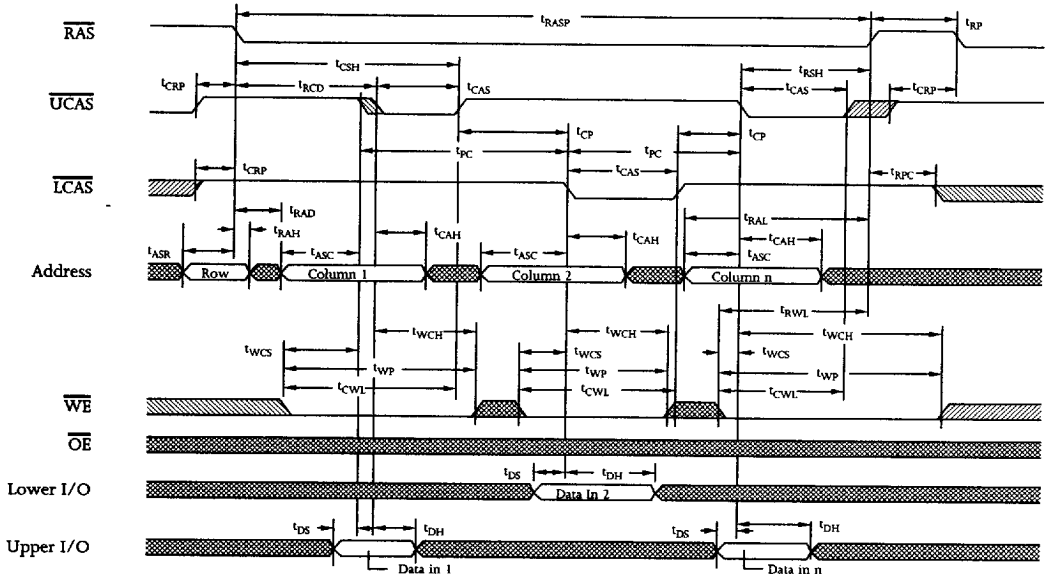


DRAM

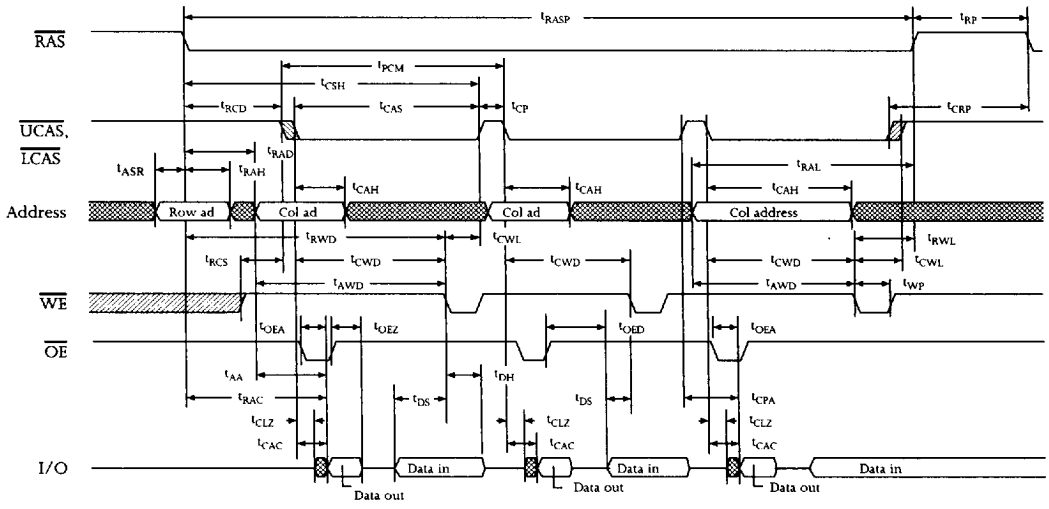
EDO page mode early write waveform



EDO page mode byte early write waveform

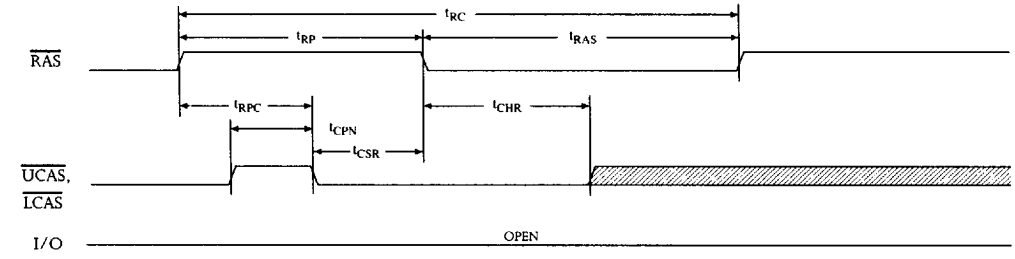


EDO page mode read-modify-write waveform



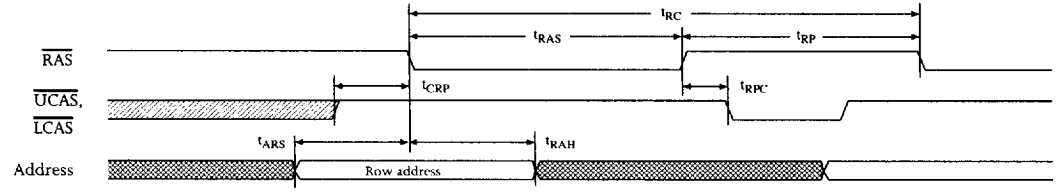
CAS before RAS refresh waveform

WE = A9 = V_{IH} or V_{IL}



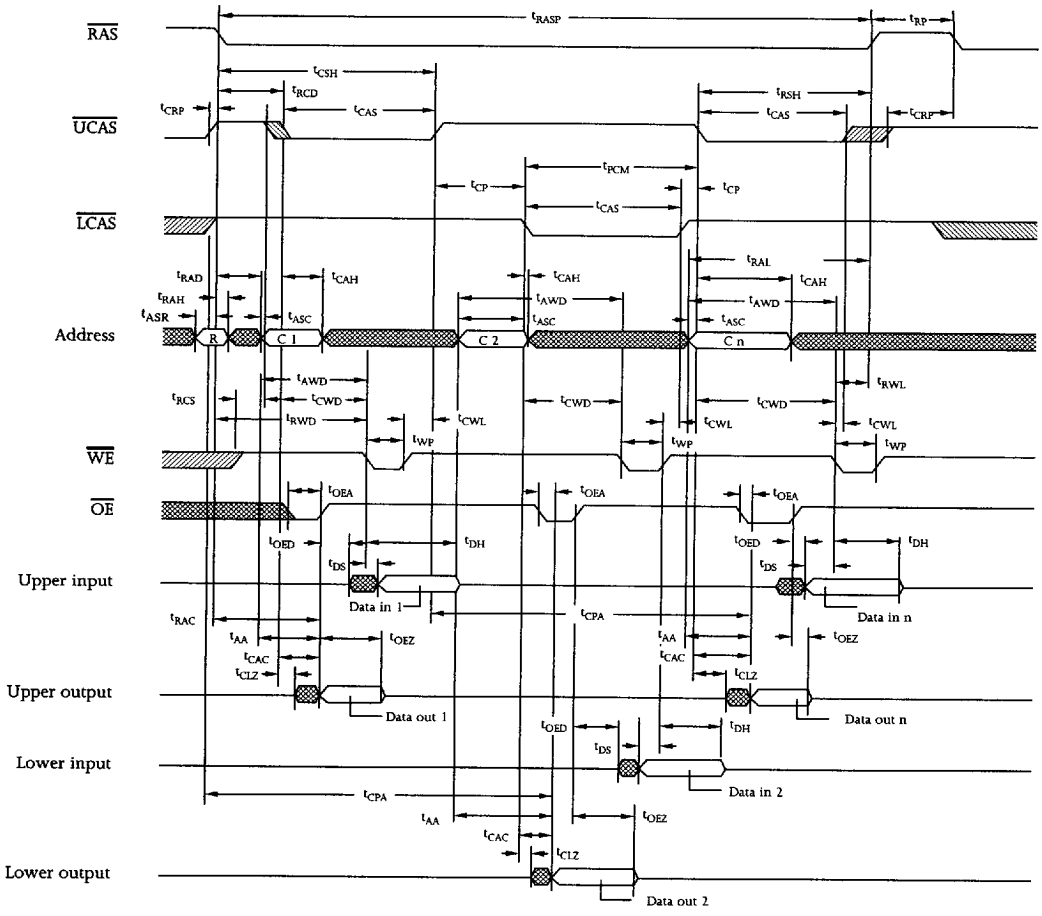
RAS only refresh waveform

WE = OE = V_{IH} or V_{IL}

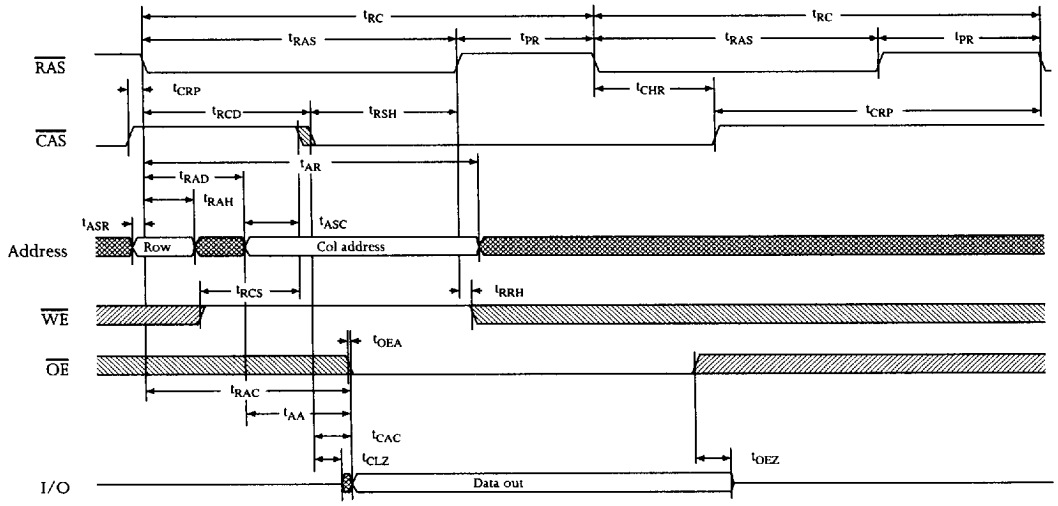


DRAM

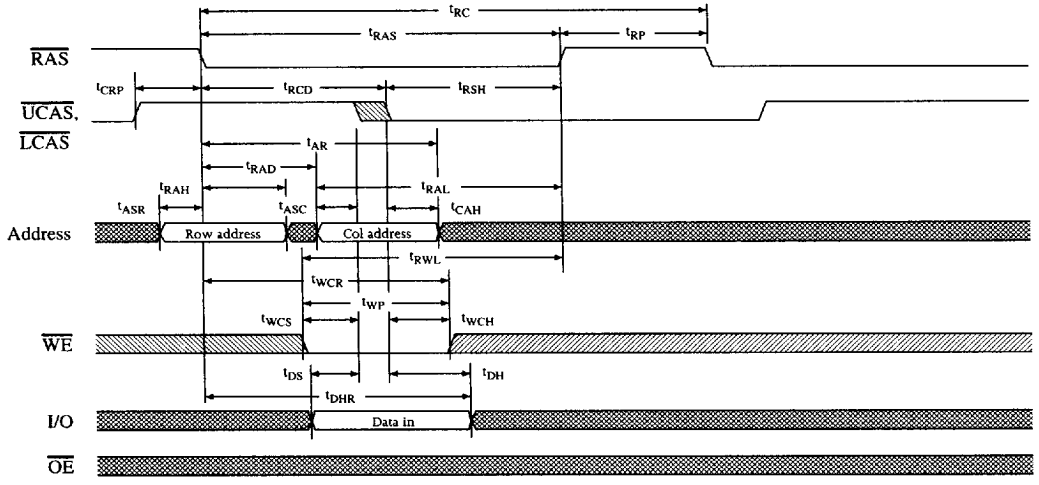
EDO page mode byte read-modify-write waveform



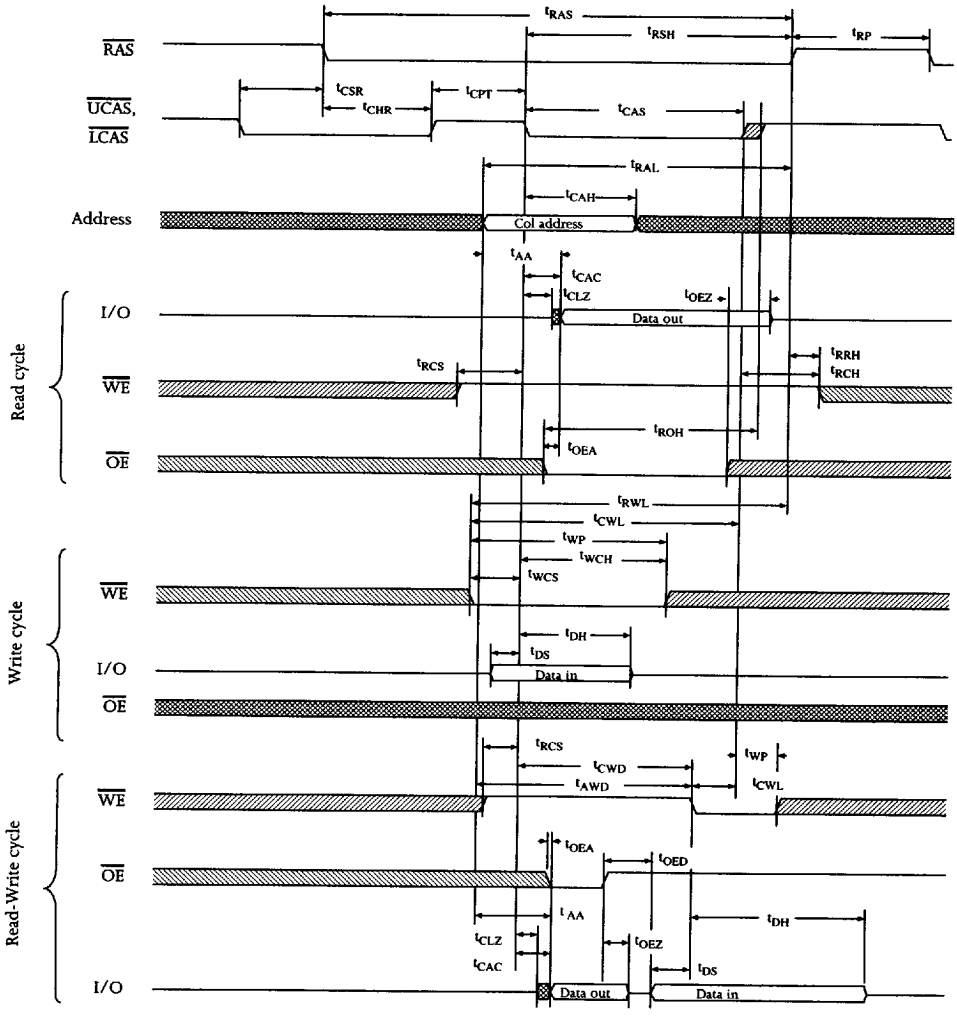
Hidden refresh waveform (read)



Hidden refresh waveform (write)

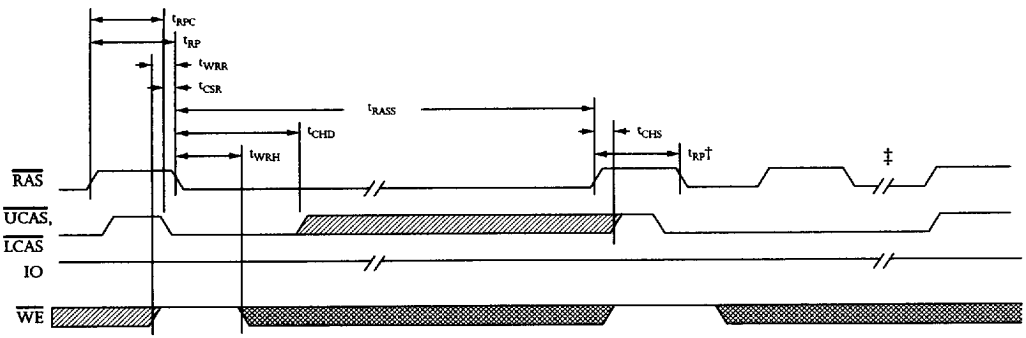


$\overline{CAS}$ before $\overline{RAS}$ refresh counter test waveform



Self refresh waveform

A0-A9; $\overline{OE}$ = don't care

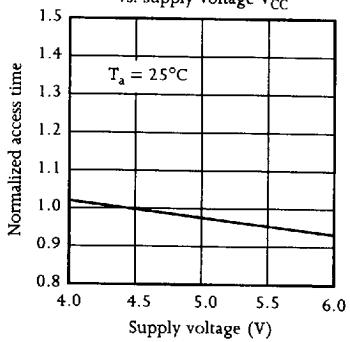


† Once t_{RASS} (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM enters self refresh mode.

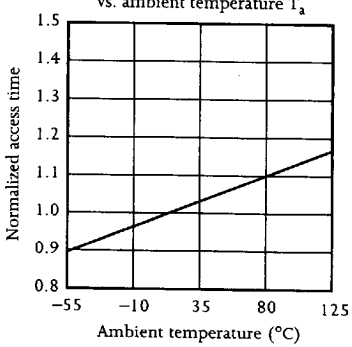
‡ Once t_{RPS} is satisfied, a complete burst of all rows should be executed.

Typical DC and AC characteristics

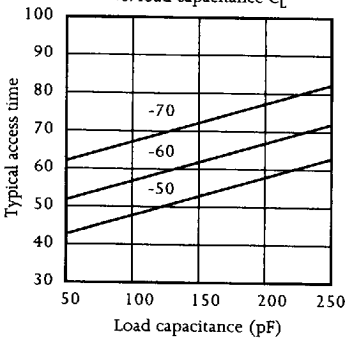
Normalized access time t_{RAC} vs. supply voltage V_{CC}



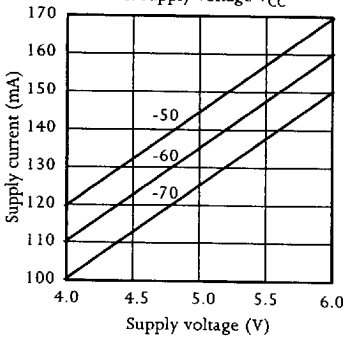
Normalized access time t_{RAC} vs. ambient temperature T_a



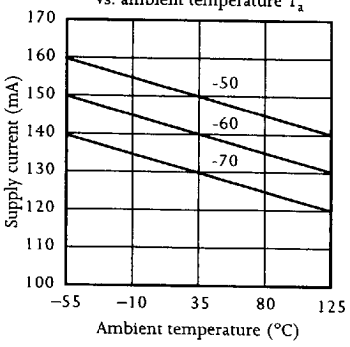
Typical access time t_{RAC} vs. load capacitance C_L



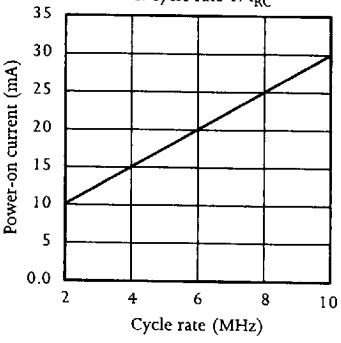
Typical supply current I_{CC} vs. supply voltage V_{CC}



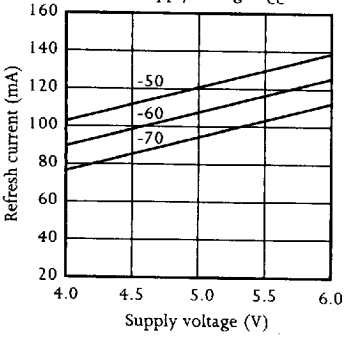
Typical supply current I_{CC} vs. ambient temperature T_a



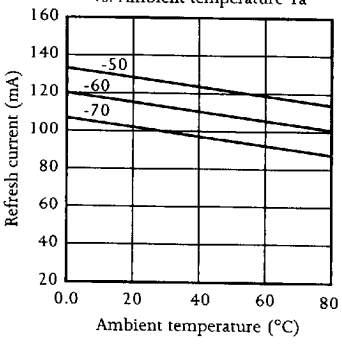
Typical power-on current I_{PO} vs. cycle rate $1/t_{RC}$



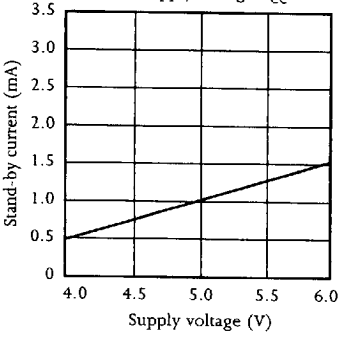
Typical refresh current I_{CC3} vs. supply voltage V_{CC}



Typical refresh current I_{CC3} vs. Ambient temperature Ta

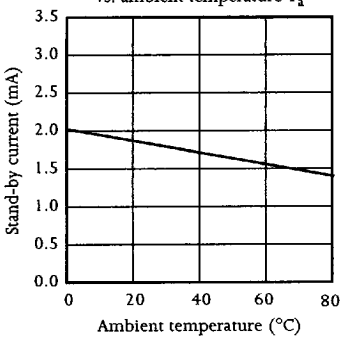


Typical TTL stand-by current I_{CC2} vs. supply voltage V_{CC}

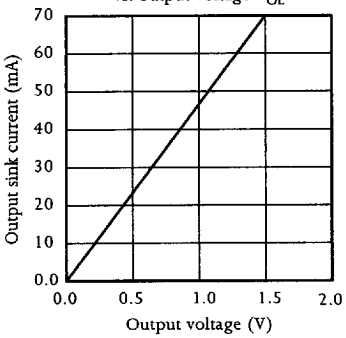


DRAM

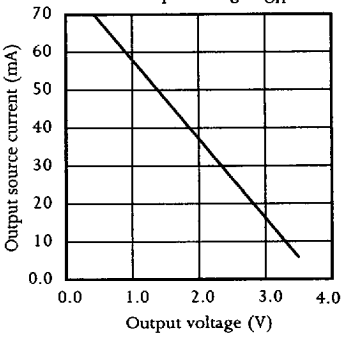
Typical TTL stand-by current I_{CC2} vs. ambient temperature T_a



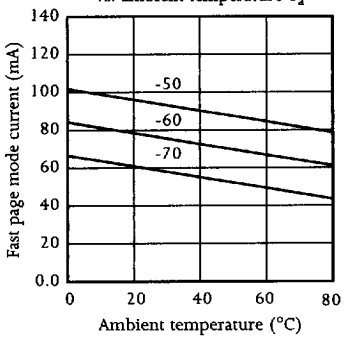
Typical output sink current I_{OL} vs. output voltage V_{OL}



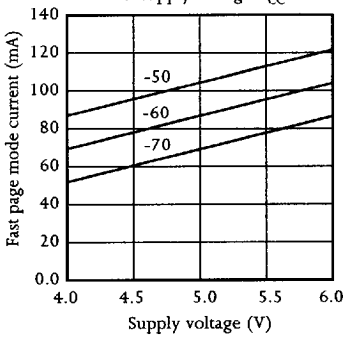
Typical output source current I_{OH} vs. output voltage V_{OH}



Typical fast page mode current I_{CC4} vs. ambient temperature T_a



Typical fast page mode current I_{CC4} vs. supply voltage V_{CC}



DRAM

Capacitance [15]

f = 1 MHz, T_a = Room temperature

Parameter	*Symbol*	*Signals*	*Test conditions*	*Max*	*Unit*
Input capacitance	C_{IN1}	A0 to A8	V_{in} = 0V	5	pF
	C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	7	pF
I/O capacitance	$C_{I/O}$	I/O0 to I/O15	V_{in} = V_{out} = 0V	7	pF

AS4C1M16E0 ordering information

Package \ RAS access time		50 ns	60 ns	70 ns
Plastic SOJ, 400 mil, 42-pin	5V	AS4C1M16E0-50JC	AS4C1M16E0-60JC	–
	3.3V	–	AS4LC1M16E0-60JC	AS4LC1M16E0-70JC

Shaded areas contain advance information.

AS4C1M16E0 part numbering system

AS4C	X	1M16E0	–XX	X	C
DRAM prefix	C = 5V CMOS LC = 3.3V CMOS	Device number	$\overline{\text{RAS}}$ access time	Package: J = 42-pin SOJ 400 mil	Commercial temperature range, 0°C to 70 °C