DAC-888

BYTEDAC® 8-BIT HIGH-SPEED "MICROPROCESSOR COMPATIBLE" MULTIPLYING D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- **8-Bit Level Triggered Latch**
- **8-Bit μP Compatible**
- **Easily Interfaced to All 8-Bit Processors**
- **TTL Logic Compatible**
- **$\overline{CE}$ and $\overline{WR}$ Inputs**
- **High Output Impedance and Compliance**
- **Proven DAC-08 Analog Flexibility and Reliability**
- **Nonlinearity to ±0.1% Max**
- **Low Power Dissipation 134mW**
- **Available in Die Form**

ORDERING INFORMATION †

NL %FS	PACKAGE INDUSTRIAL TEMPERATURE
0.1	DAC888EX
0.19	DAC888FX

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

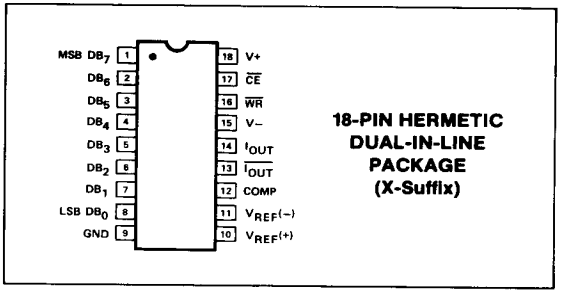
GENERAL DESCRIPTION

The BYTEDAC® DAC-888 is a buffered 8-bit digital-to-analog converter designed specifically for 8-bit bus oriented systems. The data inputs are connected to level-triggered latches. Two active-low control pins are provided for ease of interface to virtually all available microprocessors. The latches may also be operated in a transparent mode by holding both control pins low. Additionally, the DAC-888 has a data hold time requirement of zero nanoseconds.

The Analog section consists of a "Field-Proven" DAC-08 D/A Converter. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates full-scale adjustment in most applications.

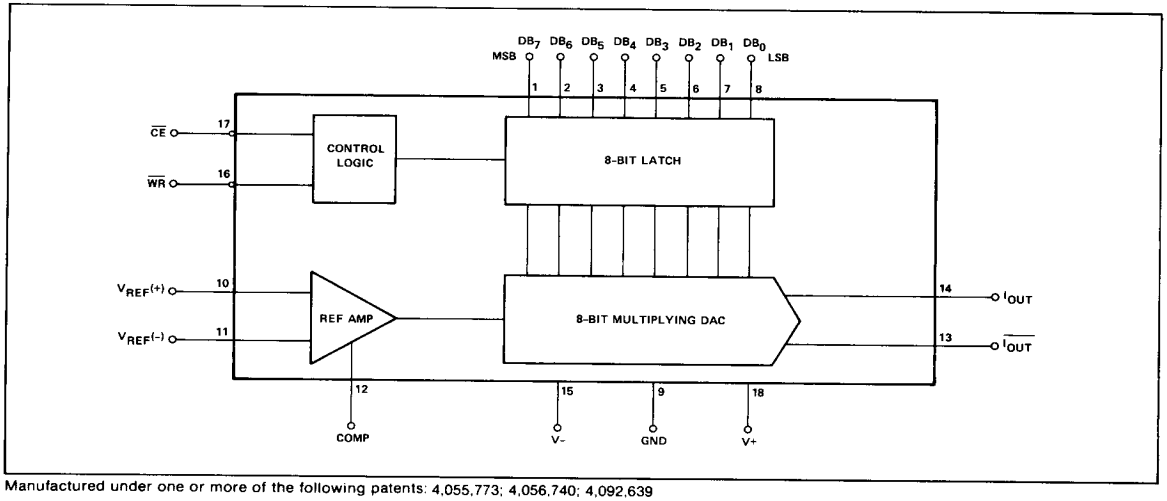
DAC-888 applications include graphic display drivers, high-speed modems, A/D converters, programmable waveform generators and power supplies, analog meter drivers, audio encoders and programmable attenuators; and other applications where low cost, high speed and buffered flexibility are required.

PIN CONNECTIONS



18-PIN HERMETIC DUAL-IN-LINE PACKAGE (X-Suffix)

FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

11 DIGITAL-TO-ANALOG CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... –25°C to +85°C
Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V– Supply 18.1V
Logic Inputs ..... 0V to 5.5V
Analog Current Outputs ..... –5mA
Reference Inputs (V_{10} to V_{11}) ..... V– to V+
Reference Input Differential Voltage
(V_{10} to V_{11}) ..... ±15V
Reference Input Current 5mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	79	11	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at V+ = +5V, V– = –12V, I_{REF} = 2mA, unless otherwise noted. T_A = +25°C to +85°C apply for DAC-888E/F. Output characteristics refer to both I_{OUT} and $I_{\overline{OUT}}$.

			DAC-888E			DAC-888F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution			8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	Bits
Nonlinearity	NL		—	—	±0.1	—	—	±0.19	%FS
Full-Scale Tempco	TCI_{FS}	See note 1	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB	-5	—	+5	-5	—	+5	V
Output Impedance	R_{OUT}		—	>20	—	—	>20	—	MΩ
Full Range Current	I_{FR}	V_{REF} = 10.000V R_{11}, R_{10} = 5.000kΩ T_A = 25°C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR14} - I_{FR13}$	—	±1	±8	—	±1	±8	µA
Zero-Scale Current	I_{ZS}		—	0.2	2	—	0.2	2	µA
Output Current Range	I_{FSR}	I_{REF} = 3mA	2.1	2.9	—	2.1	2.9	—	mA
Reference Bias Current	I_B		—	–1	–3	—	–1	–3	µA
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V– = –10.8V to –13.2V I_{REF} = 1mA	— —	±0.0003 ±0.0002	±0.01 ±0.01	— —	±0.0003 ±0.0002	±0.01 ±0.01	$\%\Delta I_{FS}/\%\Delta V+$ $\%\Delta I_{FS}/\%\Delta V-$
Power Supply Current	I+ I–	I_{REF} = 2mA	— —	12 6	16 9	— —	12 6	16 9	mA
Power Dissipation	P_d	I_{REF} = 2mA	—	134	190	—	134	190	mW
Logic Input Levels Logic Input "0" Logic Input "1"	 V_{IL} V_{IH}		 — 2	 — —	 0.8 —	 — 2	 — —	 0.8 —	V
Logic Input Current Logic Input "0" Logic Input "1"	 I_{IL} I_{IH}	 V_{IN} = 0V V_{IN} = 5.25V	 — —	 2 0.1	 -10 1	 — —	 2 0.1	 -10 1	µA

NOTE: Guaranteed by design.

ELECTRICAL CHARACTERISTICS — A.C. PARAMETERS $V_S = +5V, -12V, I_{REF} = 2mA, T_A = 25°C$.

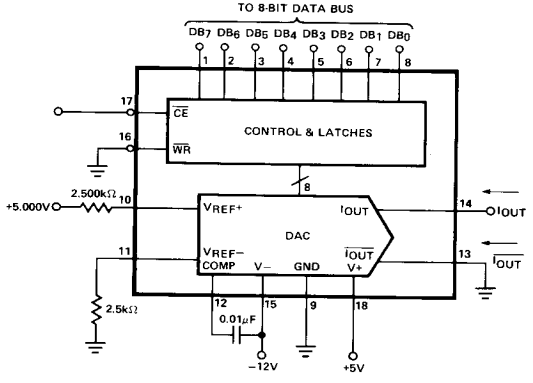
PARAMETER	SYMBOL	CONDITIONS	DAC-888E MIN	DAC-888E TYP	DAC-888E MAX	DAC-888F MIN	DAC-888F TYP	DAC-888F MAX	UNITS
Settling Time	t_S	From $\overline{CE}$ & $\overline{WR}$ Negative Level to ±1/2LSB, All Bits Switched ON or OFF, (See note)	—	300	400	—	300	400	ns
Reference Input Slew Rate	dI/dt	(See Note)	4	8	—	4	8	—	mA/μs
Data Input Setup Time	t_{DS}	(See note)	150	—	—	150	—	—	ns
Data Input Hold Time	t_{DH}	(See note)	10	—	—	10	—	—	ns
Chip Enable/Write Pulse Width	t_{ENW}	(See note)	250	—	—	250	—	—	ns

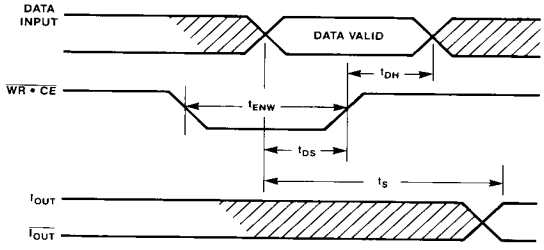
NOTE: Guaranteed by design.

DAC-888 PIN DESCRIPTION

SYMBOL	DESCRIPTION	
DB_0 - DB_7	DATA BIT — Bits 0-7 are digital, active-high inputs. DB_7 is assigned as the MSB.	PINS 1-8
$\overline{CE}$	CHIP ENABLE — An active low input control which is the device enable input terminal.	PIN 17
$\overline{WR}$	WRITE CONTROL — An active low control which enables the microprocessor to write data to the DAC.	PIN 16
I_{OUT} • $\overline{I_{OUT}}$	CURRENT OUTPUT — Complementary current outputs, which when added, equal I_{FS}.	PINS 13-14
V_{REF+}, V_{REF-}	VOLTAGE REFERENCE — Differential inputs that accept a negative, positive, or bipolar input and are used to set I_{FS}.	PINS 10-11
COMP	COMPENSATION — The reference amplifier frequency compensating terminal.	PIN 12

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 8-BIT OPERATION



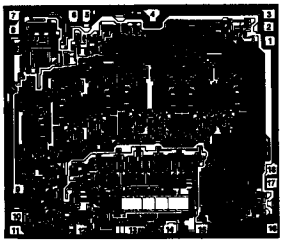


NOTE: IF INPUT DATA CHANGES AFTER ($\overline{WR} \bullet \overline{CE}$) LOW AND BEFORE ↑($\overline{WR} \bullet \overline{CE}$) HIGH − t_{DS}↓, I_{OUT}/$\overline{I_{OUT}}$ WILL CHANGE. THE LAST DATA BEFORE ↑($\overline{WR} \bullet \overline{CE}$) HIGH − t_{DS}↓ WILL BE LATCHED PROVIDED DATA VALID IS HELD FOR ($t_{DS\,(MIN)}$ − $t_{DH\,(MIN)}$).

OPERATION TABLE

$\overline{CE}$	$\overline{WR}$	OUTPUT
I	X	NO CHANGE
O	I	NO CHANGE
O	O	UPDATE LATCHES (TRANSPARENT)

DICE CHARACTERISTICS



DIE SIZE 0.141 × 0.127 inch, 17, 907 sq. mils
(3.58 × 3.23 mm, 11.56 sq. mm)

1. DB7 (MSB)
2. DB6
3. DB5
4. DB4
5. DB3
6. DB2
7. DB1
8. DB0 (LSB)
9. GROUND
10. V_{REF} (+)
11. V_{REF} (−)
12. COMP
13. $\overline{I_{OUT}}$
14. I_{OUT}
15. V−
16. $\overline{WR}$
17. $\overline{CE}$
18. V+

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at V_S = +5, −12V, I_{REF} = 2mA, T_A = 25° C, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-888N LIMIT	DAC-888G LIMIT	UNITS
Resolution			8	8	Bits MIN
Monotonicity			8	8	Bits MIN
Nonlinearity			±0.1	±0.19	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB R_{OUT} > 20MΩ Typ.	+5 −5	+5 −5	V MAX V MIN
Full Range Current	I_{FR14}	V_{REF} = 10.000V R_{11}, R_{10} = 5.000kΩ T_A = 25°C	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full Range Symmetry	I_{FRS}	I_{FR14}-I_{FR13}	±8	±8	μA MAX
Zero-Scale Current	I_{ZS}		2	2	μA MAX
Output Current Range	I_{FSR}	I_{REF} = 3mA	2.1	2.1	mA MIN
Reference Bias Current	I_B		−3	−3	μA MAX
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V− = −10.8V to −13.2V, I_{REF} = 1mA	±0.01 ±0.01	±0.01 ±0.01	$\%\Delta/_{FS}/\%\Delta V+$ MAX $\%\Delta/_{FS}/\%\Delta V-$ MAX
Power Supply Current	I+ I−	I_{REF} = 2mA	16 9	16 9	mA MAX
Power Dissipation	P_d	I_{REF} = 2mA	190	190	mW MAX
Logic Input Levels Logic Input "0" Logic Input "1"	 V_{IL} V_{IH}		 0.8 2	 0.8 2	 V MAX V MIN
Logic Input Current	I_{IL} I_{IH}	V_{IN} = 0V V_{IN} = 5.25V	−10 1	−10 1	μA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS V+ = +5V, −12V, I_{REF} = 2mA, T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-888 TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8.0	mA/μs
Settling Time	t_S	From $\overline{CE}$ Negative Edge to ±1/2 LSB, All bits Switched ON or OFF	300	ns
Data Input Setup Time	t_{DS}		100	ns
Data Input Hold Time	t_{DH}		0	ns
Chip Enable Write Pulse Width	t_{ENW}		200	ns

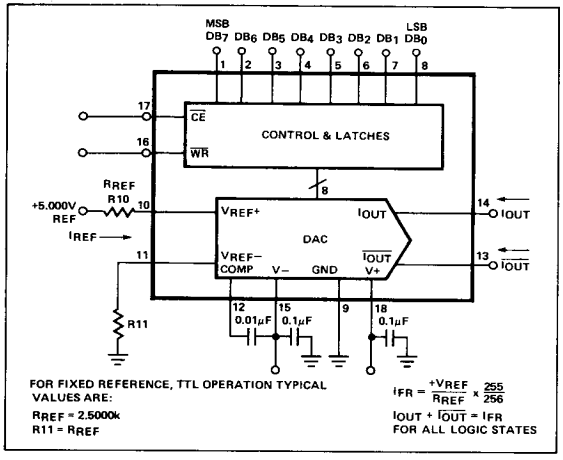
DIGITAL INFORMATION

The BYTEDAC® DAC-888 is a monolithic microprocessor compatible D/A converter consisting of an 8-bit level triggered latch, control circuitry and one 8-bit multiplying D/A converter housed in an 18-pin dual in line package (DIP).

The DAC-888 accepts 8-bit binary bytes at the data inputs. Data access is accomplished when $\overline{WR}$ and $\overline{CE}$ are low. During the low state of $\overline{CE}$ and $\overline{WR}$, the latches are transparent, therefore, data should be valid from 100ns prior to $\overline{WR}$ and $\overline{CE}$ low until $\overline{CE}$ or $\overline{WR}$ high. When $\overline{CE}$ or $\overline{WR}$ goes high, the data stored in the latches will hold the selected output indefinitely.

ANALOG INFORMATION

BASIC POSITIVE REFERENCE OPERATION



REFERENCE AMPLIFIER SET-UP

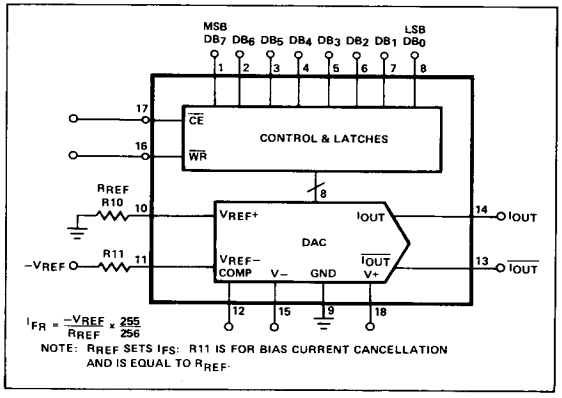
The DAC-888 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly 0 to +4.0mA. The full range output currrent is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = 1_{10}$$

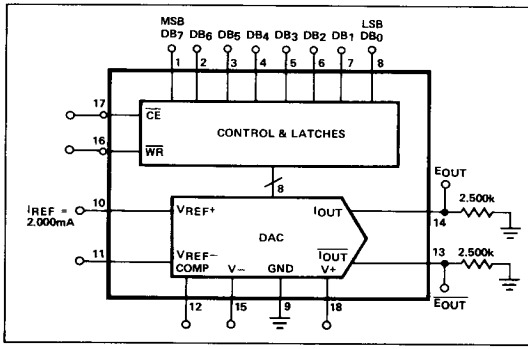
In positive reference applications, an external positive reference voltage current flows through R_{10} into the $V_{REF(+)}$ terminal of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$; reference current flows from ground through R_{10} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 11. The voltage at pin 10 is equal to and tracks the voltage at pin 11 due to the high gain of the internal reference amplifier. R_{11} (nominally equal to R_{10}) is used to cancel bias current errors; R_{11} may be eliminated with only a minor increase in error.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{10} or by using a potentiometer for R_{10}. An improved method of full-scale trimming which eliminates potentio-

BASIC NEGATIVE REFERENCE OPERATION

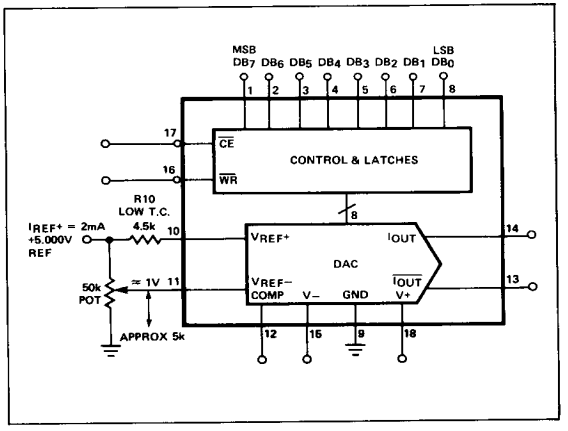


BASIC UNIPOLAR NEGATIVE OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL-SCALE	1	1	1	1	1	1	1	1	1.992	0.000	-4.980	0.000
FULL-SCALE -1 LSB	1	1	1	1	1	1	1	0	1.984	0.008	-4.960	-0.020
HALF-SCALE +1 LSB	1	0	0	0	0	0	0	1	1.008	0.984	-2.520	-2.460
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	0.992	-2.500	-2.480
HALF-SCALE -1 LSB	0	1	1	1	1	1	1	1	0.992	1.000	-2.480	-2.500
ZERO-SCALE +1 LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.020	-4.960
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	1.992	-0.000	-4.980

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



meter TC effects is shown in the Recommended Full Scale Adjustment Circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 12 to V−. For fixed reference operation a 0.01μF capacitor is recommended. For variable reference applications, see "Reference Amplifier Compensation for Multiplying Applications" section.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 12 to V−. The value of this capacitor depends on the impedance presented to pin 10 (see Table 1).

TABLE 1. REFERENCE AMPLIFIER COMPENSATION

REF. INPUT RESISTANCE	SUGGESTED C_C
1kΩ	15pF
2.5kΩ	37pF
5kΩ	75pF

NOTE: A 0.01μF capacitor is suggested for fixed references.

For fastest response to a pulse, low values of R_{10}, enabling small C_C values, should be used. If pin 10 is driven by a high current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{10} = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs, enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns (see Figure, pulsed reference operation).

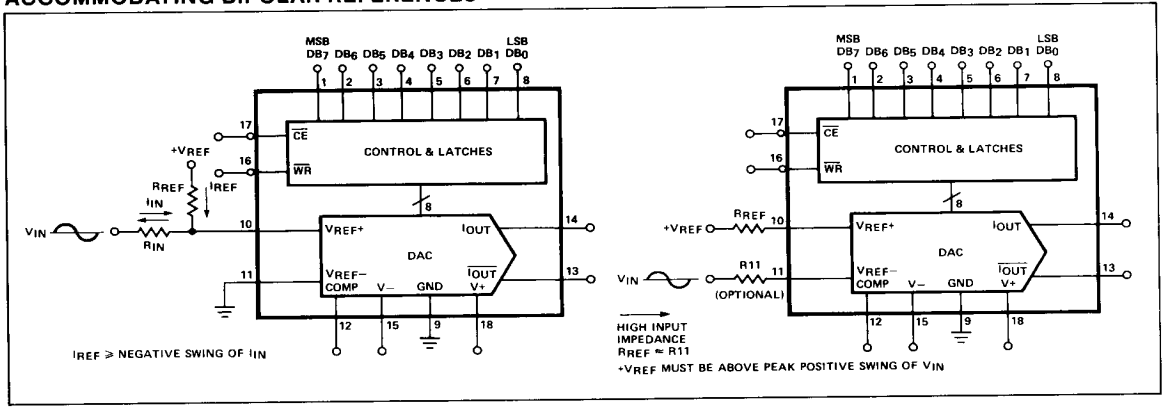
Bipolar references may be accommodated by offsetting V_{REF} or pin 11, as shown in Figure below. The negative common-mode range of the reference amplifier is given by V_{CM} = V− plus (I_{REF} X 1kΩ) plus 2.5V. The positive common-mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL Logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{10} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

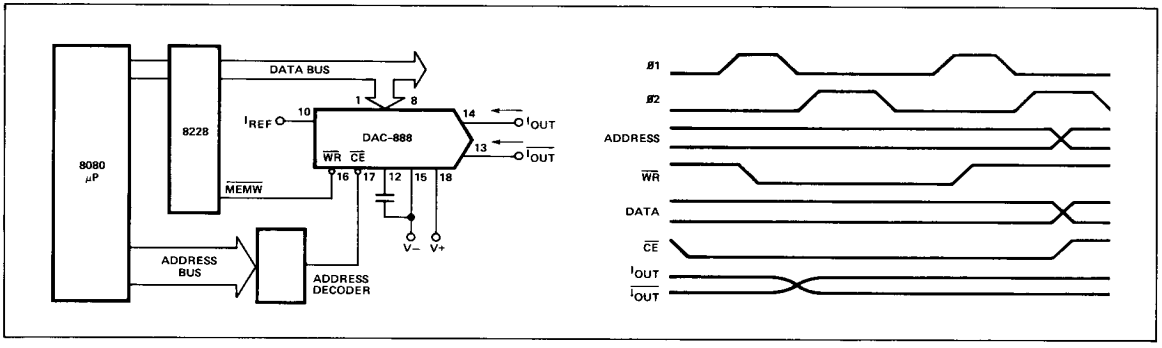
ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 14 increases proportionally in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 14 and turned on at pin 13. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

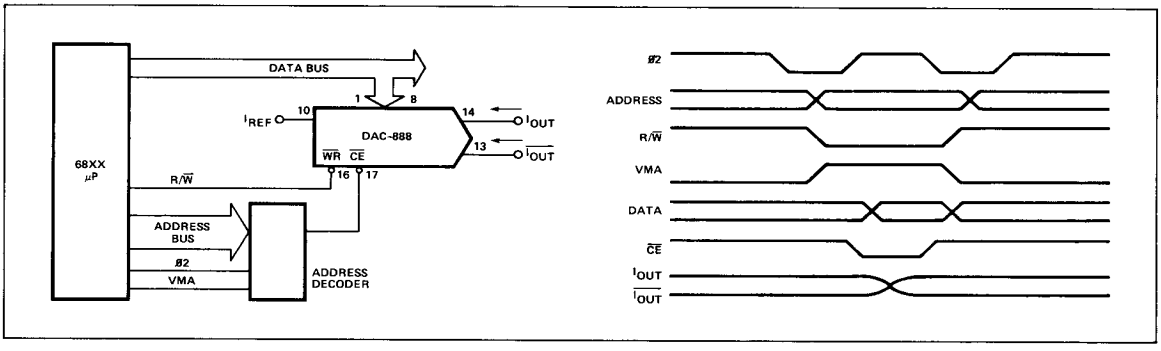
ACCOMMODATING BIPOLAR REFERENCES



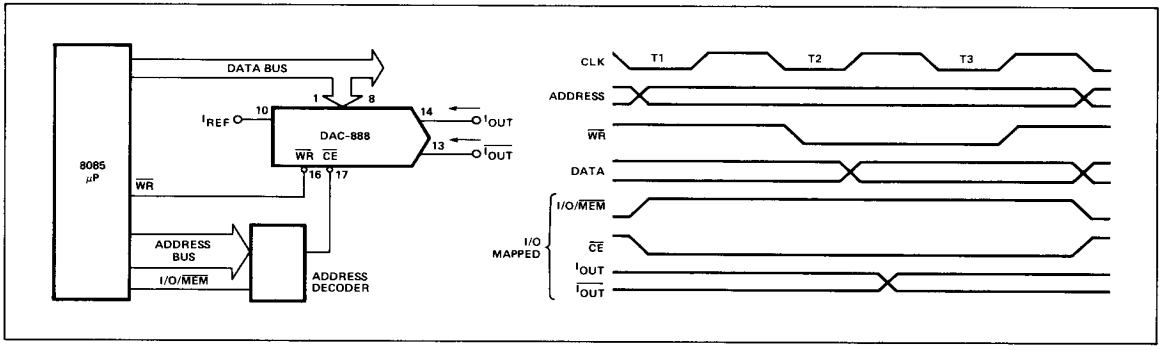
8080 INTERFACE



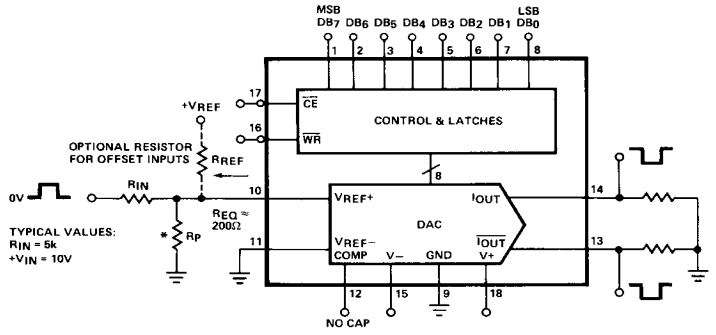
6800, 6801, 6809 INTERFACE



8085 INTERFACE

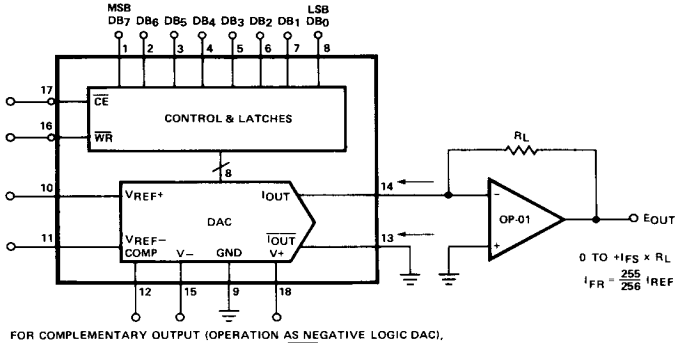


PULSED REFERENCE OPERATION



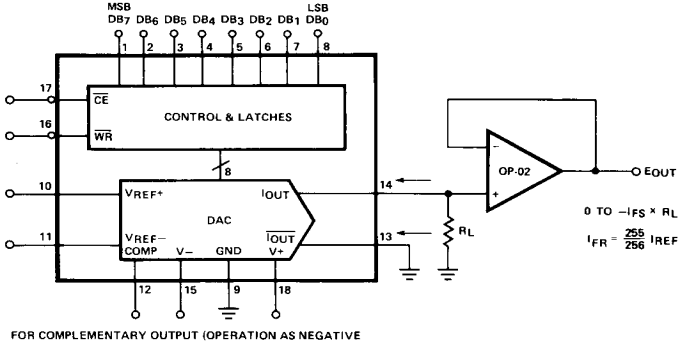
*UNBALANCED INPUTS WILL CAUSE SLIGHT DEGRADATION OF I_{FS} ACCURACY DUE TO I_{OS} OF REFERENCE AMPLIFIER.

POSITIVE LOW IMPEDANCE OUTPUT OPERATION



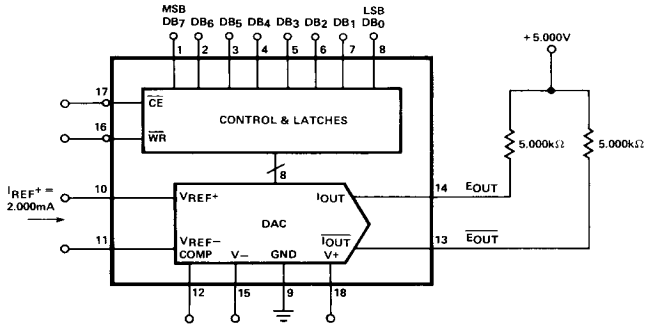
FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP AMP TO $\overline{I_{OUT}}$. CONNECT I_{OUT} TO GROUND.

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



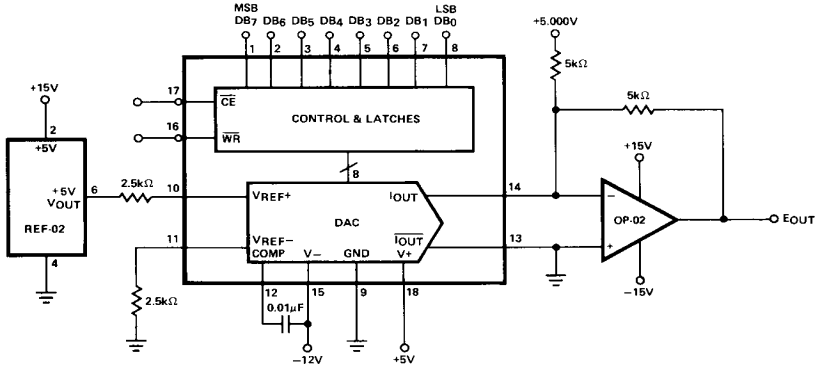
FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC,) CONNECT NONINVERTING INPUT OF OP AMP TO $\overline{I_{OUT}}$. CONNECT I_{OUT} TO GROUND.

BASIC BIPOLAR OUTPUT OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O	$\overline{E_O}$
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	−4.960	5.000
POSITIVE FULL-SCALE −1 LSB	1	1	1	1	1	1	1	0	−4.920	4.960
ZERO-SCALE +1LSB	1	0	0	0	0	0	0	1	−0.040	0.080
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	0.040
ZERO-SCALE −1LSB	0	1	1	1	1	1	1	1	0.040	0.000
NEGATIVE FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	4.900	−4.920
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	5.000	−4.960

OFFSET BINARY OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	4.960
POSITIVE FULL-SCALE −1LSB	1	1	1	1	1	1	1	0	4.920
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEGATIVE ZERO-SCALE +1LSB	0	0	0	0	0	0	0	1	−4.960
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

BASIC BIPOLAR OUTPUT OPERATION

Both outputs have an extremely wide voltage compliance, enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 18V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} X 1kΩ) plus 2.5V.

POWER SUPPLIES

The DAC-888 operates over a wide range of power supply voltages from a total supply of 9V to 15V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-888 is quite insensitive to variations in supply voltage.

Power consumption may be calculated as follows:

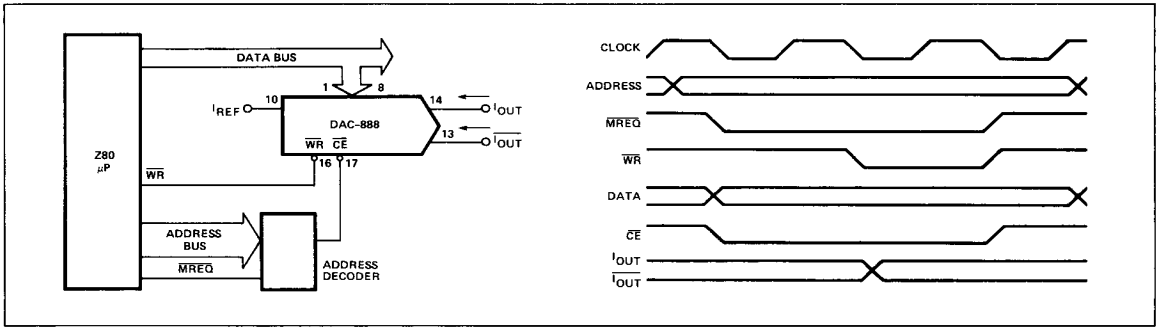
$P_d = (I+)(V+) + (I-)(V-)$.

TEMPERATURE PERFORMANCE

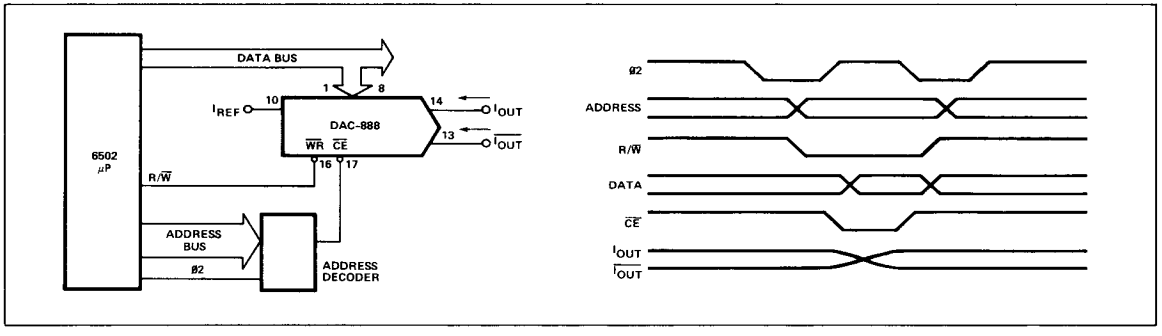
The nonlinearity and monotonicity specifications of the DAC-888 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{10} should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-888 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

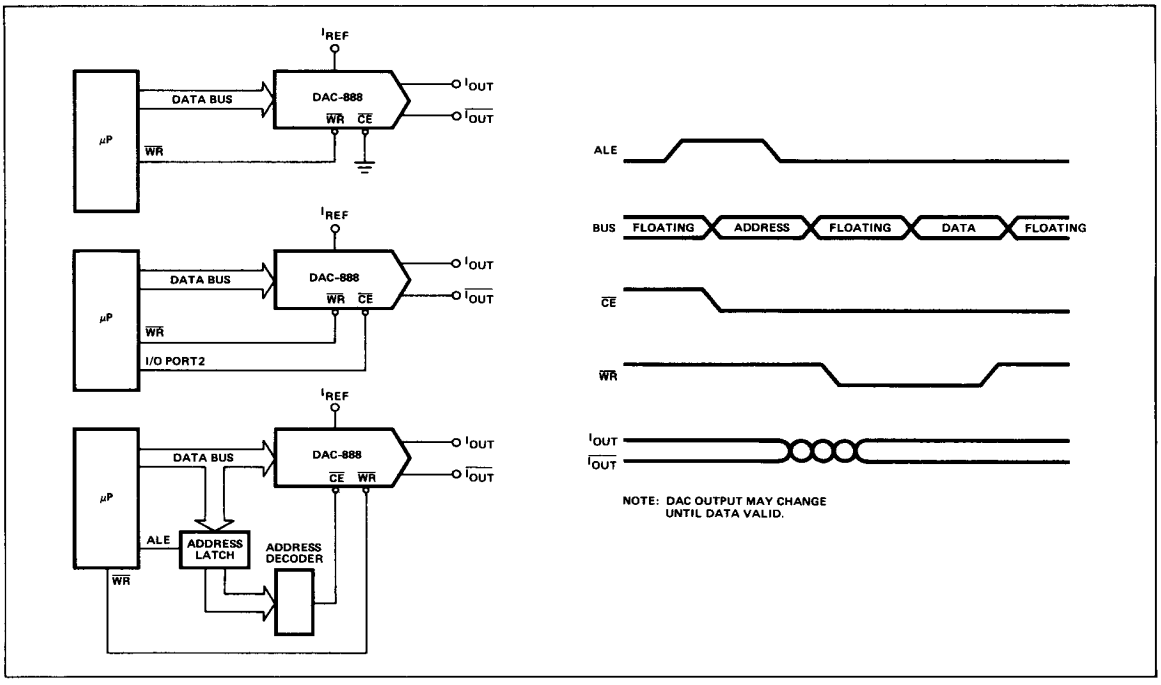
Z-80 INTERFACE



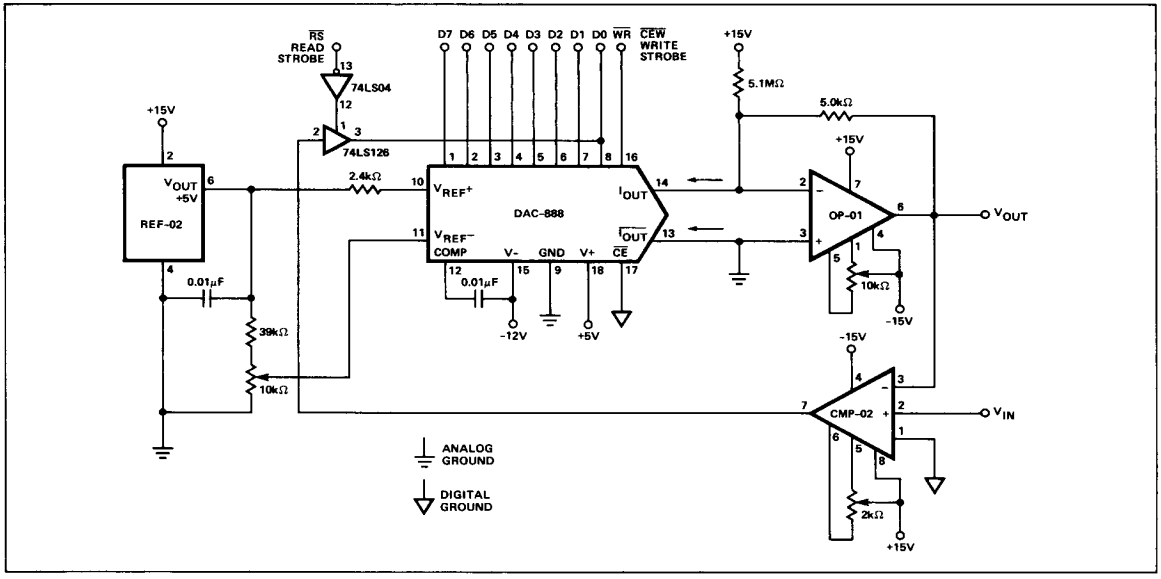
6502 INTERFACE



8048 INTERFACE



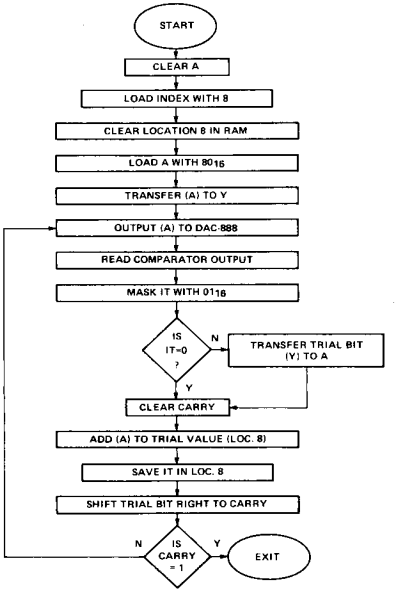
'SOFTWARE SAR' A/D CONVERTER (WITH 8048 MICROPROCESSOR)



SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERSION PROGRAM LISTING USING DAC-888 AND SYM 1 PCB WITH 6502μP WITH FLOW CHART

LOCATION	DATA	MNEMONIC	COMMENTS
500	A9 00	LDA #00	Clear
502	A2 08	LDX #08	Set Index Register
504	95 00	STA ,X	Clear Memory at 08_H
506	A9 80	LDA #80	Trial Bit
508	A8	TAY	TO Y
509	8D 00 10	STA 1000 (Cont.)	Output
50C	AD 00 1C	LDA 1C00	Read Comp.
50F	29 01	AND A, #01	Mask it
511	F0 01	BEQ * +1	Branch if CMP = 0
513	98	TYA	Get Trial Bit
514	18	CLC	Clear Carry
515	75 00	ADC ,X	Result Summed With Previous Test
517	95 00	STA ,X	Save it
519	98	TYA	Get Trial Value
51A	4A	LSR	Next Bit
51B	A8	TAY	Save it
51C	15 00	ORA ,X	Next Data
51E	90 E9	BCC *−23	Continue For 8 Trials
520	4C 00 05	JMP 500	Do Over

NOTE: 32 Bytes 260μs



BURN-IN CIRCUIT