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CCD Image Sensors

IA-D2 TURBOSENSOR™

IA-D2-0512, -1024 Series Area Image Sensor Arrays

T-41-55

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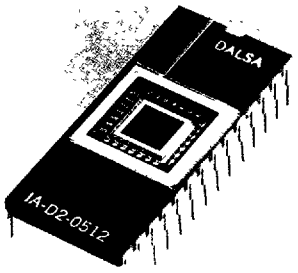
FEATURES

- **Up to 60 frames / second (max.)**
- **512x512 or 1024x1024 Elements**
- **Full Frame Architecture**
- **16 MHz Output Data Rate**
- **TURBOSENSOR™ technology**
- **10μm (H) x 10μm (V) Pixel Size**
- **3,000:1 Dynamic Range**
- **3 Phase BCCDs for Simple Operation**



DESCRIPTION

DALSA's IA-D2 area array image sensors use DALSA's TURBOSENSOR™ technology in a full frame transfer architecture to provide high output data rates of 16 MHz. The series is ideally suited for applications requiring maximum operating speed and high resolution, and employs three phase buried channel CCD readout shift registers to maximize output speed and reduce noise. The IA-D2 sensors use square pixels and a square imaging area of 512 x 512 or 1024 x 1024 elements. The dynamic range of the photoelements exceeds 3,000:1 and provides an output which is linear for all light levels.

DALSA also offers the CA-D2 cameras which use the IA-D2 series of image sensors.

APPLICATIONS

The IA-D2 series sensor is ideally suited for applications requiring maximum operating speed and high resolution. This sensor can be used for:

- **image processing**
- **machine-vision**
- **medical imaging**

The IA-D2 can also be operated in a time delay and integration (TDI) mode by operating the three phase imager clocks continuously. Normal production devices are characterized in full frame mode only.

For mechanical information regarding package size and tolerance, refer to package #50-01-28004 in **Optical and Mechanical Considerations of Sensors** on pp. 101-104 of this databook.

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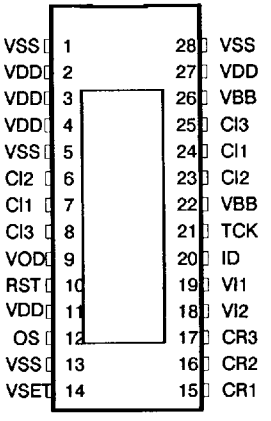
IA-D2-0512 PIN FUNCTIONAL DESCRIPTION

PIN	SYMBOL	NAME
1,5, 13, 28	VSS	Ground Reference
2, 3, 4, 11, 27	VDD	Amplifier Supply
6, 23	CI2	Image Region Clock, Phase 2
7, 24	CI1	Image Region Clock, Phase 1
8, 25	CI3	Image Region Clock, Phase 3
9	VOD	Output Node Drain Bias
10	RST	Output Node Reset Clock
12	OS	Analog Output Signal
14	VSET	Output Node Set Voltage
15	CR1	Readout Clock, Phase 1
16	CR2	Readout Clock, Phase 2
17	CR3	Readout Clock, Phase 3
18	VI2	Electrical Reference Pixel, Bias 2
19	VI1	Electrical Reference Pixel, Bias 1
20	ID	Electrical Reference Pixel Clock
21	TCK	Image to Readout Region Transfer Clock
22, 26	VBB	Substrate Bias



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Phone:(519)886-6000 Fax:(519)886-8023

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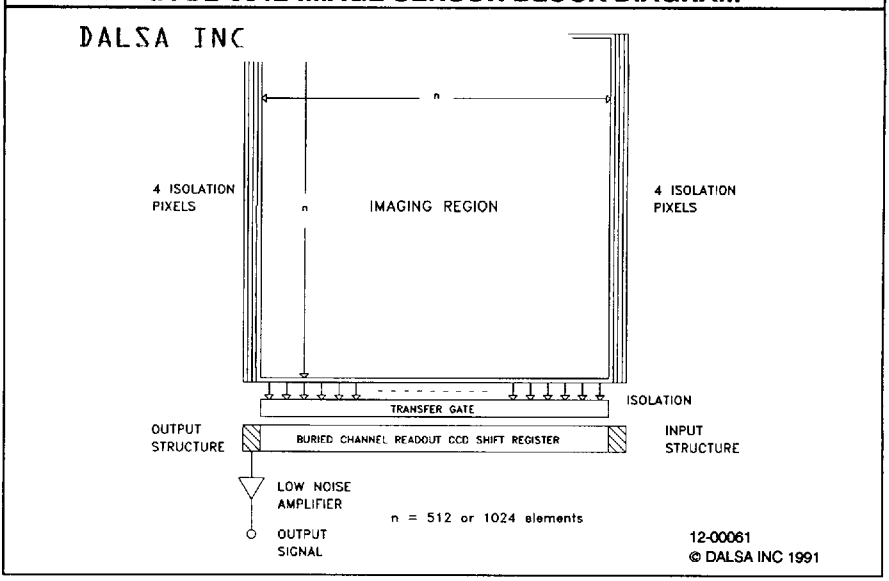
IA-D2-0512 IMAGE SENSOR BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

ORGANIZATION

The IA-D2 series area array image sensors use a full frame transfer organization with photogate photoelements. There is no on-chip storage region to block the light from the image plane during readout of the frame. In operation, a scene is imaged onto the imaging region during the integration period. Subsequently the scene is transferred into the readout shift register one line at a time until the entire image has been read out. When transfer from the imaging region to the readout shift register occurs, all light should be blocked. It is recommended that a mechanical shutter or a strobed light source be used for this purpose; however, a smear ratio of 100:1 (integration time to readout time) is usually sufficient to eliminate the need for shuttering in applications with a long integration period.

PHOTOELEMENTS

The area array consists of a square matrix of 512x512 or 1024x1024 valid photoelements for imaging plus an additional row of isolation pixels at the beginning and end of the frame. Each line of data has 4 extra pixels at each end to provide dark reference and isolation. Each pixel has a photosensitive area of 100 square micrometers and center to center spacing of 10 micrometers in both directions.

The photoelements are controlled by the image region clocks CI1, CI2 and CI3, and are organized to allow parallel transfer into the readout shift register. CI2 translates through TCK into CR1.

The TURBOSENSOR™ photogate photoelement offers ultra high speed operation and responds linearly with respect to input light intensity.

TRANSFER GATE

This gate controls the flow of light generated signal charge from the imaging region CCD into the readout CCD shift register. Specifically, TCK interfaces between CI2 of the image region and CR1 of the readout shift register.

Electrons from the image region are transferred when a high potential (equal to the high clock voltage) is applied to the transfer gate.

OUTPUT STRUCTURE

The signal charge packets from the readout shift register (CR3) are transferred serially, over the SET gate, to a floating sensing diffusion. As the signal charge is received, the corresponding potential on the diffusion is applied to the input of a two stage low noise amplifier structure, producing an output signal voltage (OS). The floating sensing diffusion is cleared of signal charge by the reset gate, driven by the reset clock (RST) in preparation for the subsequent signal charge packet.

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RECOMMENDED DC OPERATION

SIGNAL NAMES

The signal names assigned to the package pins describe both the function of the pin as well as the sense of input signals. DC (unclocked) bias and supply voltages are designated with signal names beginning with "V". Clocked signals begin with any other letter and are representative of the function of the pin.

SUPPLY VOLTAGES

VDD provides operating current to the on chip output amplifier and hence should be well regulated. The substrate, or bulk bias voltage, VBB, is negative with respect to ground in some applications. This low current bias should be well regulated. Since protection diodes are provided between many clock lines and the substrate, no clocks can be permitted to go below VBB. In most cases, VBB can be maintained at 0 volts (equal to VSS), although a negative VBB can reduce charge injection.

OUTPUT BIAS

A very low current DC gate bias, VSET, controls transfer of signal charge onto the output sensing diffusion. Charge is transferred from CR3 over VSET to the output node. Video becomes present on the falling edge of CR3. This voltage should be adjusted with a resistive divider to optimize output structure operation. If VSET is not optimized, single bright pixels will appear to "bleed" into adjacent pixels and could be mistaken for very poor CTE or crosstalk.

The shift register output drain voltage, VOD, is a bias provided to the output structure to discharge signal electrons after sensing. Both VSET and VOD are low current nodes.

INPUT STRUCTURE BIAS

Two reference voltages (VI1, VI2) may be used to create a reference output signal included in the output signal stream. These references are not used for most applications, but are available if necessary. When not used, the reference voltages VI1 and VI2 should be grounded. Both of these signals are low current nodes.

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IA-D2 DC OPERATING CONDITIONS

Recommended Operating Conditions at T_p = 25°C. (See notes)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Amplifier supply voltage	12.0	15.0	16.0	V
VBB	Substrate voltage	-3.0	0.0	0.0	V
VOD	Shift register drain voltage	10.0	13.0	16.0	V
VSET	Set Voltage	1.0	3.0	8.0	V
VI1	Input reference bias 1	0.0	2.0	8.0	V
VI2	Input reference bias 2	0.0	4.0	10.0	V

NOTES:

1. Voltages with respect to ground (VSS).
2. Tp is defined as the package temperature.
3. VI1, VI2 typically are grounded to disable reference.

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RECOMMENDED CLOCK OPERATION

PHOTOELEMENTS (IMAGE CLOCKS)

The three phase image clocks are the photosensitive elements in this device. These clocks, CI1, CI2 and CI3, control exposure and transfer signal charge from the image region to the readout shift register.

Signal charge electrons are photogenerated during the exposure period. During exposure, CI2 should be maintained high and CI1 and CI3 should be maintained low. This will provide for maximum uniformity.

Following exposure, CI1, CI2 and CI3 are clocked to move the lines of signal charge in parallel to the readout shift register. Charge transfers from CI2 into CI1. When a line of data is being read out, it is recommended that the imaging clocks remain constant. (i.e. not clocked). This will improve the quality of the video signal.

TRANSFER CLOCK

The transfer gate is controlled by the TCK signal. When TCK is pulsed high the pixel data is transferred from CI2 through TCK into the first phase (CR1) of the CCD readout shift register.

During integration, TCK pulses occur once per line, and transfer each line of the previous frame into the readout shift register.

READOUT CLOCKS

Three phase transport clocks (CR1, CR2, and CR3) are used to transfer data to the output structure. CR1 should be held high while the line of data is being transferred from the image region. Once a line has been transferred, the readout clocks should start cycling the current line of data towards the output structure.

Several clocking possibilities exist. It is important to maintain overlaps of adjacent phases and to ensure that all three clock phases are never all on or all off at the same time.

OUTPUT CONTROL CLOCKS

One output structure clock (RST) is required to clear the output node after sensing. This clock should go to a high voltage equal to the transport clock (CR) high voltages, and to a low of VSS. During RST high, the output will go to a reset level as shown in the clock diagrams.

OUTPUT SIGNAL

The output signal OS provides video data. The frequency of OS is equal to the frequency of the RST clock. The output signal is an AC waveform on a DC offset. Its is recommended that the video signal be buffered for current gain. After buffering, it is also recommended that the video signal be AC coupled.

IA-D2 CLOCK CHARACTERISTICS

Recommended Operating Conditions at T_p = 25°c.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{H(C)}$	Transport clock[1] HIGH	4.0	12.0	16.0	V
$V_{L(C)}$	Transport clock[1] LOW	0.0	0.0	0.5	V
$V_{H(TCK)}$	Transfer clock HIGH	4.0	12.0	16.0	V
$V_{L(TCK)}$	Transfer clock LOW	0.0	0.0	0.5	V
$V_{H(RST)}$	Reset clock HIGH	4.0	12.0	16.0	V
$V_{L(RST)}$	Reset clock LOW	0.0	0.0	0.5	V
$f_{(RST)}$	Reset frequency		10	16	MHz

NOTE:

1. Transport clocks include CI1, CI2, CI3, CR1, CR2 and CR3.

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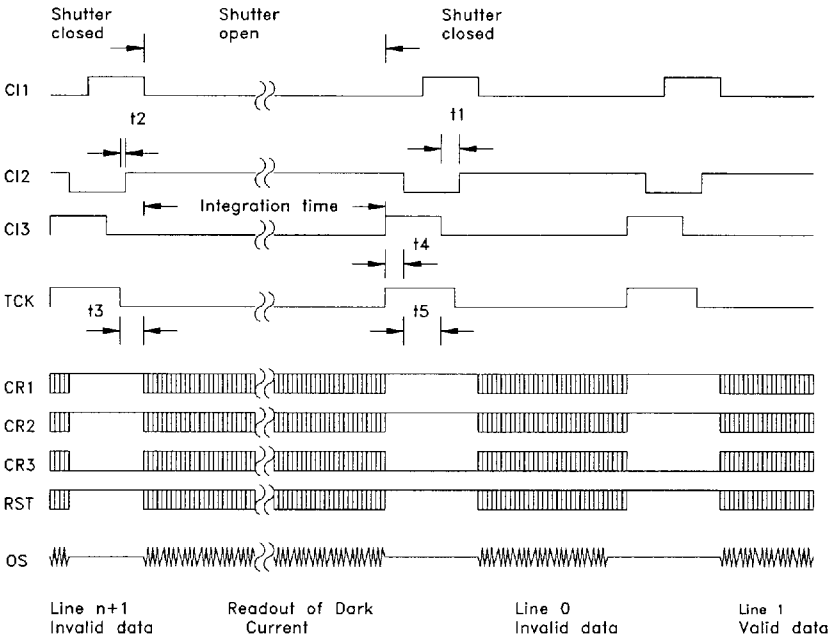
IA-D2 FRAME CLOCKING



NOTES:

t1: All overlaps CI1 - CI2, CI2 - CI3, CI3 - CI1 should have > 250 ns overlap.

t2: CI2 rising edge ≥ 100 ns after TCK falling edge.

t3: TCK falling edge ≥ 20 ns before CR1 falling edge.

t4: CI2 falling edge ≥ 100 ns after TCK rising edge.

t5: CI2 low, TCK high, CR1 high ≥ 100 ns.

Clocking is shown for a minimum frame of n + 2 lines.

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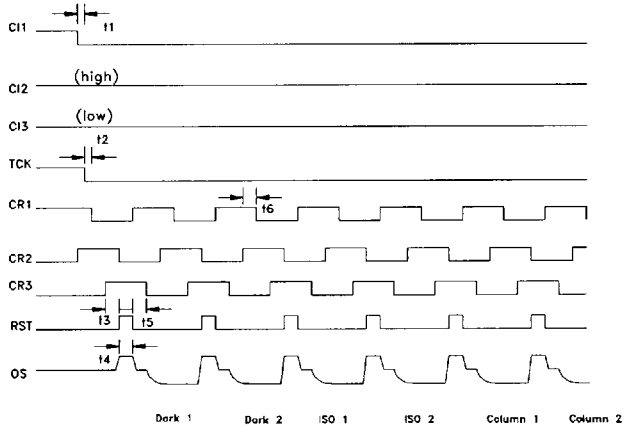
IA-D2 DETAILED DEVICE CLOCKING

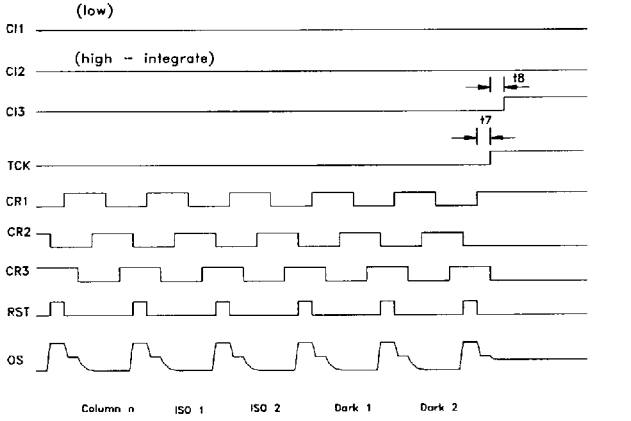
Beginning of Frame



NOTES

t1 : CI1 falling edge to TCK falling edge > 0 ns
t2: TCK falling edge to CR1 falling edge > 20 ns
t3 : CR3 rising edge to RST rising edge > 5 ns
t4 RST high period duration > 15 ns
t5: RST falling edge to CR3 falling edge > 5 ns
t6: Overlap between adjacent clocks on readout CCD > 10 ns

End of Frame



NOTES

t7 Rising edge of CR1 to rising edge of TCK > 0 ns
t8 - Rising edge of TCK to rising edge of CI3 > 0 ns

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IA-D2 PERFORMANCE CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Recommended Operating Conditions at Tp = 25°C. (See notes).				
Dynamic range[1]		3,000:1		
Noise Equivalent Exposure (NEE)		50		pJ/cm^2
Saturation Equivalent Exposure (SEE)[2]		150		nJ/cm^2
Responsivity[2]		2		V/μJ/cm^2
Saturation Output Amplitude (V_{SAT})[3]		300		mV
V_{NOISE}[4]				
Peak-Peak		0.5		mV
RMS		0.1		mV
FPN		15.0		mV
PRNU[5]		10		% V_{SAT}
CTE[6]	0.99990	0.99999	0.999999	
DC Output Offset		8		V
Storage Temperature (T_P)[7]	−70		+125	°C
Operating Temperature (T_P)[7]	−60		+90	°C

Notes:

1. Ratio of V_{SAT} to RMS Noise with reset noise eliminated through correlated double sampling (CDS).
2. Responsivity at peak Quantum Efficiency (near 700 nm).
3. Output amplitude with respect to dark reference level
4. Amplifier noise measured with reset noise eliminated through correlated double sampling (CDS).
5. PRNU is measured at approximately 50% V_{SAT} and is the difference between the pixels with the lowest and highest outputs, expressed as a percentage of V_{SAT}.
6. CTE is the measurement for a one stage transfer, measured at f_{RST} = 3.75 MHz.
7. T_P is package temperature.
8. See cosmetic specifications for this device.

Test Conditions:

1. All tests are done at f_{RST} = 3.75 MHz
2. Light Source QTH lamp with WBHM, unless otherwise noted.
3. VDD, VOD = 15 V; VBB = 0 V; Clock high voltage 12 V, low voltage 0 V, (includes CRx, Clx, CSx, TCK, RST as applicable); VSET as required for maximum V_{SAT} and CTE
4. All measurements exclude first and last 2 rows and columns.

IA-D2 ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Recommended Operating Conditions at Tp = 25°C.				
Output impedance		200		Ω
Amplifier supply current		15		mA
DC Bias Currents (VOD, VSET, VBB)			1	mA
Amplifier power dissipation	150	225	300	mW
Resistance to VBB				
Transport gate (CR1, CR2)		5		MΩ
Transfer gate		5		MΩ
Reset, Set gate		5		MΩ
Capacitance to VBB				
Transport clock (CR1, CR2)[1]		75		pF
Transfer clock (TCK)		25		pF
Imaging clock (Clx)		1200		pF
Reset (RST), Set (VSET) gate		12		pF

Notes:

1. Capacitance given for 512x512 element array.

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Optical and Mechanical Considerations of Sensors

Optical and Mechanical Considerations of DALSA CCD Image Sensors

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This applications note provides packaging information for the sensors listed in this databook. Please refer to the tables on the following pages for the critical dimensions of each image sensor series. For more information on a particular image sensor, please refer to the specific datasheet.

FIGURE 1. DIMENSIONS OF PACKAGE # 50-01-24005

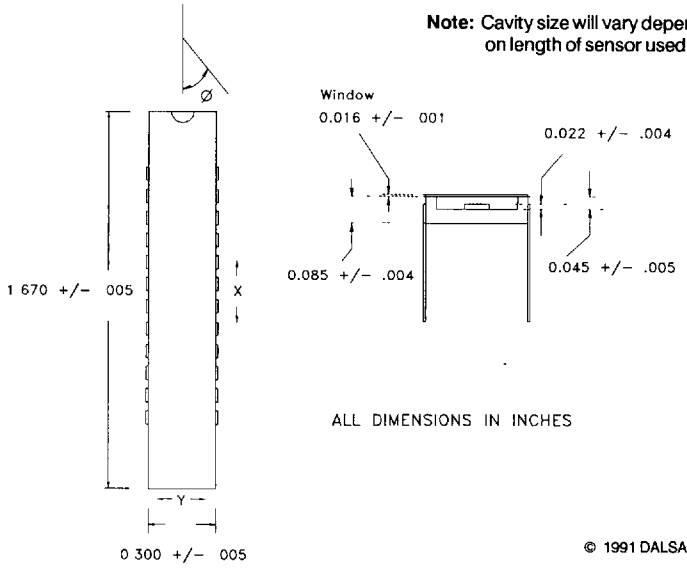

TABLE 1. PACKAGE # 50-01-24005 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-24005	IL-C3-0128	0.55 ± .09	0.15 ± .02	$0^{o} \pm 3.0^{o}$
50-01-24005	IL-C3-0256	0.55 ± .08	0.15 ± .02	$0^{o} \pm 2.5^{o}$
50-01-24005	IL-C3-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C2-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C9-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C4-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-C4-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-C5-2048	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-C5-4096	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-C6-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-E1-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-E1-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-E1-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-F2-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-F2-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-F2-2048	0.55 ± .04	0 15 ± .02	$0^{o} \pm 1.0^{o}$

Note: X = center imaging area to center pin 1 along package Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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Optical and Mechanical Considerations of Sensors

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FIGURE 2. DIMENSIONS OF PACKAGE # 50-01-40003

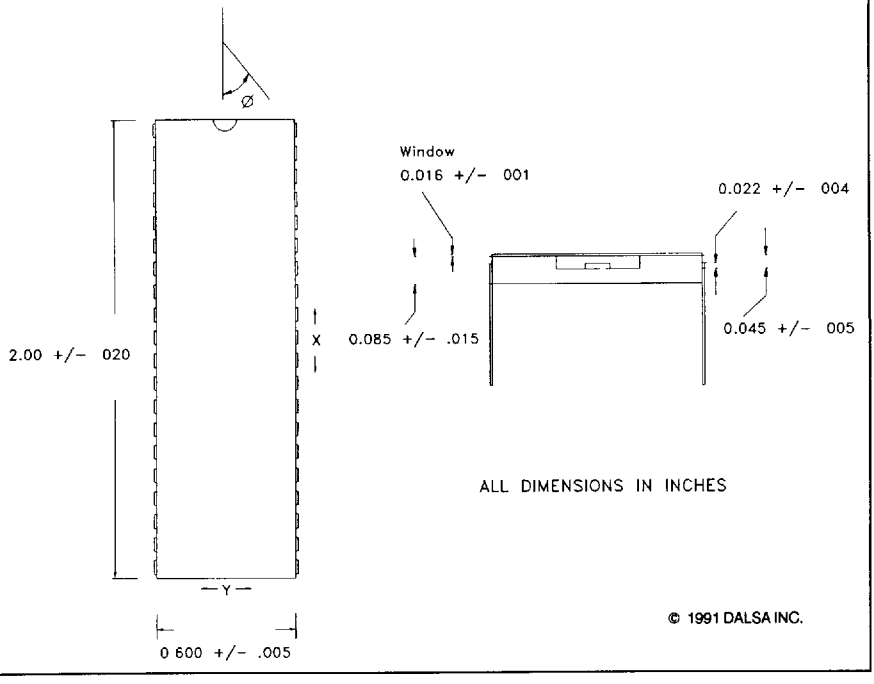

TABLE 2. PACKAGE # 50-01-40003 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-40003	IT-C5-2048	0.95 ± 0.1	0.3 ± 0.05	$0^{\circ} \pm 2.5^{\circ}$
50-01-40003	IT-C5-4096	0.95 ± 0.08	0.3 ± 0.03	$0^{\circ} \pm 1.5^{\circ}$
50-01-40003	IT-E1-1536	0.95 ± 0.08	0.3 ± 0 05	$0^{\circ} \pm 2.0^{\circ}$
50-01-40003	IT-E1-2048	0.95 ± 0.06	0.3 ± 0.05	$0^{\circ} \pm 1.5^{\circ}$
50-01-40003	IT-F2-2048	0.95 ± 0.06	0.3 ± 0.03	$0^{\circ} \pm 1.5^{\circ}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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Optical and Mechanical Considerations of Sensors

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FIGURE 3. DIMENSIONS OF PACKAGE # 50-01-24002

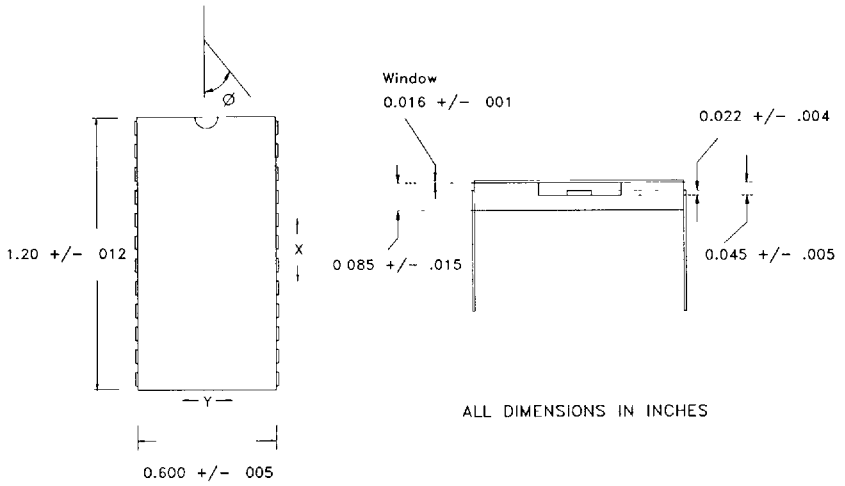

TABLE 3. PACKAGE # 50-01-40002 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-40002	IA-D1-0032	0.56 ± 0.12	0.3 ± 0.05	$0^{o} \pm 5.0^{o}$
50-01-40002	IA-D1-0064	0.57 ± 0.09	0.3 ± 0.04	$0^{o} \pm 4.0^{o}$
50-01-40002	IA-D1-0128	0.59 ± 0.12	0.3 ± 0.03	$0^{o} \pm 2.5^{o}$
50-01-40002	IA-D1-0256	0.71 ± 0.10	0.3 ± 0.03	$0^{o} \pm 1.5^{o}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation

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FIGURE 4. DIMENSIONS OF PACKAGE # 50-01-28004

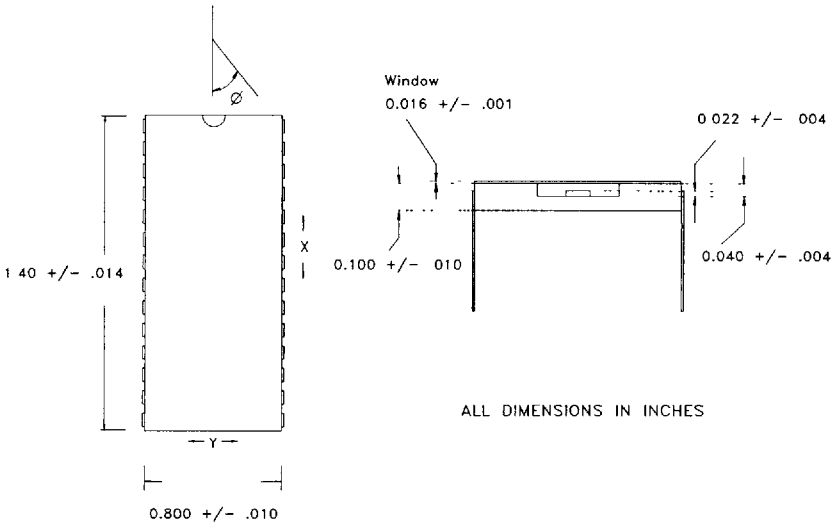

TABLE 4. PACKAGE # 50-01-28004 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-28004	IA-D2-0512	0.65 ± 0.08	0.4 ± 0.04	$0^{o} \pm 3.0^{o}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation