Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

T-46-23-08

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 12/15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 10/12/15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC, 20-pin SOJ, 20-pin CERPACK and 20-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

Access times as fast 10ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300 mil ceramic or plastic DIP, 20-pin CERPACK, 20-pin SOIC, 20-pin SOJ, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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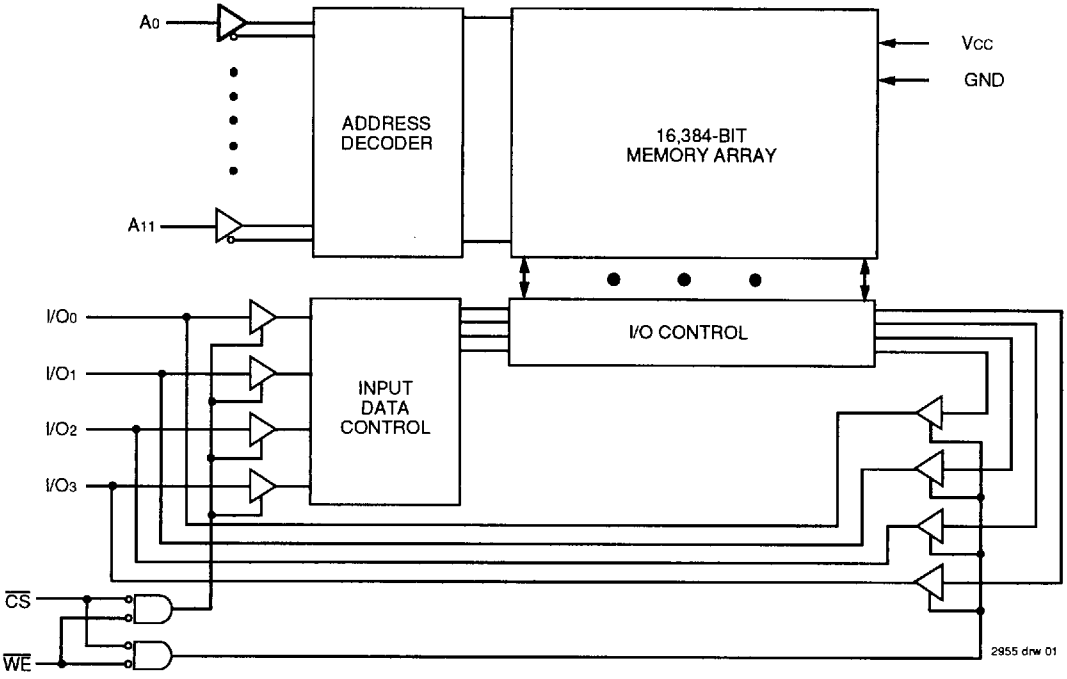
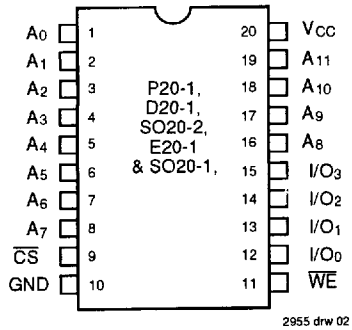
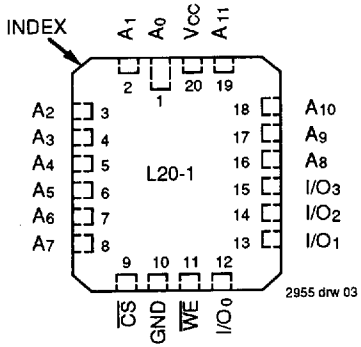
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK
TOP VIEW



LCC
TOP VIEW

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

2955 tbl 02

NOTE:
1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

2955 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTIONS

Name	Description
A0–A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O0-3	Data Input/Output
VCC	Power
GND	Ground

2955 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input HIGH Voltage	2.2	—	6.0	V
VIL	Input LOW Voltage	–0.5[1]	—	0.8	V

2955 tbl 05

NOTE:
1. VIL (min.) = –3.0V for pulse width less than 20ns, once per cycle.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

2955 tbl 04

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2955 tbl 06

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA10 Com'l.	6168SA10 Mil.	6168SA12[4] Com'l.	6168SA12[4] Mil.	6168SA15[4] Com'l.	6168SA15[4] Mil.	6168SA20 6168LA20 Com'l.	6168SA20 6168LA20 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	120	—	110	120	110	120	90	100	mA
		LA	—	—	—	—	—	—	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	175	—	165	175	145	165	120	120	mA
		LA	—	—	—	—	—	—	100	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	65	—	65	65	55	60	45	45	mA
		LA	—	—	—	—	—	—	30	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	20	—	20	20	20	20	20	20	mA
		LA	—	—	—	—	—	—	0.5	5	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25 Com'l.	6168SA25 6168LA25 Mil.	6168SA35 6168LA35 Com'l.	6168SA35 6168LA35 Mil.	6168SA45/55 6168LA45/55 Com'l.	6168SA45/55 6168LA45/55 Mil.	6168SA70[2] 6168LA70[2] Com'l.	6168SA70[2] 6168LA70[2] Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	110	120	100	110	—	110	—	110	mA
		LA	90	100	80	90	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	35	45	30	35	—	35	—	35	mA
		LA	25	30	20	25	—	25/20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	3	10	3	10	—	10	—	10	mA
		LA	0.5	0.3	0.5	0.3	—	0.3	—	0.3	

NOTES:
1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs are changing.
4. Military values are preliminary only.

2955 tbl 07

5

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6168SA Min.	IDT6168SA Max.	IDT6168LA Min.	IDT6168LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L	—	2	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L	—	2	—	2	
V_{OL}	Output LOW Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OL} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2955 tbl 08

DATA RETENTION CHARACTERISTICS (LA Version Only)

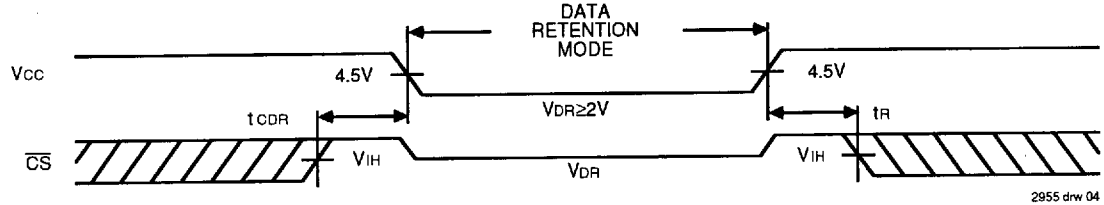
V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition		IDT6168LA Min.	IDT6168LA Typ.(1)	IDT6168LA Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	0.5(2)	100(2)	µA
			—	1.0(3)	150(3)		
			COM'L.	—	0.5(2)	20(2)	µA
			—	1.0(3)	30(3)		
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2955 tbl 09

NOTES:
1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2955 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2955 tbl 10

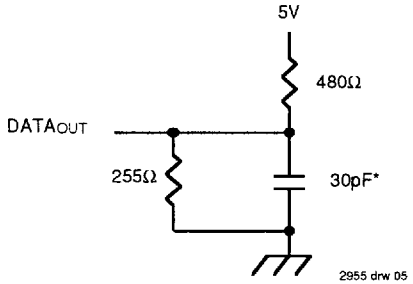


Figure 1. AC Test Load

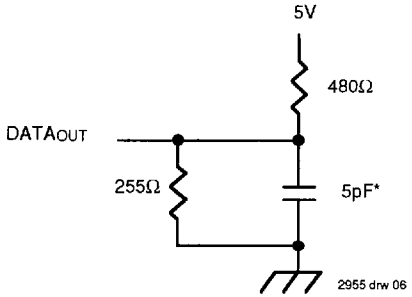


Figure 2. AC Test Load
(for tCHZ, tCLZ, tWHZ and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10(1) Min.	6168SA10(1) Max.	6168SA12 Min.	6168SA12 Max.	6168SA15 Min.	6168SA15 Max.	6168SA20/25 6168LA20/25 Min.	6168SA20/25 6168LA20/25 Max.	Unit
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20/25	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	20/25	ns
tCLZ	Chip Select to Output in Low-Z(3)	3	—	3	—	3	—	5	—	ns
tCHZ	Chip Deselect to Output in High-Z(3)	—	6	—	7	—	8	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tPU	Chip Select to Power-Up Time(3)	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power-Down Time(3)	—	10	—	12	—	15	—	20/25	ns

2955 drw 11

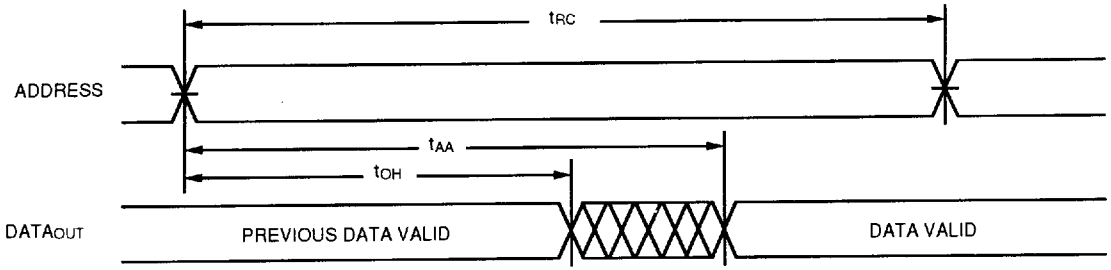
AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35 Min.	6168SA35 6168LA35 Max.	6168SA45(2) 6168LA45(2) Min.	6168SA45(2) 6168LA45(2) Max.	6168SA55(2) 6168LA55(2) Min.	6168SA55(2) 6168LA55(2) Max.	6168SA70(2) 6168LA70(2) Min.	6168SA70(2) 6168LA70(2) Max.	Unit
Read Cycle										
tRC	Read Cycle Time	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	55	—	70	ns
tACS	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
tCLZ	Chip Select to Output in Low-Z(3)	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Deselect to Output in High-Z(3)	—	15	—	25	—	25	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tPU	Chip Select to Power-Up Time(3)	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power-Down Time(3)	—	35	—	40	—	50	—	60	ns

2955 tbl 12

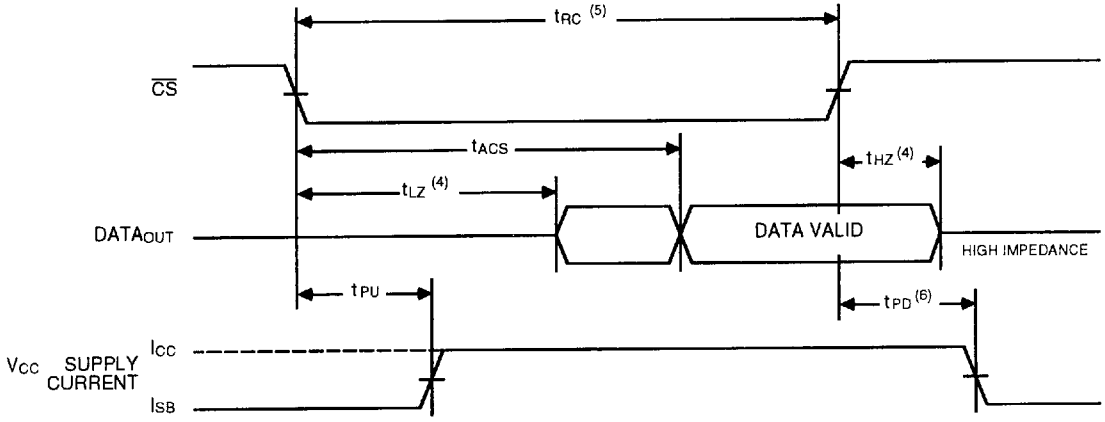
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
3. This parameter is guaranteed with AC Test load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2955 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2955 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. $\overline{CS}$ is LOW for read cycle.
3. Device is continuously selected, $\overline{CS} \leq V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10[1] Min.	6168SA10[1] Max.	6168SA12 Min.	6168SA12 Max.	6168SA15 Min.	6168SA15 Max.	6168SA20/25 6168LA20/25 Min.	6168SA20/25 6168LA20/25 Max.	Unit
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tCW	Chip Select to End-of-Write	10	—	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	10	—	12	—	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	7	—	8	—	9	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High-Z[3]	—	4	—	5	—	6	—	7	ns
tOW	Output Active from End-of-Write[3]	0	—	0	—	0	—	0	—	ns

2955 tbl 13

AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35 Min.	6168SA35 6168LA35 Max.	6168SA45[2] 6168LA45[2] Min.	6168SA45[2] 6168LA45[2] Max.	6168SA55[2] 6168LA55[2] Min.	6168SA55[2] 6168LA55[2] Max.	6168SA70[2] 6168LA70[2] Min.	6168SA70[2] 6168LA70[2] Max.	Unit
Write Cycle										
tWC	Write Cycle Time	30	—	40	—	50	—	60	—	ns
tCW	Chip Select to End-of-Write	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End-of-Write	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	30	—	40	—	50	—	60	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	DataValid to End-of-Write	15	—	20	—	20	—	25	—	ns
tDH	Data Hold Time	0	—	3	—	3	—	3	—	ns
tWHZ	Write Enable to Output in High-Z[3]	—	13	—	20	—	25	—	30	ns
tOW	Output Active from End-of-Write[3]	0	—	0	—	0	—	0	—	ns

2955 tbl 14

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
3. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

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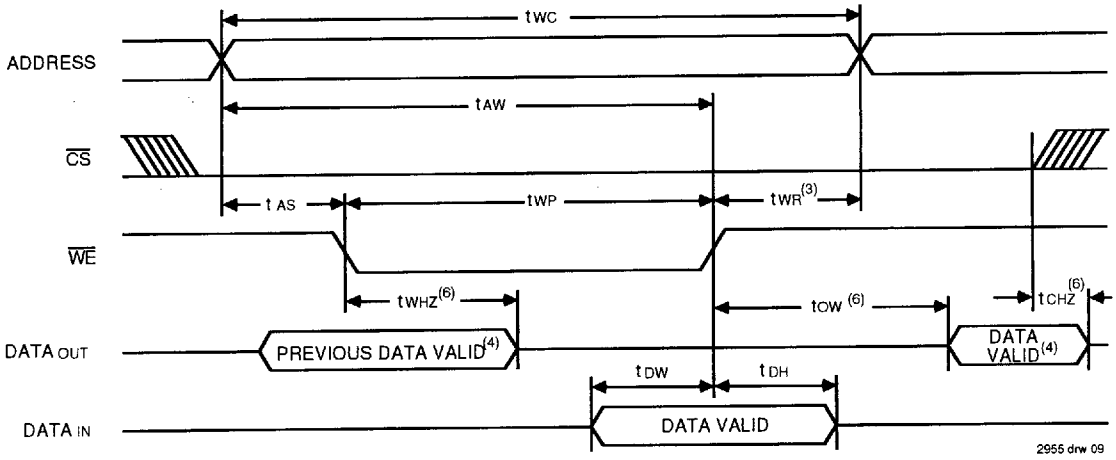
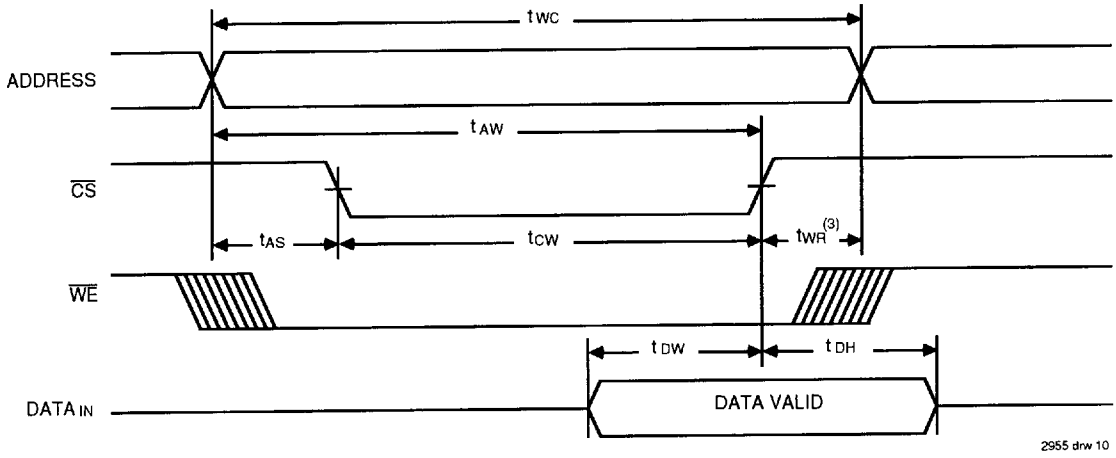
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5)

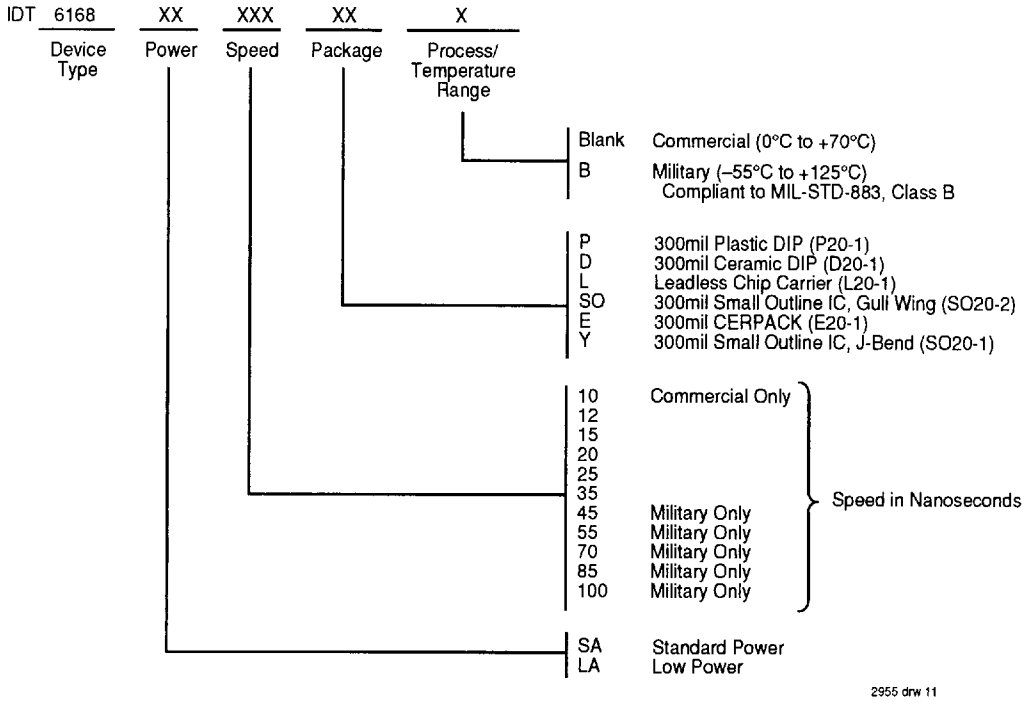


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



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