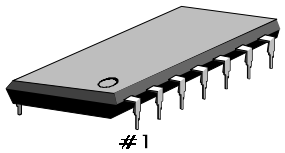
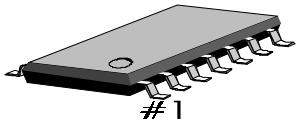
INTRODUCTION

The S5T0167 is a DTMF dialer for 4 bit binary data input from the microprocessor. When the tone enable input is low, the oscillator is inhibited and the device is in a low power consumption at standby mode.
On the low to high transition of tone enable, data is latched into the device and selected the standard DTMF signals.
The N-channel open drain output provides a MUTE output during tone generation.

14–DIP–300



14–SOP–225B



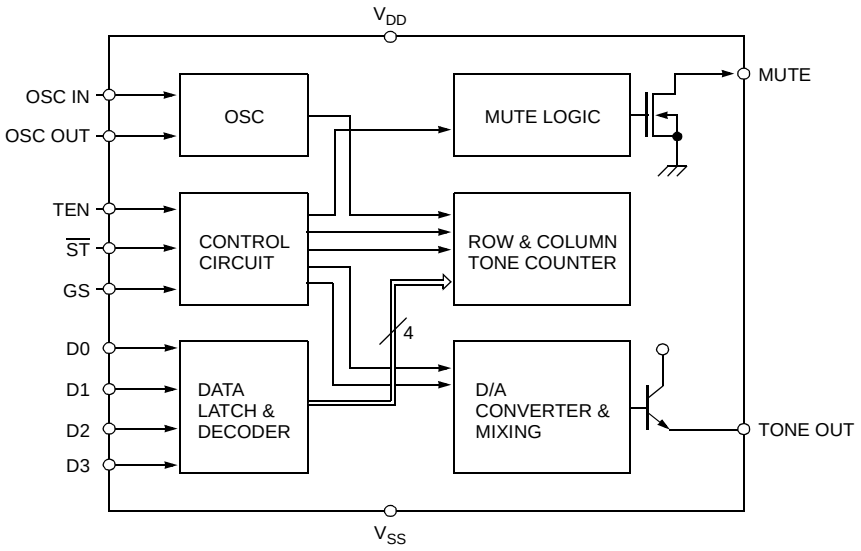
FEATURES

- Direct interface with microprocessor
- Generates 16 standard tones
- Uses inexpensive TV crystal or ceramic resonator (3.579545MHz)
- Very low total harmonic distortion
- Low power standby mode
- Binary data inputs with latches
- Wide Operating Voltage : 2.5 to 8.0V

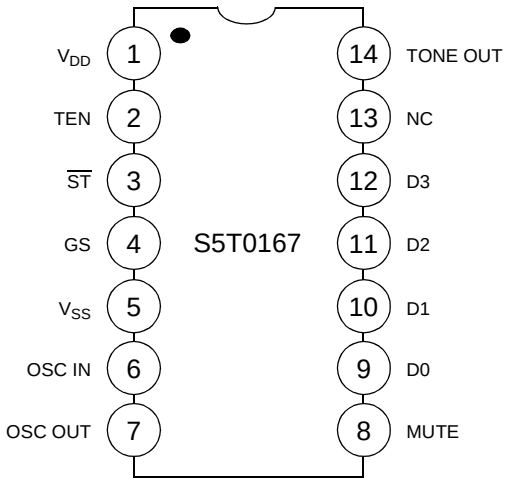
ORDERING INFORMATION

Device	Package	Operating Temperature
S5T0167X01-D0B0	14–DIP–300	– 30°C to +70°C
S5T0167X01-S0B0	14–SOP–225B	

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	Descriptions
1	V_{DD}	Positive supply input
2	TEN	Tone enable input. An internal pull-up resistor is in a chip. When this pin connects to logic low, the oscillator is inhibited and the tone generators and output transistor are turned off. A low to high transition on this pin latches in data from D0 to D3, and tone generation continues until this pin is connected low again.
3	ST	Single tone enable. An internal pull-up resistor is in a chip. When this pin connects to logic low, the device is in a single tone mode. For normal operation, connects this pin to V_{DD} or open-circuit.
4	GS	Group selection input. This pin is used to select the high group or low group frequency, when the device is in single tone mode. An internal pull-up resistor is in a chip. When this pin connects to V_{DD} or open, the high group will be generated, and when connects to V_{SS}, the low group will be generated.
5	V_{SS}	Negative supply input
6	OSC IN	Oscillator input
7	OSC OUT	Oscillator output
8	MUTE	N-channel open drain output. This pin is a logic high state, when the tone enable pin is a high state. This pin goes a logic low state, when the tone enable pin is a low state.
9, 10, 11, 12	D0, D1, D2, D3	DATA-INPUTS. These are the inputs for binary-coded data, which is latched in on the rising edge of the tone enable signal.
13	N.C	No connection.
14	Tone out	This output is the open emitter of a NPN transistor. When an external load resistor is connected from this pin to V_{SS}, the tone generates on the tone enable pin = High.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	9	V
MUTE Voltage	$V_{I\ (MUTE)}$	9	V
Input Voltage	V_I	V_{DD} + 0.3 to V_{SS} - 0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{OPR}	– 30 to + 70	°C
Storage Temperature	T_{STG}	– 55 to + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, 2V<V_{DD}<8V, f_{OSC} = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating voltage range	V_{DD}	–	2.0	–	8.0	V
Operating Current	I_{DD}	V_{DD} = 3.0V, MUTE Open	–	–	1.5	mA
Standby Current	I_{SB}	R_L = 10K, D0 to D3 open, V_{DD} = 3.0V	–	50	100	µA
Input Pull-up resistance	$R_{I\ (PULL)}$	DI0 to DI3, TEN	–	100	–	KΩ
Input Voltage	V_{IL}	DI0 to DI3, TEN	V_{SS}	–	$0.2V_{DD}$	V
	V_{IH}		$0.8V_{DD}$	–	V_{DD}	V
Output Current (MUTE)	$I_{OL\ (MUTE)}$	V_{DD} = 3V, V_O = 0.5, TEN = LOW	0.5	1.5	–	mA
	$I_{OH\ (MUTE)}$	V_{DD} = 3V, V_O = V_{DD}, TEN = HIGH	–	1	2	µA
Tone Output Level	$V_{O\ (TONE)}$	V_{DD} = 3V, R_L = 5kΩ, Row Tone	–14	–	–11	dBV
Ratio of Column to Row	dB_{CR}	V_{DD} = 3V, R_L = 5kΩ	1	2	3	dB
THD (Dual Tone)	THD	1MHz Bandwidth, V_{DD} = 5V, R_L = 5kΩ	–20	–	–	dB
Oscillator Start-up Time	$t_{ST\ (OSC)}$	90% Amplitudes, V_{DD} = 3.0V	–	4	–	mS
Data Set-up Time	$t_{SU\ (DATA)}$	V_{DD} = 3.0V	200	–	–	nS
Data Hold Time	$t_{H\ (DATA)}$	V_{DD} = 3.0V	200	–	–	nS
Data Duration	$t_{W\ (DATA)}$	V_{DD} = 3.0V	600	–	–	nS

APPLICATION INFORMATION

FUNCTION DESCRIPTION

When tone enable input is low, oscillator is inhibited, being allowed to low power standby mode since transistor goes to turn off state, so D0 to D3 input data is ignored.
However if tone enable input goes from low to high, input data is latched and tone output is enabled, and it is correspond to data input. This device is designed with 14 levels, 28 segments in each single-tone. The column tone is pre-emphasized 2dB than the row tone.

Table 1. Single Tone Frequency

Tone Group	Standard DTMF (Hz)	Tone Output Actual Frequency	% Deviation from Standard
ROW 1	697	699.13	+ 0.31
ROW 2	770	766.17	– 0.50
ROW 3	852	845.43	– 0.54
ROW 4	941	947.97	+ 0.74
COLUMN 1	1209	1215.89	+ 0.57
COLUMN 2	1336	1331.67	– 0.33
COLUMN 3	1477	1471.85	– 0.35
COLUMN 4	1633	1645.01	+ 0.75

Table 2. Function Table

Key Board Equivalent	Data Input				Tone Output	
	D3	D2	D1	D0	f_L (Hz)	f_H (Hz)
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

NOTES