U 6024 BS-FP
U 6028 BS-FP

6-GHz Frequency Divider

Description

U 6024/28 BS are high speed frequency dividers using TELEFUNKEN's advanced bipolar technology. The input frequency ranges from 3 to 6 GHz. Output buffer and voltage regulator are integrated. The devices are suitable for satellite communications, instrumentation and telecomunications.

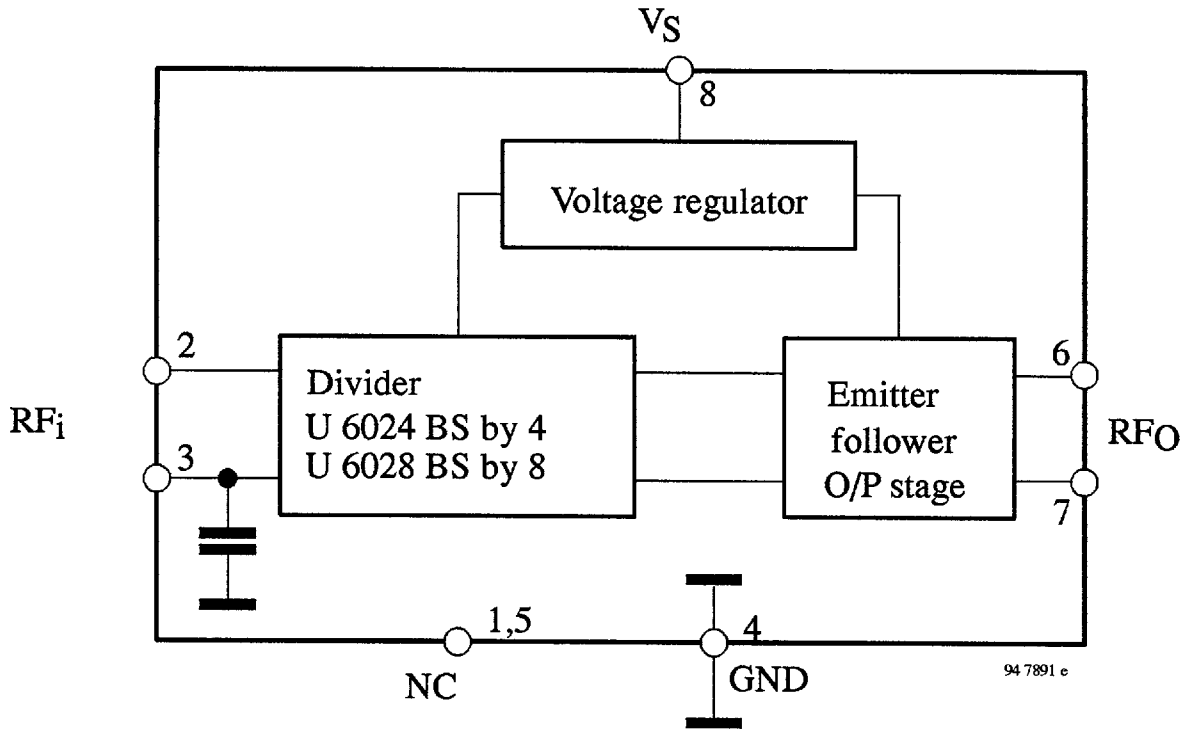
Features

- U 6024 BS divides by 4
- U 6028 BS divides by 8
- Very low current consumption (45 mA typical)
- 6-GHz maximum operating frequency
- 5-V (typical) supply voltage
- ESD protected according to MIL-STD.883 method 3015 class 2
- SO-8 package

Benefits

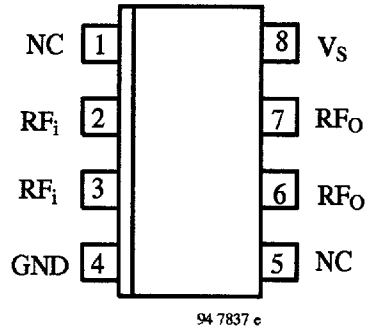
- Extended operation time due to low current consumption
- Only three external components
- Low RF input level reduces radiation problems

Block Diagram



Pin Description

Pin	Symbol	Function
1	NC	Not connected
2	RF_i	RF input
3	RF_i	RF input with internal decoupling capacitor
4	GND	Ground
5	NC	Not connected
6	RF_o	RF Output
7	RF_o	RF Output
8	V_S	Supply voltage



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Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pin 8	V_S	6	V
Input voltage range	Pins 2 and 3	V_i	0 to Vs	V
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	-40 to +125	°C

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage range	V_S	4.5 to 5.5	V
Ambient temperature range	T_{amb}	-25 to +80	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient, SO-8	R_{thja}	175	K/W

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 4.5 to 5.5 V, T_{amb} = 0 to 70°C., referred to test circuit

Parameters	Test Conditions / Pin	Symbol	Min	Typ	Max	Unit
Supply current	V_S = 5 V Pin 8	I_S		45		mA
RF input	Pin 2	RF_i				
Input sensitivity	R_S = 50 Ω	V_{RFi}		Figure 2		
Large signal compatibility	R_S = 50 Ω	V_{maxRFi}		Figure 2		
Input frequency range		fi_{min} fi_{max}	6000		3000	MHz
RF output	Pins 6 and 7	RF_O				
Output level		V_{RFo}		200		mV_{PP}
DC output level High Low	V_S = 5 V $R_L \geq 10$ kΩ	 RF_{DCH} RF_{DCL}		 3.6 3.1		 V V

Note: 1 RMS-voltage calculated from the measured available power
R_S = system resistance, R_L = load resistance

Output stage

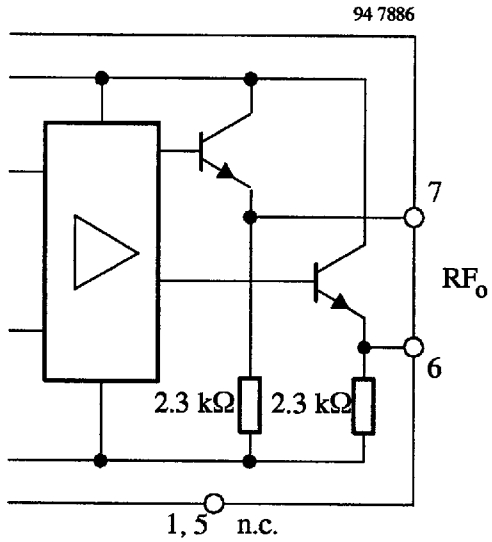

Figure 1

Input sensitivity vs. frequency

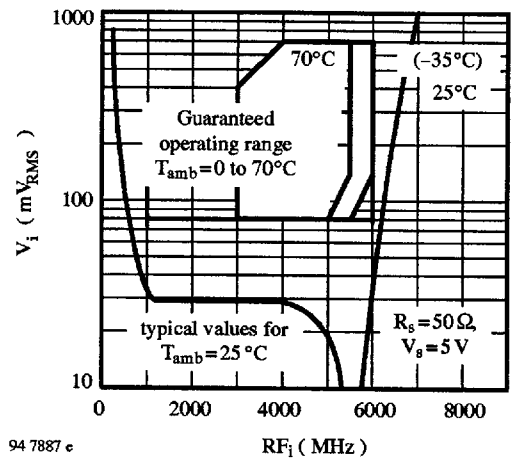

Figure 2

Input impedance S11

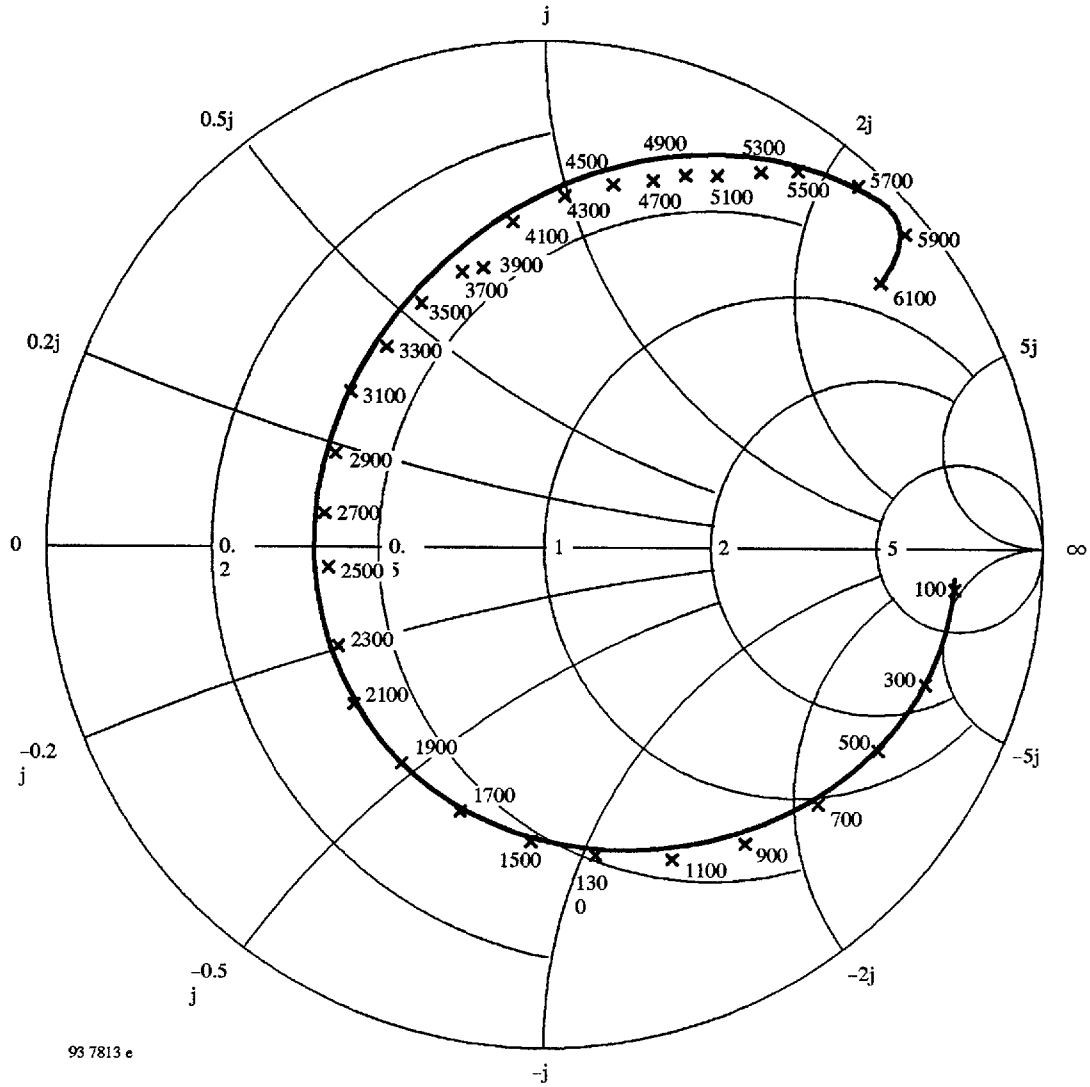

Figure 3

Application

Master-Slave-D-Flip-Flops (MS-D-FF's) can be used for frequency division by feeding back the inverted output to the data input. Typical for this kind of dividers is a free running oscillation of the first divider stage. Here the input sensitivity of the circuit has a minimum (see input sensitivity vs. frequency). An oscillation frequency of e.g. 5.6 GHz (related to the input) will result in an output frequency of 5.6 GHz: 8 = 700 MHz. TEMIC's self oscillating frequency dividers are indicated with suffix "S" (U 6028 BS-AFP). This oscillation often is used for quality control of IC's: the higher the frequency, the better the performance.

On the other hand, if this oscillation causes problems e.g. in frequency counters an external offset can be added. This can simply be done by connecting an ohmic resistor from pin 3 (RF INPUT) to ground. A value of R_3 = 47 kΩ will stop self oscillation without degrading the input sensitivity markly. Smaller values will decrease the sensitivity especially at higher frequencies.

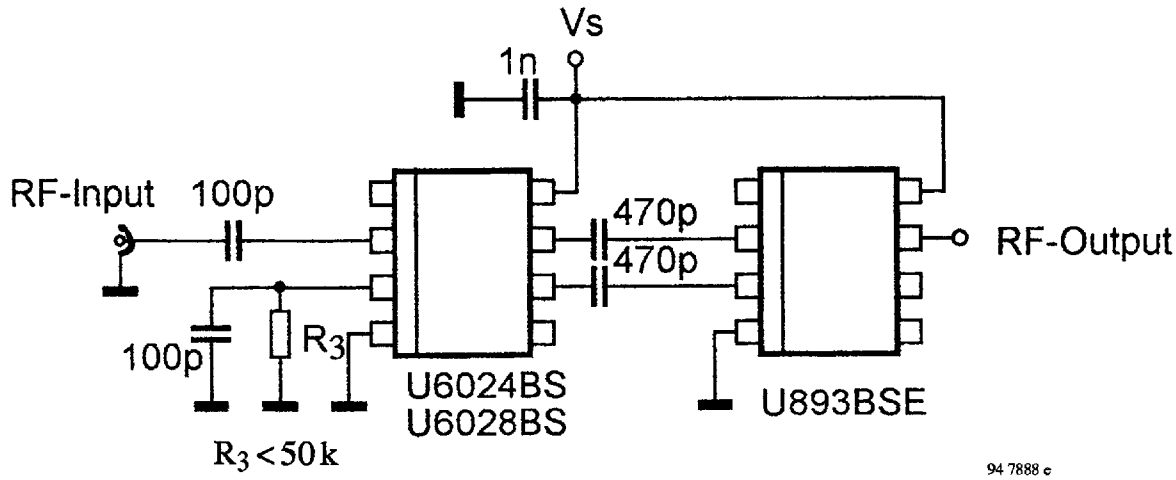

Figure 4 Application Circuitry

Dimensions in mm

Package: SO 8