

1/16, 1/32 DUTY LCD CONTROLLER/DRIVER
DESCRIPTION

μPD16676 is a controller/driver containing RAMs capable of full-dot LCD displays. One of these IC chips can drive the full-dot LCD up to 61-by-16 dots.

These ICs are the most suitable for Kanji character or Chinese character pagers, as well as graphic pagers, displaying 16-by-16 dots per character.

FEATURES

- LCD driver with built-in display RAM
- Dot display RAM: 2560 bits
- Output: 61 segments & 16 commons
- 8-bit parallel interface
- Oscillation circuit incorporated

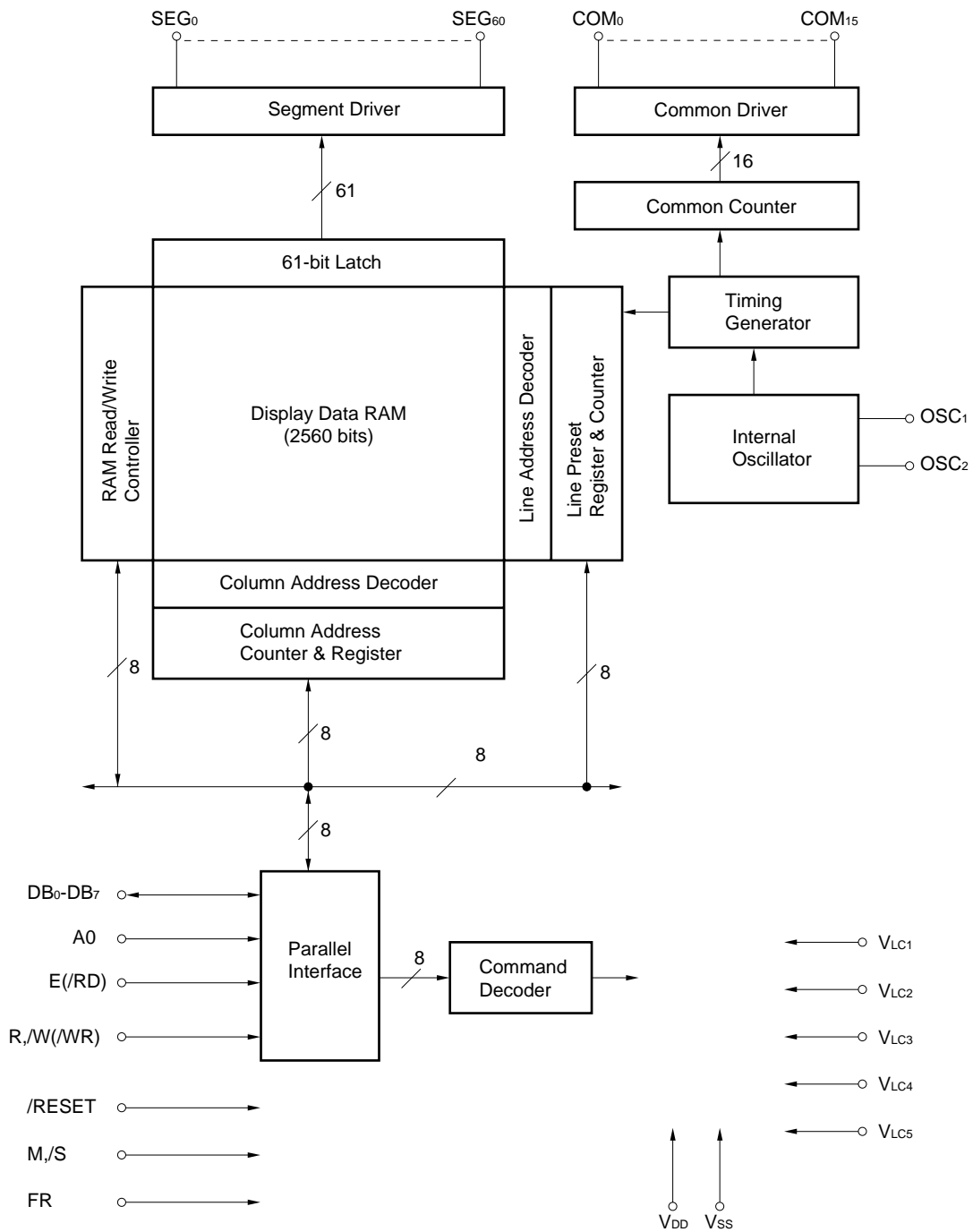
★ ORDERING INFORMATION

Part Number	Package
μPD16676P	Chips
μPD16676W	Wafer
μPD16676GF-3BA	100-PIN PLASTIC QFP (14 x 20 mm)

Remark Purchasing the above products in terms of chips per wafer requires an exchange of other documents as well, including a memorandum of the product quality. Therefore, those who are interested in this regard are advised to contact an NEC salesperson for further details.

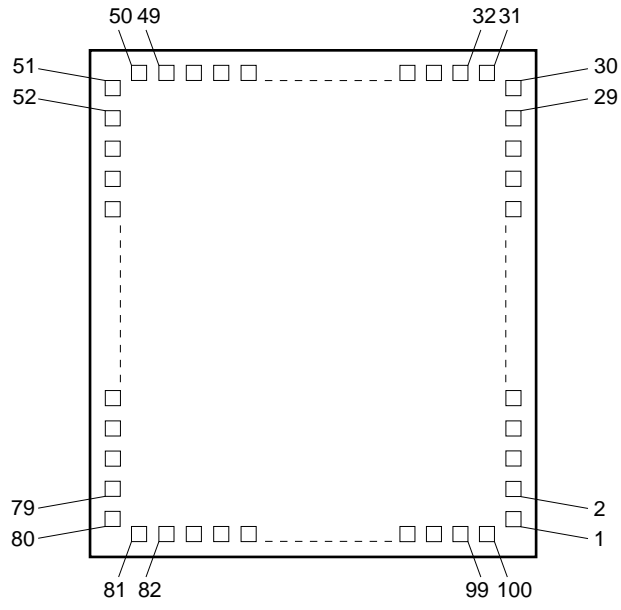
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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signals.

2. PIN CONFIGURATION (Pad Layout)



3. PIN CONNECTION

Pin No.	Pin Symbol	I/O	Pin No.	Pin Symbol	I/O
1	COM ₅	Output	51	SEG ₂₁	Output
2	COM ₆	Output	52	SEG ₂₀	Output
3	COM ₇	Output	53	SEG ₁₉	Output
4	COM ₈	Output	54	SEG ₁₈	Output
5	COM ₉	Output	55	SEG ₁₇	Output
6	COM ₁₀	Output	56	SEG ₁₆	Output
7	COM ₁₁	Output	57	SEG ₁₅	Output
8	COM ₁₂	Output	58	SEG ₁₄	Output
9	COM ₁₃	Output	59	SEG ₁₃	Output
10	COM ₁₄	Output	60	SEG ₁₂	Output
11	COM ₁₅	Output	61	SEG ₁₁	Output
12	SEG ₆₀	Output	62	SEG ₁₀	Output
13	SEG ₅₉	Output	63	SEG ₉	Output
14	SEG ₅₈	Output	64	SEG ₈	Output
15	SEG ₅₇	Output	65	SEG ₇	Output
16	SEG ₅₆	Output	66	SEG ₆	Output
17	SEG ₅₅	Output	67	SEG ₅	Output
18	SEG ₅₄	Output	68	SEG ₄	Output
19	SEG ₅₃	Output	69	SEG ₃	Output
20	SEG ₅₂	Output	70	SEG ₂	Output
21	SEG ₅₁	Output	71	SEG ₁	Output
22	SEG ₅₀	Output	72	SEG ₀	Output
23	SEG ₄₉	Output	73	A0	Input
24	SEG ₄₈	Output	74	OSC ₁	Input
25	SEG ₄₇	Output	75	OSC ₂	Output
26	SEG ₄₆	Output	76	E(/RD)	Input
27	SEG ₄₅	Output	77	R _i /M(/WR)	Input
28	SEG ₄₄	Output	78	V _{SS}	—
29	SEG ₄₃	Output	79	DB ₀	Input/Output
30	SEG ₄₂	Output	80	DB ₁	Input/Output
31	SEG ₄₁	Output	81	DB ₂	Input/Output
32	SEG ₄₀	Output	82	DB ₃	Input/Output
33	SEG ₃₉	Output	83	DB ₄	Input/Output
34	SEG ₃₈	Output	84	DB ₅	Input/Output
35	SEG ₃₇	Output	85	DB ₆	Input/Output
36	SEG ₃₆	Output	86	DB ₇	Input/Output
37	SEG ₃₅	Output	87	V _{DD}	—
38	SEG ₃₄	Output	88	/RESET	Input
39	SEG ₃₃	Output	89	FR	Input/Output
40	SEG ₃₂	Output	90	V _{LC5}	—
41	SEG ₃₁	Output	91	V _{LC3}	—
42	SEG ₃₀	Output	92	V _{LC2}	—
43	SEG ₂₉	Output	93	M _i /S	Input
44	SEG ₂₈	Output	94	V _{LC4}	—
45	SEG ₂₇	Output	95	V _{LC1}	—
46	SEG ₂₆	Output	96	COM ₀	Output
47	SEG ₂₅	Output	97	COM ₁	Output
48	SEG ₂₄	Output	98	COM ₂	Output
49	SEG ₂₃	Output	99	COM ₃	Output
50	SEG ₂₂	Output	100	COM ₄	Output

4. PIN COORDINATES

Chip Size : 4.04 x 5.53 mm²
 Pad Size Al Area : 120 x 120 μm²
 Pad Size Open Area : 108 x 108 μm²

Pin No.	X (μm)	Y (μm)	Pin No.	X (μm)	Y (μm)	Pin No.	X (μm)	Y (μm)
1	1771	-2230	36	668.8	2517.2	71	-1771	-757.2
2	1771	-2076	37	518.8	2517.2	72	-1771	-907.2
3	1771	-1922	38	368.8	2517.2	73	-1767.8	-1149.4
4	1771	-1768	39	218.8	2517.2	74	-1767.8	-1299.4
5	1771	-1614	40	68.8	2517.2	75	-1767.8	-1489.4
6	1771	-1460	41	-81.2	2517.2	76	-1767.8	-1639.4
7	1771	-1306	42	-231.2	2517.2	77	-1767.8	-1839.4
8	1771	-1152	43	-381.2	2517.2	78	-1767.8	-1989.4
9	1771	-998	44	-531.2	2517.2	79	-1767.8	-2139.4
10	1771	-844	45	-681.2	2517.2	80	-1767.8	-2289.4
11	1771	-690	46	-831.2	2517.2	81	-1745	-2513.4
12	1771	-536	47	-981.2	2517.2	82	-1595	-2513.4
13	1771	-382	48	-1131.2	2517.2	83	-1395	-2513.4
14	1771	-228	49	-1281.2	2517.2	84	-1245	-2513.4
15	1771	-74	50	-1431.2	2517.2	85	-1045	-2513.4
16	1771	80	51	-1771	2242.8	86	-895	-2513.4
17	1771	234	52	-1771	2092.8	87	-682.6	-2513.4
18	1771	388	53	-1771	1942.8	88	-532.2	-2513.4
19	1771	542	54	-1771	1792.8	89	-382.2	-2513.4
20	1771	696	55	-1771	1642.8	90	-106.6	-2513.4
21	1771	850	56	-1771	1492.8	91	69.8	-2513.4
22	1771	1004	57	-1771	1342.8	92	219.8	-2513.4
23	1771	1158	58	-1771	1192.8	93	369.8	-2513.4
24	1771	1312	59	-1771	1042.8	94	569.8	-2513.4
25	1771	1466	60	-1771	892.8	95	719.8	-2513.4
26	1771	1620	61	-1771	742.8	96	952.4	-2513.4
27	1771	1774	62	-1771	592.8	97	1102.4	-2513.4
28	1771	1928	63	-1771	442.8	98	1252.4	-2513.4
29	1771	2082	64	-1771	292.8	99	1402.4	-2513.4
30	1771	2236	65	-1771	142.8	100	1552.4	-2513.4
31	1418.8	2517.2	66	-1771	-7.2			
32	1268.8	2517.2	67	-1771	-157.2			
33	1118.8	2517.2	68	-1771	-307.2			
34	968.8	2517.2	69	-1771	-457.2			
35	818.8	2517.2	70	-1771	-607.2			

5. PIN DESCRIPTIONS

5.1 Power System

Pin Symbol	Pin Name	Pin No.	I/O	Function Description
V _{DD}	Power supply pin	87	—	Power supply
V _{SS}	Ground	78	—	Ground
V _{LC1} to V _{LC5}	Reference power supply for drivers	90,91,92, 94,95	—	Reference power supply for LCD driving

5.2 Logic system

Pin Symbol	Pin Name	Pin No.	I/O	Function Description
M,/S	Master/Slave selection	93	Input	Switches between the master chip and the slave chip.
FR	LCD to AC signal	89	Input/ Output	Exchanges synchronizing signals (LCD-to-AC signals) in connecting cascades. This pin is for output if the chip is the master, and for input if the chip is the slave.
DB ₀ to DB ₇	Data Bus	79 to 86	Input/ Output	Data inputs/outputs
A0	Data/Instruction Switching	73	Input	This pin is used for switching between the display data and the instruction. High level : Display data Low level : Instruction
/RESET	Reset and 68/80-series switching	88	Input	This pin performs reset at the edge of the low-level pulse. At that level, it performs switching 68/80 series modes. High level : 68 series MPU interface Low level : 80 series MPU interface
E(/RD)	Enable and read enable	76	Input	68 series mode : Enable signal 80 series mode : Read enable signal
R,/W(/WR)	Read/Write and Write enable	77	Input	68 series mode : Read/Write signal 80 series mode : Write enable signal
OSC ₁	Oscillation pin	74	Input	Oscillation (connected with a register between OSC ₂)
OSC ₂	Oscillation pin	75	Output	Oscillation (connected with a register between OSC ₁)

5.3 Driver System

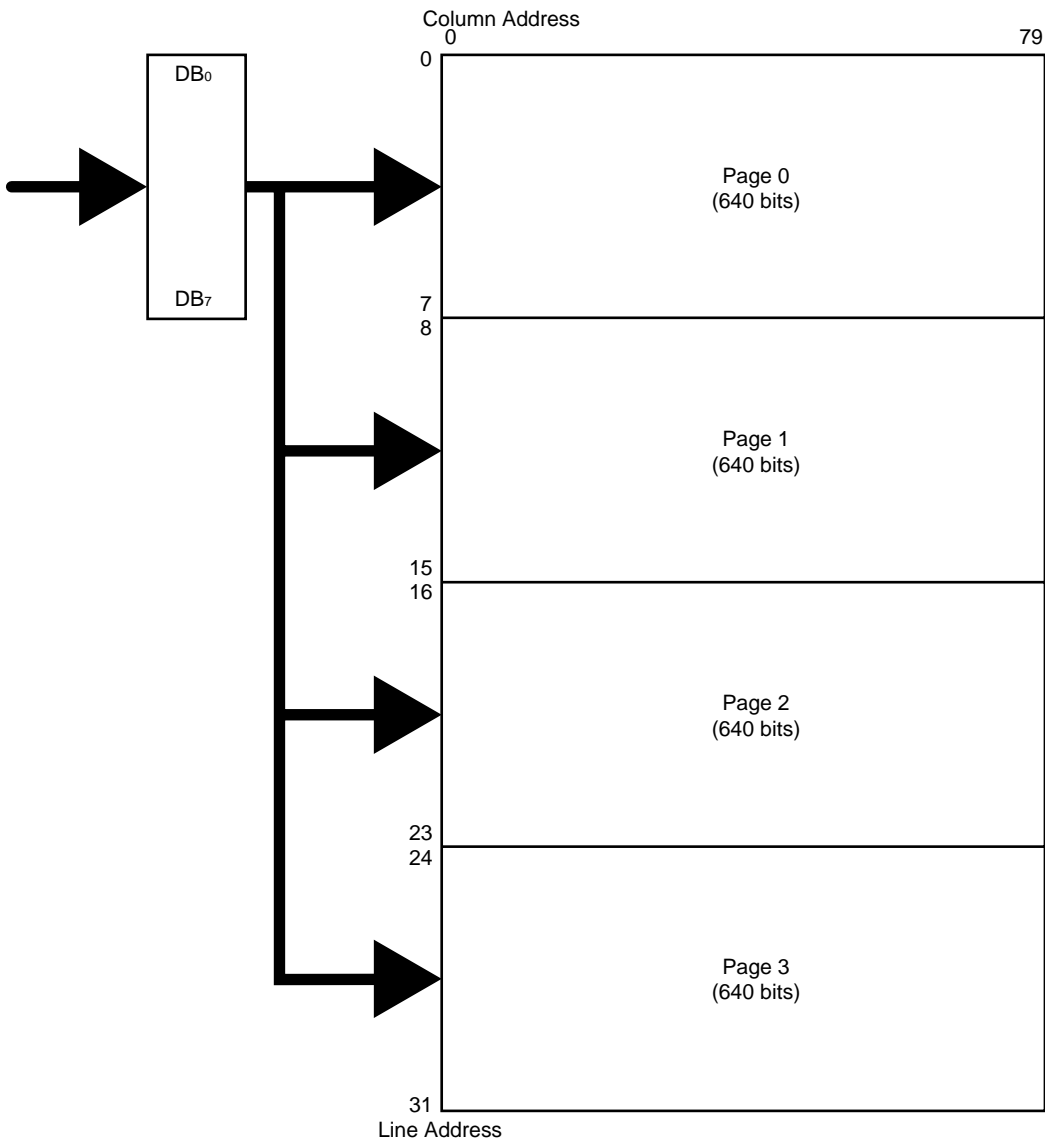
Pin Symbol	Pin Name	Pin No.	I/O	Description
SEG ₀ to SEG ₆₀	Segment	72 to 12	Output	Segment output pins
COM ₀ to COM ₁₅	Common	96 to 100, 1 to 11	Output	Common output pins If the chip is a slave, these pins correspond to COM ₁₆ to COM ₃₁ .

6. COMMANDS

Command	/RD	/WR	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
1 Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	ON/OFF of the whole display is performed independent of the display RAM's data or internal state. 1: ON, 0: OFF (Power save at static drive ON) ^{Note}
2 Display start line	1	0	0	1	1	0	Display start address (0 to 31)					Determines the RAM line displayed on the uppermost line (COM ₀) of the display.
3 Page address set	1	0	0	1	0	1	1	1	0	Pages (0 to 3)		Sets display RAM pages in the page address register.
4 Column(segment) address set	1	0	0	0			Column addresses (0 to 79)					Sets display RAM's column address in the column address register.
5 Status read	0	1	0	B U S Y	A D C	O N / O F	R E S E T	0	0	0	0	Reads status BUSY 1: During internal operation 0: READY status ADC 1: Clockwise output(Normal rotation) 0: Counterclockwise output (Reverse) ON/OFF 1: Display OFF, 0: Display ON RESET 1: Being reset, 0: Normal
6 Display data write	1	0	1	Write Data							Displays the data bus data and writes it onto the display RAM.	Accesses the display RAM of a pre-specified address. After access, the column address is incremented.
7 Display data read	0	1	1	Read data							Reads the data in the display RAM onto the data bus.	
8 ADC select	1	0	0	1	0	1	0	0	0	0	0/1	This command is used to reverse the correspondence relationship between display RAM's column addresses and segment driver outputs. 0: Clockwise output (Normal rotation) 1: Counterclockwise output (Reverse)
9 Static drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects between the normal display operation and the static all-lamp-driven display. 1: Static drive (Power save) ^{Note} 0: Normal display operation
10 Duty select	1	0	0	1	0	1	0	1	0	0	0/1	Selects between two different liquid-crystal cell driving duties. 1: 1/32 duty 0: 1/16 duty
11 Read modify write	1	0	0	1	1	1	0	0	0	0	0	Increments the column address counter only when writing the display data; but not when reading it.
12 END	1	0	0	1	1	1	0	1	1	1	0	Cancels read modify write mode
13 Reset	1	0	0	1	1	1	0	0	0	1	0	Sets the display start line register to the first line. Sets the column address counter and the page address register to 0.

Note If the static drive is turned ON in the display OFF state, the machine is placed in the power save state.

7. DISPLAY RAM MAP

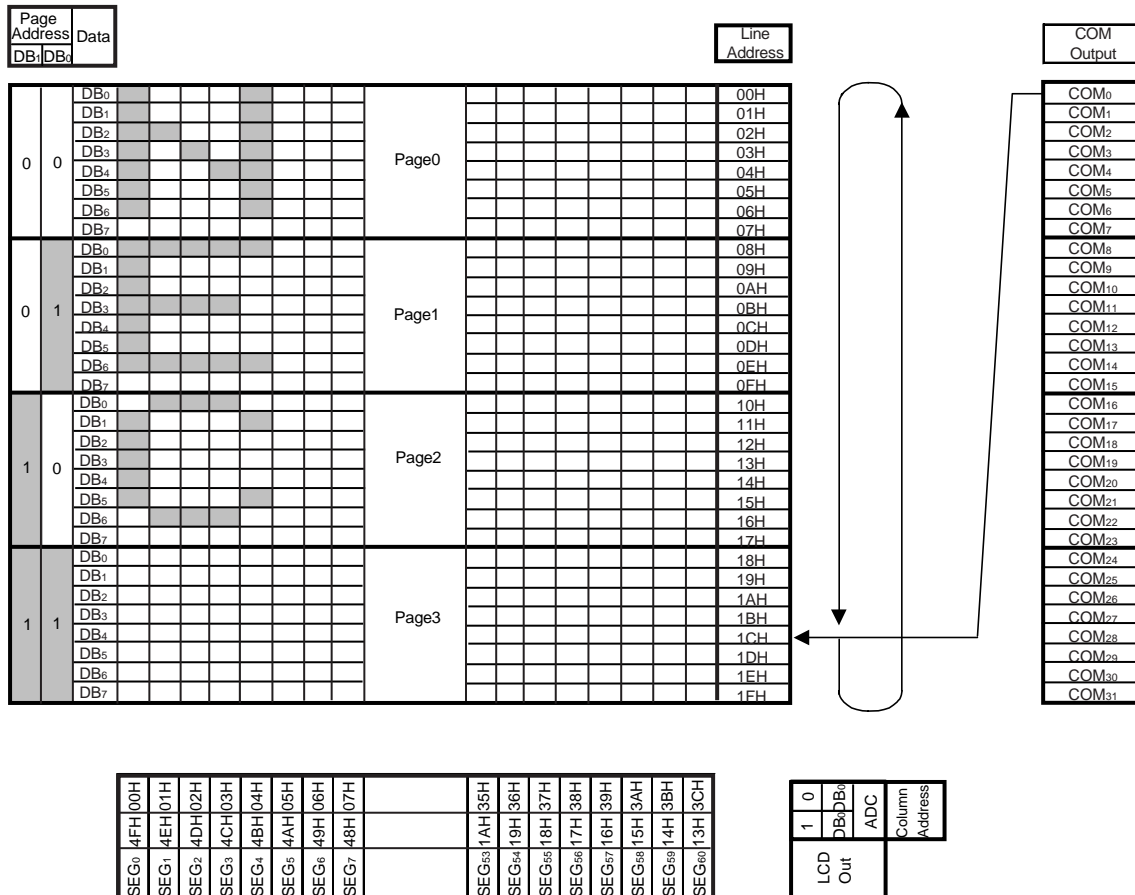


★ 8. Line Address Circuit

As is shown in Figure 8-1, the line address circuit specifies the line address that corresponds to a COM output for displaying the contents of display data RAM. The display start line address set command specifies line address of to the COM₀ output.

The screen can be scrolled by dynamically changing the line address via the display start line address set command.

Figure 8-1. Specification of Display Start Line Address in Display Data RAM



Remark COM₁₆ to COM₃₁ are valid in only 1/32 duty.

★ 9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{DD}	-0.3 to +6.5	V
Driver reference supply input voltage	V _{LC1} to V _{LC4}	V _{DD} -13 to V _{DD} +0.3	V
Driver reference supply input voltage	V _{LC5}	V _{DD} -13 to +0.3	V
Logic system input voltage	V _{IN1}	-0.3 to V _{DD} + 0.3	V
Logic system output voltage	V _{OUT1}	-0.3 to V _{DD} + 0.3	V
Logic system input/output voltage	V _{I/O1}	-0.3 to V _{DD} + 0.3	V
Driver system output voltage	V _{OUT2}	V _{LC5} -0.3 to V _{DD} + 0.3	V
Operating ambient temperature	T _A	-40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C

Cautions 1. If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

2. Ensure that the phase relationship is V_{DD} ≥ V_{LC1} ≥ V_{LC2} ≥ V_{LC3} ≥ V_{LC4} ≥ V_{LC5}.

Recommended Operating Range (V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{DD}	2.7		5.5	V
Reference supply voltage	V _{LC1} to V _{LC4}	V _{DD} -12		V _{DD}	V
Reference supply voltage	V _{LC5}	V _{DD} -12		0	V
Logic system input voltage	V _{IN1}	0		V _{DD}	V

Electrical Characteristics (Unless otherwise specified, T_A = -40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP. ^{Note}	MAX.	Unit
High-level input voltage	V _{IH1}	A0, DB ₀ to DB ₇ , E, R, _/ W	0.8 V _{DD}			V
High-level input voltage	V _{IH2}	FR, M, _/ S, _/ RESET	0.8 V _{DD}			V
Low-level input voltage	V _{IL1}	A0, DB ₀ to DB ₇ , E, R, _/ W			0.2 V _{DD}	V
Low-level input voltage	V _{IL2}	FR, M, _/ S, _/ RESET			0.2 V _{DD}	V
High-level input current	I _{IH}	A0, E, R, _/ W, _/ RESET			1	μA
Low-level input current	I _{IL}	A0, E, R, _/ W, _/ RESET			-1	μA
High-level output voltage	V _{OH1}	I _{OUT} = -3 mA, DB ₀ to DB ₇ , V _{DD} = 4.5 to 5.5 V	0.8 V _{DD}			V
High-level output voltage	V _{OH2}	I _{OUT} = -2 mA, FR, V _{DD} = 4.5 to 5.5 V	0.8 V _{DD}			V
High-level output voltage	V _{OH3}	I _{OUT} = -120 μA, OSC ₂ , V _{DD} = 4.5 to 5.5 V	0.8 V _{DD}			V
Low-level output voltage	V _{OL1}	I _{OUT} = 3 mA, DB ₀ to DB ₇ , V _{DD} = 4.5 to 5.5 V			0.2 V _{DD}	V
Low-level output voltage	V _{OL2}	I _{OUT} = 2 mA, FR, V _{DD} = 4.5 to 5.5 V			0.2 V _{DD}	V
Low-level output voltage	V _{OL3}	I _{OUT} = 120 μA, OSC ₂ , V _{DD} = 4.5 to 5.5 V			0.2 V _{DD}	V
High-level output voltage	V _{OH1}	I _{OUT} = -1.5 mA, DB ₀ to DB ₇ , V _{DD} = 2.7 to 4.5 V	0.8 V _{DD}			V
High-level output voltage	V _{OH2}	I _{OUT} = -1 mA, FR, V _{DD} = 2.7 to 4.5 V	0.8 V _{DD}			V
High-level output voltage	V _{OH3}	I _{OUT} = -80 μA, OSC ₂ , V _{DD} = 2.7 to 4.5 V	0.8 V _{DD}			V
Low-level output voltage	V _{OL1}	I _{OUT} = 1.5 mA, DB ₀ to DB ₇ , V _{DD} = 2.7 to 4.5 V			0.2 V _{DD}	V
Low-level output voltage	V _{OL2}	I _{OUT} = 1 mA, FR, V _{DD} = 2.7 to 4.5 V			0.2 V _{DD}	V
Low-level output voltage	V _{OL3}	I _{OUT} = 80 μA, OSC ₂ , V _{DD} = 2.7 to 4.5 V			0.2 V _{DD}	V
High-level leak current	I _{LOH}	DB ₀ to DB ₇ , V _{IN/OUT} = V _{DD}			3	μA
Low-level leak current	I _{LOL}	DB ₀ to DB ₇ , V _{IN/OUT} = V _{SS}			-3	μA
Driver output ON resistor	R _{ON}	T _A = 25 °C, V _{DD} = 5 V, V _{LCS} = V _{SS}			7.5	kΩ
Driver output ON resistor	R _{ON}	T _A = 25 °C, V _{DD} = 3.5 V, V _{LCS} = V _{SS}			50	kΩ
Static current consumption	I _{DD0}				1.0	μA
Dynamic current consumption	I _{DD1}	External clock: 18 kHz			15.0	μA
		Self-oscillation: R = 1.3 MΩ			30.0	μA
Dynamic current consumption	I _{DD3}	During access: t _{CYC} = 200 kHz			500	μA
Input capacitance	C _{IN}	T _A = 25 °C, f = 1 MHz			8.0	pF
Oscillator frequency	f _{OSC}	In self-oscillation, V _{DD} = 5.0 V, R = 1.3 MΩ ± 2%	15	18	21	kHz
Oscillator frequency	f _{OSC}	In self-oscillation, V _{DD} = 3.0 V, R = 1.3 MΩ ± 2%	11	16	21	kHz
Reset time	t _R	_/ RESET↓→Internal reset release	1.0		1000	μs

Remark The TYP. value is a reference value when T_A = 25 °C.

AC Characteristics 1 (Unless otherwise specified, T_A = -40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

80 Series MPU Read/Write Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address hold time	t _{AH8}	A0	10			ns
Address setup time	t _{AW8}		20			ns
System cycle time	t _{CYC8}	/WR, /RD	1000			ns
Control pulse width	t _{CC}		200			ns
Data setup time	t _{DS8}	DB ₀ to DB ₇	80			ns
Data hold time	t _{DH8}		10			ns
/RD access time	t _{ACC8}	DB ₀ to DB ₇ , C _L = 100 pF			90	ns
Output disable time	t _{OH8}		10		60	ns

68 Series MPU Read/Write Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System cycle time	t _{CYC6}	A0, R,/W	1000			ns
Address setup time	t _{AW6}		20			ns
Address hold time	t _{AH6}		10			ns
Data setup time	t _{DS6}	DB ₀ to DB ₇	80			ns
Data hold time	t _{DH6}		10			ns
Output disable time	t _{OH6}	DB ₀ to DB ₇ , C _L = 100 pF	10		60	ns
Access time	t _{ACC6}				90	ns
Enable pulse width	READ	E	t _{EW}	100		ns
	WRITE			80		ns

AC Characteristics 2 (Unless otherwise specified, T_A = -40 to +85 °C, V_{DD} = 2.7 to 4.5 V)

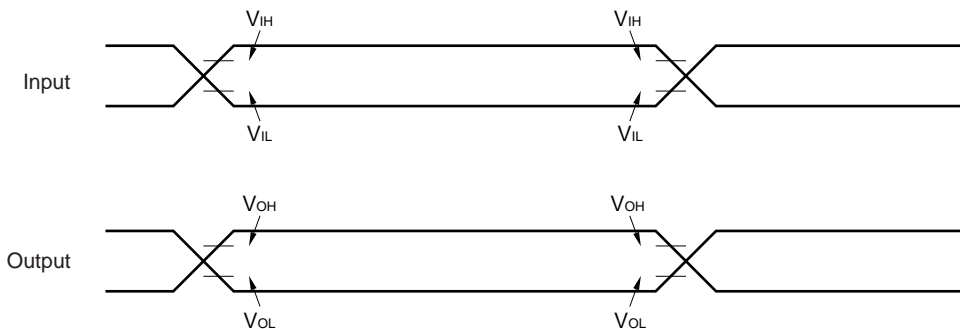
80 Series MPU Read/Write Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address hold time	t _{AH8}	A0	20			ns
Address setup time	t _{AW8}		40			ns
System cycle time	t _{CYC8}	/WR, /RD	2000			ns
Control pulse width	t _{CC}		400			ns
Data setup time	t _{DS8}	DB ₀ to DB ₇	160			ns
Data hold time	t _{DH8}		20			ns
/RD access time	t _{ACC8}	DB ₀ to DB ₇ , C _L = 100 pF			180	ns
Output disable time	t _{OH8}		20		120	ns

68 Series MPU Read/Write Timing

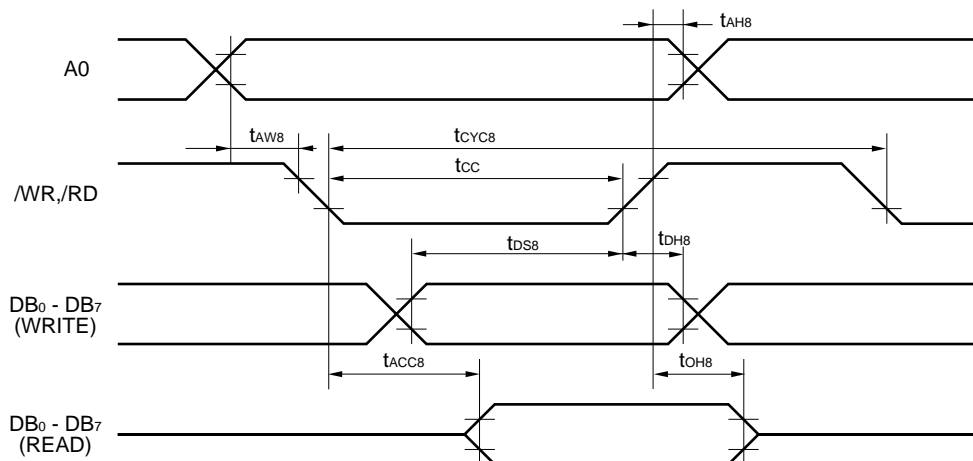
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System cycle time	t _{CYC6}	A0, R,/W	2000			ns
Address setup time	t _{AW6}		40			ns
Address hold time	t _{AH6}		20			ns
Data setup time	t _{DS6}	DB ₀ to DB ₇	160			ns
Data hold time	t _{DH6}		20			ns
Output disable time	t _{OH6}	DB ₀ to DB ₇ , C _L = 100 pF	20		120	ns
Access time	t _{ACC6}				180	ns
Enable pulse width	READ	t _{EW}	E	200		ns
	WRITE			160		ns

Test Point of Switching Characteristics

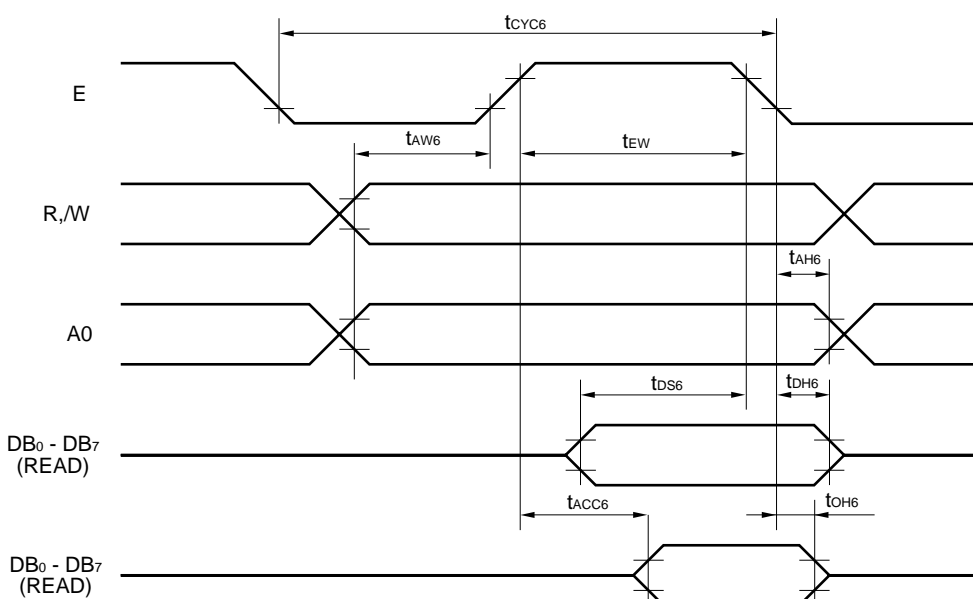


Waveforms of Switching Characteristics

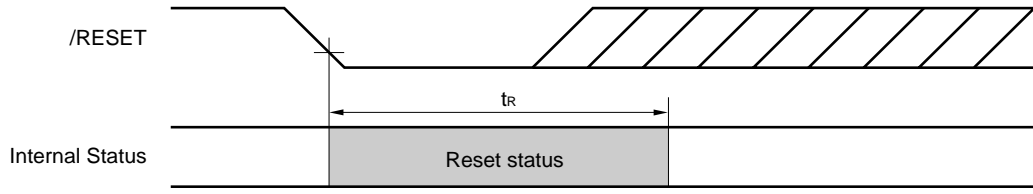
80 Series MPU Read/Write Timing



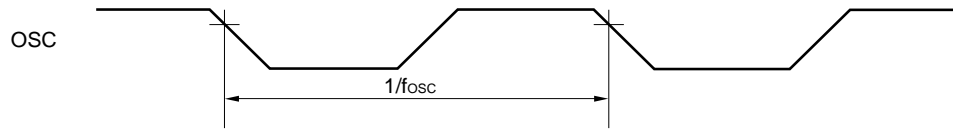
68 Series MPU Read/Write Timing



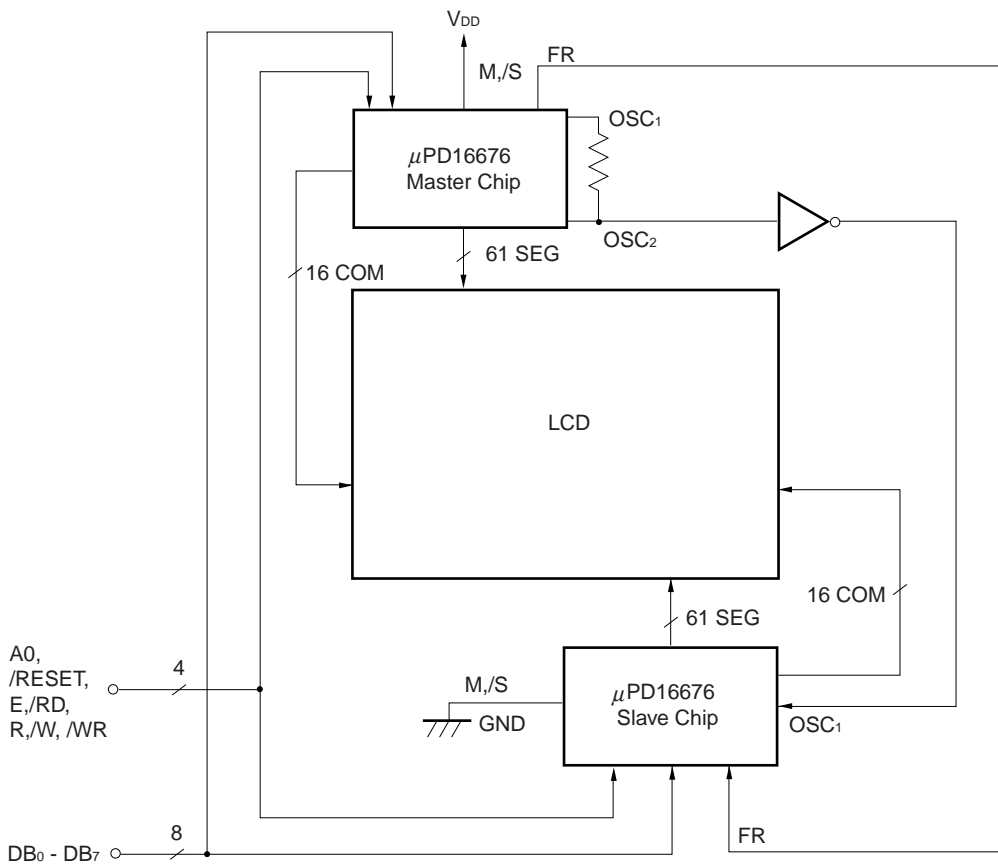
Reset



OSC

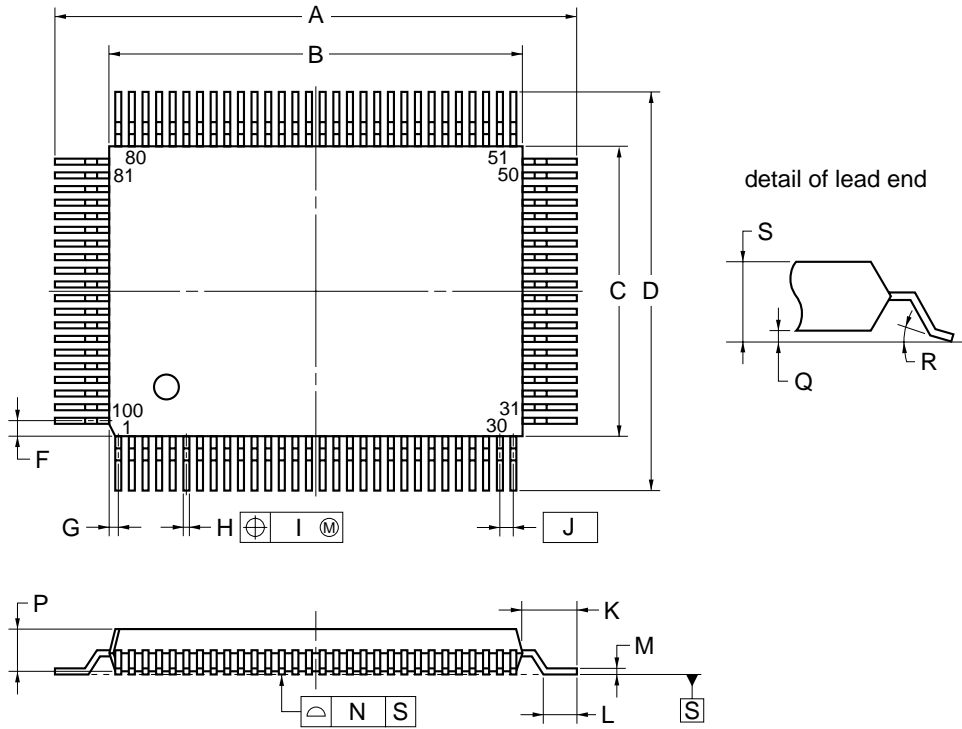


★ 10. Application Circuit Example



★ 11. PACKAGE DRAWING

100 PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.2±0.2
B	20.0±0.2
C	14.0±0.2
D	17.2±0.2
F	0.8
G	0.6
H	0.32±0.08
I	0.15
J	0.65 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	0.17 ^{+0.08} _{-0.07}
N	0.10
P	2.7
Q	0.125±0.075
R	5°±5°
S	2.825±0.175

S100GF-65-3BA-4

★ 12. RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μ PD16676.

Type of Surface Mount Device

μ PD16676GF-3BA : 100-PIN PLASTIC QFP (14 x 20 mm)

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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 - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
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