V63C430
2 x 8K x 16 BIT/16K x 16 BIT CACHE CMOS STATIC RAM

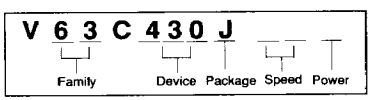
PRELIMINARY

Features

- Designed for 64KB, 128KB, and 256KB implementation
- Direct interface to 82385, A38202, C395e, 82C482 and 82C312 Cache Controllers
- High Speed
  - Designed for 80386 and 80486 systems up to 40/33/25/20 MHz
  - Maximum access time of 18/20/25/30 ns
  - Output Enable access time of 8/10 ns
  - Write Pulse width of 10 ns
- Fast input-address latch
- High Output driveability – 100 pF
- Low Power
  - Full CMOS Design offers lower standby power
  - Internal Automatic Power Down feature provides low operating current
- Supports Direct Mapped and 2-way Set Associative Cache Scheme
- Two $\overline{WE}$ and two $\overline{OE}$ control pins
- Separate Upper and Lower Byte Select
- Multiple power buses for optimum noise reduction
- Available in 52 pin PLCC

Description

The V63C430 is a high performance, full CMOS, 2 x 8K x 16, 256K cache memory. This highly integrated solution is specifically designed to provide direct interface to the 80386 and 80486 32-bit CPU and to most industry standard cache controllers. Built-in Mode Control allows the user to configure the memory internally as either one 16K x 16 memory, or two 8K x 16 memories through the use of a programmable MODE pin. Two V63C430 chips may be used in parallel to provide 64K bytes, and four chips provide 128KB of cache memory for high performance 32-bit personal computers and CAD/CAM engineering workstations that use the Intel 386/486 microprocessor. The Cache RAM works with systems running at speeds of 40, 33, 25 and 20 MHz.



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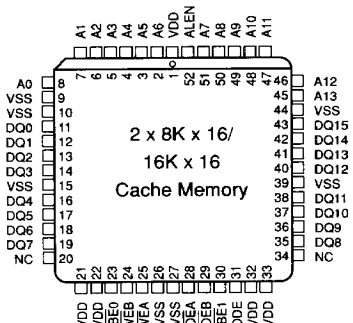
PLCC PIN CONFIGURATION Top View



Speed Selection Guide

Clock Speed	*V63C430 Speed*
20 MHz	01
25 MHz	02
33 MHz	03
40 MHz	04

Package	*Sym*	*Pin Count*
Plastic LCC	J	52

Operating Temperature Range	Package Outline	Access Time (ns)					Power Temperature Mark
	J	18 (04)	20 (03)	25 (02)	30 (01)	Std.	
0°C to 70°C	•	•	•	•	•	•	Blank

V63C430 Rev. 01 April 1990

Functional Block Diagrams

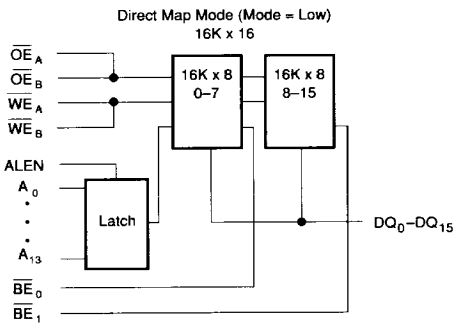


Figure 1.

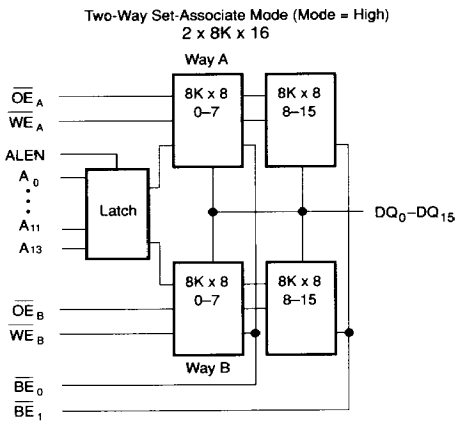


Figure 2.

Functional Description

The 2 x 8K x 16 Cache Memory consists of four 8K x 8 SRAMs (Figures 1 & 2) which can function as:

1. 16K x 16 direct mapped cache, or
2. 8K x 16 2-way set associate cache

The operation of the V63C430 cache memory is controlled by the MODE control, $\overline{WE}$ and $\overline{OE}$ as shown in Table 1.

Table 1.

Description	Mode	$\overline{WE}$ (A, B)	$\overline{OE}$ (A, B)
Direct Map	0	Tied together as $\overline{WE}_1$	Tied together as $\overline{OE}_1$
2-way Set Associative	1	$\overline{WE}$ (A) = $\overline{WE}_1$ $\overline{WE}$ (B) = $\overline{WE}_2$	$\overline{OE}$ (A) = $\overline{OE}_1$ $\overline{OE}$ (B) = $\overline{OE}_2$

The mode control alters the addresses to the internally configured 8K x 8 SRAMs through the on-chip address logic as follows:

Mode = 0, A_0–A_{13} same as chip address inputs

Mode = 1, A_{12} always grounded, others same as chip address inputs

Two 16K x 16 cache memories may be used in parallel to provide 64K bytes of cache to the Intel 82385 with double word, word, and byte transfers controlled by Byte Enable $\overline{BE}_0$ and $\overline{BE}_1$ pairs. The V63C430 can be interfaced directly to the 80386/80486 system without external address latches or data transceivers. It is designed for systems operating at speeds up to 40 MHz. In a 2-way set associative 64KB cache configuration, two V63C430's replace eight 8K x 8 SRAM's, two 74F373's, and eight 74F245 devices.

Pin Description

A_0–A_{13}	Addresses
DQ_0–DQ_{15}	Data Inputs/Outputs
ALEN	Address Latch Enable
MODE	Mode
$\overline{BE}_0$, $\overline{BE}_1$	Byte Enables
$\overline{OE}_A$, $\overline{OE}_B$	Output Enables
$\overline{WE}_A$, $\overline{WE}_B$	Write Enables
V_{DD}	+5 V Power
V_{SS}	Ground

Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	−0.5* to +7.0	V
V_T	Terminal Voltage with Respect to V_{SS}	−0.5* to V_{DD} +0.5	V
t_{OPR}	Operating Temperature	0 to +70	°C
t_{STG}	Storage Temperature	−55 to +125	°C

* −3.5V for 20 ns pulse.

NOTE: 1. Operation above absolute maximum rating can affect device reliability.

Truth Table

$\overline{BE}_0$	$\overline{BE}_1$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	Operation
H	H	X	X	X	X	Standby, All Outputs High-Z
X	X	H	H	H	H	All Outputs High-Z
L	H	L	H	H	H	Read low byte, Select Way A
L	H	H	L	H	H	Read low byte, Select Way B
L	H	X	X	L	H	Write low byte, Select Way A
L	H	X	X	H	L	Write low byte, Select Way B
H	L	L	H	H	H	Read high byte, Select Way A
H	L	H	L	H	H	Read high byte, Select Way B
H	L	X	X	L	H	Write high byte, Select Way A
H	L	X	X	H	L	Write high byte, Select Way B
L	L	L	H	H	H	Read word, Select Way A
L	L	H	L	H	H	Read word, Select Way B
L	L	X	X	L	H	Write word, Select Way A
L	L	X	X	H	L	Write word, Select Way A

NOTE: In direct mapped cache mode, A_{12} is used to control Reads and Writes from Way A and Way B.

*Capacitance**

T_A = 25°C, f = 1MHz

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	pF

***NOTE:** These parameters are sampled and not 100% tested.

Recommended DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, unless otherwise noted.

Parameter	Symbol	Speed	Min.	Max.	Units	Test Condition
Supply Voltage	V_{DD}		4.75	5.25	V	
Supply Voltage	V_{SS}		0.0	0.0	V	
Input High Voltage	V_{IH}		2.2	V_{DD}+.3	V	
Input Low Voltage	V_{IL}		−0.5*	+0.8	V	
Input Leakage Current	I_{LI}		−10	10	µA	V_{DD} = 5.25 V, V_{IN} = V_{SS} to V_{DD}
Output Leakage Current	I_{LO}		−10	10	µA	$\overline{BE}_0$ = V_{IH}, $\overline{BE}_1$ = V_{IH} V_{OUT} = V_{SS} to V_{DD}
Read Operating Current	I_{DD1}	01		140	mA	Cycle Time = 100ns, Duty Cycle = 100%
	I_{DD2}	02		175	mA	Cycle Time = 80ns, Duty Cycle = 100%
	I_{DD3}	03		240	mA	Cycle Time = 60ns, Duty Cycle = 100%
	I_{DD4}	04		275	mA	Cycle Time = 50ns, Duty Cycle = 100%
Write Operating Current	I_{DD5}	01		180	mA	Cycle Time = 100ns, Duty Cycle = 100%
	I_{DD6}	02		220	mA	Cycle Time = 80ns, Duty Cycle = 100%
	I_{DD7}	03		250	mA	Cycle Time = 60ns, Duty Cycle = 100%
	I_{DD8}	04		275	mA	Cycle Time = 50ns, Duty Cycle = 100%
CMOS Standby Current	I_{SB}			20	mA	$\overline{BE}_0$ = $\overline{BE}_1$ ≥ V_{DD}−0.2 V, V_{DD} = Max. V_{IH} ≥ V_{DD} -0.2 V, V_{IL} ≤ V_{SS} +0.2 V,
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}		2.4		V	I_{OH} = −1.0 mA

* −3.5V for 20 ns pulse.

AC Test Loads

Signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0.0 V to 3.0 V, output loading as shown in the diagrams below.

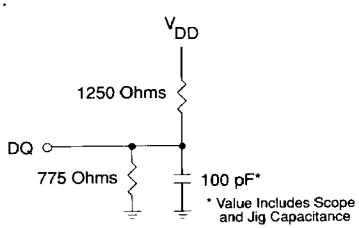


Figure 3. Output Load.

AC Test Conditions

(Applies to READ and WRITE Cycle Timing)

Input Pulse High Level	V_{IH} = 3.0 V
Input Pulse Low Level	V_{IL} = 0.0 V
Input Rise Time	t_R = 3 ns
Input Fall Time	t_F = 3 ns
Input and Output Reference Level	1.5 V
Output Load	C_L = 100 pF, 1 TTL
V_{DD}	5V ± 5%
T_A	0° to +70°C

AC Characteristics

At recommended operating conditions, unless otherwise noted.

Read Cycle (4)

Symbol	Parameter	01		02		03		04		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	30		25		20		18		ns	1
t_{AA}	Address Access Time / ALEN Access Time		30		25		20		18	ns	
t_{BES}	Byte Enable Access Time		30		25		20		18	ns	
t_{OE}	Output Enable to Output Valid		10		10		8		8	ns	
t_{OH}	Output Hold from Address Change	5		5		5		5		ns	
t_{LZ}	Byte Enable to Output in Low-Z	5		5		5		5		ns	2, 3
t_{OLZ}	Output Enable to Output in Low-Z	2		2		2		2		ns	2, 3
t_{BHZ}	Byte Disable to Output in High-Z		10		10		8		8	ns	2, 3
t_{OHZ}	Output Disable to Output in High-Z		7		7		7		7	ns	2, 3
t_{AP}	Address Latch Enable Pulse Width	8		8		8		8		ns	
t_{ASLL}	Address Setup to Latch Low	4		4		4		4		ns	
t_{AHLL}	Address Hold to Latch Low	5		5		2		2		ns	

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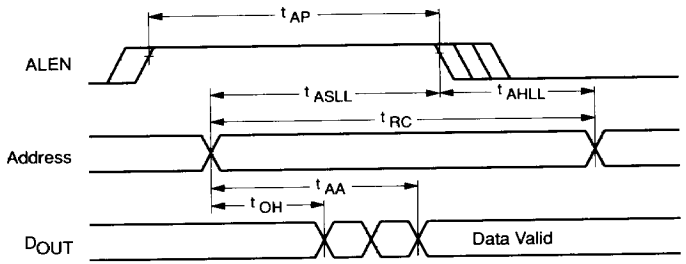
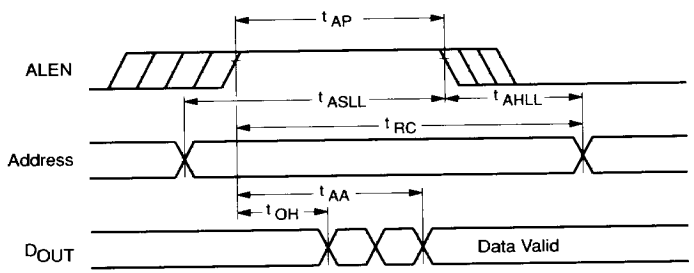
Notes:

1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 500 mV from low or high voltage with load (see Figure 3).
4. $\overline{WE}$ is High for read cycle.

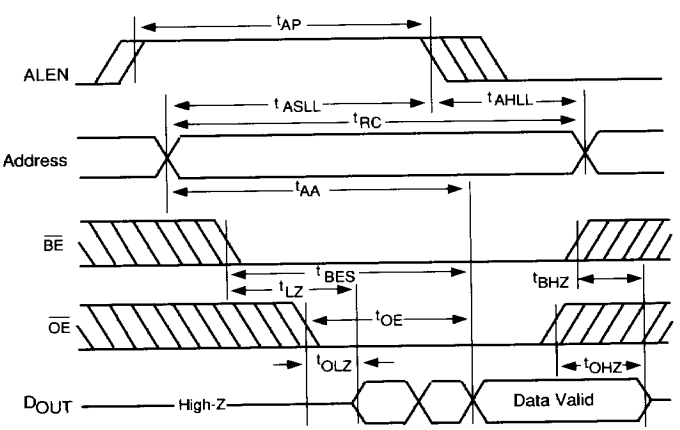
Timing Waveforms of Read Cycle No. 1 (Address Controlled) (4)



Timing Waveforms of Read Cycle No. 2 (ALEN Controlled) (4)



Timing Waveforms of Read Cycle No. 3 (4)



Write Cycle (1, 4, 5, 6)

Symbol	Parameter	01		02		03		04		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	30		25		20		18		ns	
t_{AW}	Address Valid to End of Write	25		20		18		18		ns	
t_{CW}	Byte Select to End of Write	18		16		12		10		ns	
t_{DW}	Data Valid to End of Write	10		10		10		8		ns	
t_{WP}	Write Pulse Width	15		15		12		10		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{WR}	Write Recovery Time ($\overline{WE}$)	0		0		0		0		ns	
t_{LZ}	Chip Enable to Output in Low-Z	5		5		5		5		ns	2,3
t_{AP}	Address Latch Enable Pulse Width	8		8		8		8		ns	
t_{ASLL}	Address Setup to Latch Low	4		4		4		4		ns	
t_{AHLL}	Address Hold to Latch Low	5		5		2		2		ns	
t_{OHZ}	Output Disable to Output in High-Z		7		7		7		7	ns	2,3
t_{OLZ}	Output Enable to Output in Low-Z	2		2		2		2		ns	2,3

Notes:
1. A write occurs during the overlap of low $\overline{BE}$, and a low $\overline{WE}$.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 500 mV from low or high voltage with load (see Figure 3).
4. $\overline{BE}$ or $\overline{WE}$ must be high during address transition.
5. If $\overline{OE}$ is high, I/O pins remain in an high impedance state.
6. $\overline{BE}$ must remain static during the Write Cycle, i.e. when $\overline{WE}$ is low. The Write Cycle can only be controlled by the $\overline{WE}$ pulse.

Timing Waveforms of Write Cycle (1, 4, 5)