REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated test load circuit and table.	96-02-14	M. A. Frye
B	Added case outline "Y". Updated boilerplate.	97-06-23	Raymond Monnin

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B												
SHEET	15	16	17	18	19	20	21	22												
REV STATUS OF SHEETS		REV		B	B	B	B	B	B	B	B	B	B	B	B	B	B			
		SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Gary L. Gross	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216-5000**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Jeff Bowling	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, MEMORY, DIGITAL, 1024 X 18 CLOCKED FIFO, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 95-11-09	SIZE **A** / CAGE CODE **67268** / **5962-95627**
	REVISION LEVEL B	SHEET 1 OF 22

DSCC FORM 2233
APR 97

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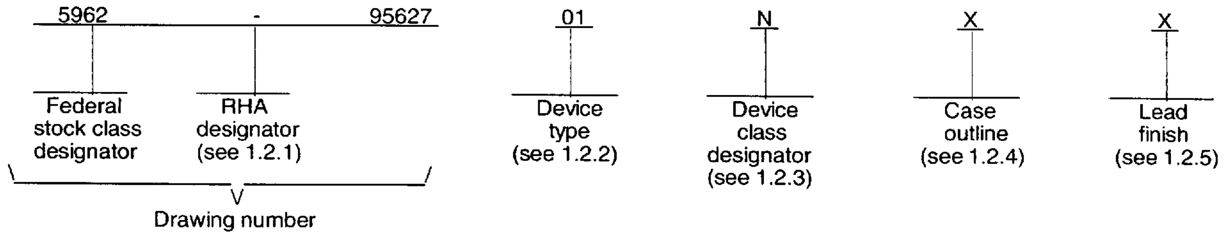
1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ACT7881	1024 X 18 clocked FIFO

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
N	Certification and qualification to MIL-PRF-38535 with a non-traditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
X	MS-026 BDD	80	Plastic quad flat package	JEP 95
Y	See figure 1	68	Ceramic quad flat package	---

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.2.5.1 Lead finish D. Lead finish D shall be designated by a single letter as follows:

Finish letter	Process
D	Palladium

1/ Any device outside the traditional performance environment; i.e., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

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1.3 Absolute maximum ratings. 2/ 3/ 4/

Supply voltage range (V_{CC}) .... -0.5 V dc to +7.0 V dc
DC input voltage (V_{IN}) .... 7.0 V dc
Voltage applied to a disabled 3-state output .... 5.5 V dc
Operating free-air temperature range (T_A) .... -55°C to +125°C
Storage temperature range (T_{STG}) .... -65°C to +150°C

1.4 Recommended operating conditions. 3/ 4/

Supply voltage range (V_{CC}) .... +4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL}) .... +0.8 V
Minimum high level input voltage (V_{IH}) .... +2.0 V
Maximum high level output current (I_{OH}) .... -8.0 mA
Maximum low level output current (I_{OL}) .... +16.0 mA
Case operating temperature range (T_C) .... -55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) .... XX percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Unless otherwise noted, all voltages are referenced to GND.
4/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
5/ Values will be added when they become available.

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2.2 Non-Government publication. The following document forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices.

JEDEC STANDARD No. 17 - A Standard Test Procedure for the characterization of latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be i accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operatin temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5 V \le V_{CC} \le +5.5 V$ unless otherwise specified		Device types	Group A subgroups 2/	Limits 3/		Unit
						Min	Max	
High level output voltage	V_{OH}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V, I_{OH} = -8.0 mA, V_{CC} = 4.5 V		01	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V, I_{OL} = 16 mA, V_{CC} = 4.5 V		01	1, 2, 3		0.5	V
Input current	I_I 4/	For input under test, $V_I = V_{CC}$ or GND, V_{CC} = 5.5 V		01	1, 2, 3		±5	µA
Three-state output leakage current high	I_{OZH} 5/	For control input affecting output under test, V_{IN} = 2.0 V or 0.8 V, $V_{OUT} = V_{CC}$, V_{CC} = 5.5 V		01	1, 2, 3		5	µA
Three-state output leakage current low	I_{OZL} 5/	For control input affecting output under test, V_{IN} = 2.0 V or 0.8 V, V_{OUT} = GND, V_{CC} = 5.5 V		01	1, 2, 3		-5	µA
Quiescent supply current	I_{CC} 6/	For input under test, $V_{IN} = V_{CC}$-0.2V or 0 V_{CC} = 5.5 V		01	1, 2, 3		400	µA
		One input at 3.4 V. For all other inputs $V_{IN} = V_{CC}$ or GND. V_{CC} = 5.5 V					1.2	mA
Input capacitance	C_{IN}	T_A = +25°C, V_{BIAS} = 0 V V_{CC} = 5.0 V, See 4.4.1e f = 1 MHz	V_I = 0	01	4		4	pF
Output capacitance	C_O		V_O = 0		4		8	
Functional tests	7/	V_{IH} = 2.0 V, V_{IL} = 0.8 V, verify output V_O, V_{CC} = 4.5 V and 5.5 V, 4.4.1c		01	7, 8A, 8B	L	H	
Clock frequency CLKA or CLKB	f_{clock}	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5V, see figure 3 as applicable		01	9, 10, 11	50		MHz
Pulse duration, WRTCLK high	t_{w1}			01	9, 10, 11	7		ns
Pulse duration, WRTCLK low	t_{w2}			01	9, 10, 11	7		
Pulse duration, RDCLK high	t_{w3}			01	9, 10, 11	7		
Pulse duration, RDCLK low	t_{w4}			01	9, 10, 11	7		
Pulse duration, $\overline{DAF}$ high	t_{w5}			01	9, 10, 11	7		
Setup time, D0-D17 before WRTCLK↑	t_{su1}			01	9, 10, 11	5		
Setup time, WRTEN1, WRTEN2 high before WRTCLK↑	t_{su2}			01	9, 10, 11	5		
Setup time, OE, RDEN1, RDEN2 high before RDCLK↑	t_{su3}			01	9, 10, 11	5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Test conditions 1/ $-55°C \leq T_C \leq +125°C$ $+4.5 V \leq V_{CC} \leq +5.5 V$ unless otherwise specified	Device types	Group A subgroups 2/	Limits 3/		Unit
					Min	Max	
Setup time, Define AF/AE: D0-D8 before $\overline{DAF}$ ↓	t_{su4}	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, see figure 3 as applicable	01	9, 10, 11	5		ns
Setup time, Define AF/AE: $\overline{DAF}$ ↓ before $\overline{RESET}$ ↑	t_{su5}		01	9, 10, 11	6		
Setup time, Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$ ↑	t_{su6}		01	9, 10, 11	5		
Hold time, D0-D17 after WRTCLK ↑	t_{h1}		01	9, 10, 11	0		
Hold time, WRTEN1, WRTEN2 high after WRTCLK ↑	t_{h2}		01	9, 10, 11	0		
Hold time, OE, RDEN1, RDEN2 high after RDCLK ↑	t_{h3}		01	9, 10, 11	0		
Hold time, Define AF/AE: D0-D8 after $\overline{DAF}$ ↓	t_{h4}		01	9, 10, 11	1		
Hold time, Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$ ↑	t_{h5}		01	9, 10, 11	0		
Hold time, Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$ ↑	t_{h6}		01	9, 10, 11	0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions 2/ $-55°C \leq T_C \leq +125°C$ $+4.5 V \leq V_{CC} \leq +5.5 V$ unless otherwise specified	Device types	Group A subgroups 3/	Limits 4/		Unit
					Min	Max	
Maximum frequency WRTCLK or RDCLK	f_{max}	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, see figure 3 as applicable	01	9, 10, 11	50		MHz
Propagation delay time, RDCLK↑ to any Q	t_{pd1}		01	9, 10, 11	3	13	ns
Propagation delay time, WRTCLK↑ to IR	t_{pd2}		01	9, 10, 11	2	9.5	
Propagation delay time, RDCLK↑ to OR	t_{pd3}		01	9, 10, 11	2	9.5	
Propagation delay time, WRTCLK↑ or RDCLK↑ to AF/AE	t_{pd4}		01	9, 10, 11	6	19	
Propagation delay time, WRTCLK↑ or RDCLK↑ to HF	t_{PLH1} t_{PHL1}		01	9, 10, 11	6	17	
Propagation delay time, $\overline{RESET}$↓ to AF/AE	t_{PLH2}		01	9, 10, 11	3	17	
Propagation delay time, $\overline{RESET}$↓ to HF	t_{PHL2}				3	19	
Propagation delay time, output enable OE to any Q	t_{en}		01	9, 10, 11	2	11	
Propagation delay time, output disable, OE to any Q	t_{dis}		01	9, 10, 11	2	14	

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \geq 3.0$ V.

2/ For device class N, all limits for Subgroups 1, 3, 7, 8B, 9 and 11 are guaranteed but not production tested. These limits are characterized at qualification. Production testing is performed at maximum operating temperature.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ For I/O ports, the limit includes I_{OZH} or I_{OZL} leakage current from the output circuitry.

5/ For I/O ports, the limit includes I_I leakage current from the input circuitry.

6/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.0 mA, and the preferred method and limits are guaranteed.

7/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

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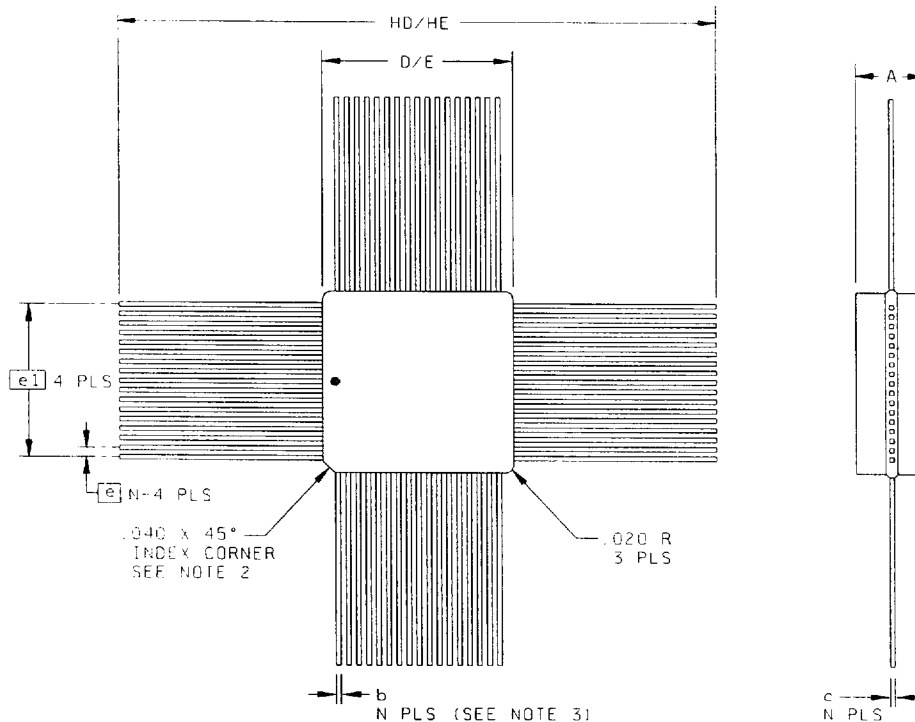

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
HD/HE	33.02	38.10	1.300	1.500
D/E	12.32	12.70	.485	.500
A	3.404	3.912	.134	.154
b	0.203	0.330	.008	.013
e	0.635 BSC		.025 BSC	
e1	10.160 BSC		.400 BSC	
c	0.127	0.178	.005	.007
N	68		68	

NOTES:

1. The US government preferred system of measurement is the metric SI system. However, this item is originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. A terminal 1 identification mark shall be located on the first side clockwise from the index corner. Terminal numbers shall increase in a counterclockwise direction when viewed as shown.
3. N is the maximum number of terminals.

FIGURE 1. Case outline.

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Device type	01				
Case outline	X	Y		X	Y
Terminal number	Terminal symbol	Terminal symbol	Terminal number	Terminal symbol	Terminal symbol
1	NC	$\overline{\text{RESET}}$	41	NC	Q2
2	GND	OE	42	GND	Q3
3	GND	RDEN2	43	WRTCLK	V_{CC}
4	Q16	RDEN1	44	WRTEN1	Q4
5	Q17	RDCLK	45	WRTEN2	GND
6	V_{CC}	GND	46	V_{CC}	Q5
7	OR	D17	47	AF/AE	Q6
8	GND	D16	48	GND	V_{CC}
9	V_{CC}	D15	49	GND	Q7
10	$\overline{\text{RESET}}$	D14	50	IR	Q8
11	OE	D13	51	HF	GND
12	RDEN2	D12	52	V_{CC}	Q9
13	RDEN1	D11	53	Q0	Q10
14	RDCLK	D10	54	Q1	V_{CC}
15	GND	D9	55	GND	Q11
16	D17	V_{CC}	56	Q2	Q12
17	D16	D8	57	Q3	GND
18	D15	GND	58	NC	Q13
19	NC	D7	59	V_{CC}	Q14
20	NC	D6	60	V_{CC}	V_{CC}
21	NC	D5	61	Q4	Q15
22	D14	D4	62	GND	GND
23	D13	D3	63	GND	Q16
24	D12	D2	64	Q5	Q17
25	D11	D1	65	Q6	V_{CC}
26	D10	D0	66	V_{CC}	OR
27	D9	$\overline{\text{DAF}}$	67	Q7	GND
28	V_{CC}	GND	68	Q8	V_{CC}
29	D8	WRTCLK	69	GND	---
30	GND	WRTEN1	70	Q9	---
31	D7	WRTEN2	71	Q10	---
32	D6	V_{CC}	72	V_{CC}	---
33	D5	AF/AE	73	Q11	---
34	D4	GND	74	Q12	---
35	D3	IR	75	GND	---
36	D2	HF	76	GND	---
37	D1	V_{CC}	77	Q13	---
38	D0	Q0	78	Q14	---
39	$\overline{\text{DAF}}$	Q1	79	V_{CC}	---
40	NC	GND	80	Q15	---

FIGURE 2. Terminal connections.

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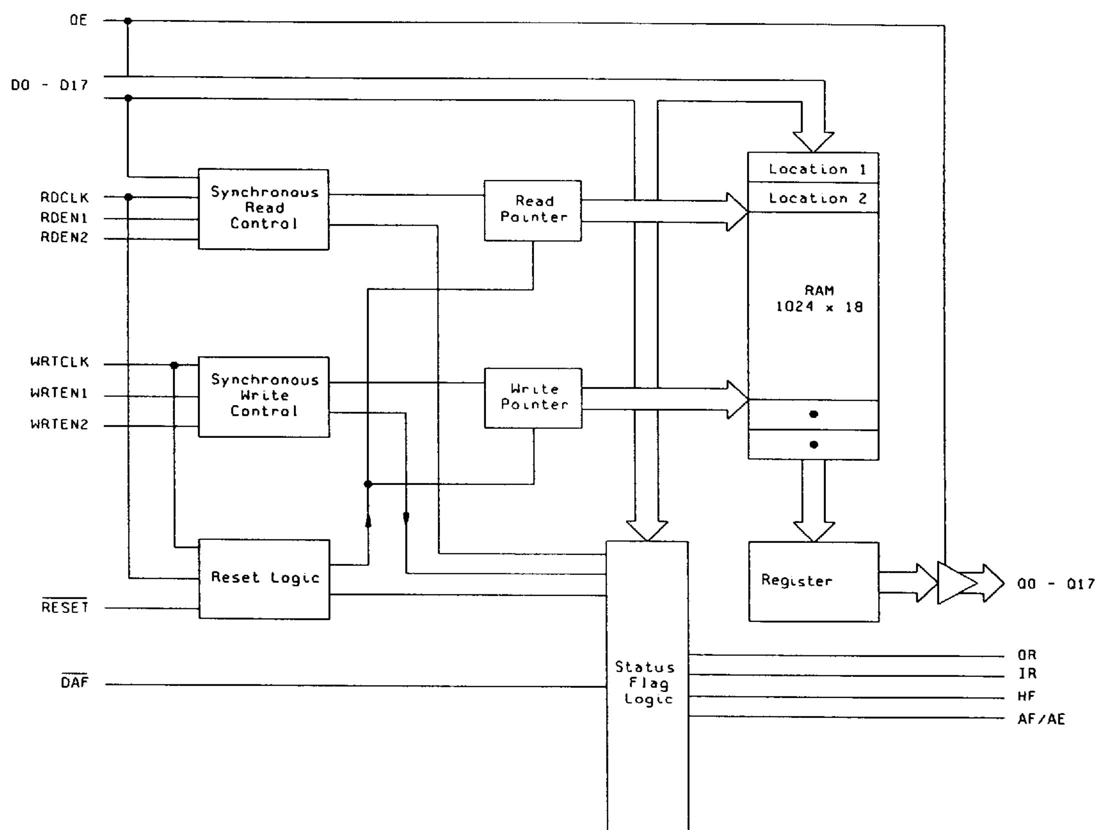

FIGURE 3. Block diagram.

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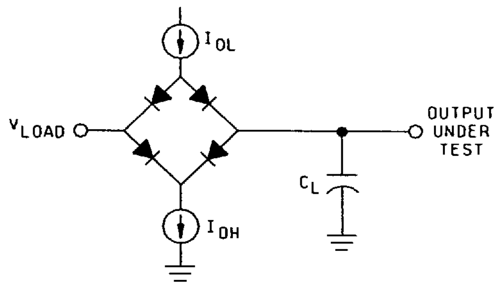
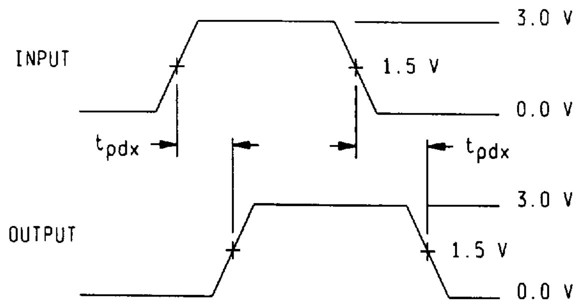
STANDARD CMOS OUTPUTS

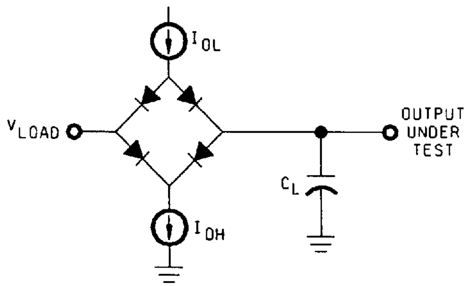


LOAD CIRCUIT

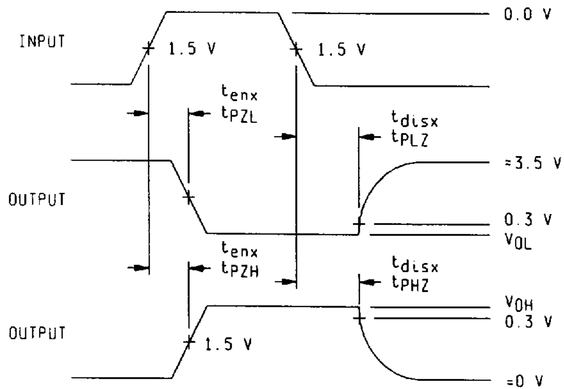


TOTEM-POLE OUTPUTS

3-STATE OUTPUTS (ANY Q)



LOAD CIRCUIT



VOLTAGE WAVEFORMS

Parameter		I_{OL}	I_{OH}	V_{LOAD}	C_L (see note)
t_{en}	t_{PZH}	8 mA	8 mA	0 V	20 pF
	t_{PZL}	8 mA	8 mA	3.5 V	20 pF
t_{dis}	t_{PHZ}	8 mA	8 mA	1.5 V	20 pF
	t_{PLZ}	8 mA	8 mA	1.5 V	20 pF
t_{pd}		16 mA	8 mA	1.5 V	20 pF

NOTE: C_L includes probe and test fixture capacitance

FIGURE 4. Test load circuit and voltage timing waveforms.

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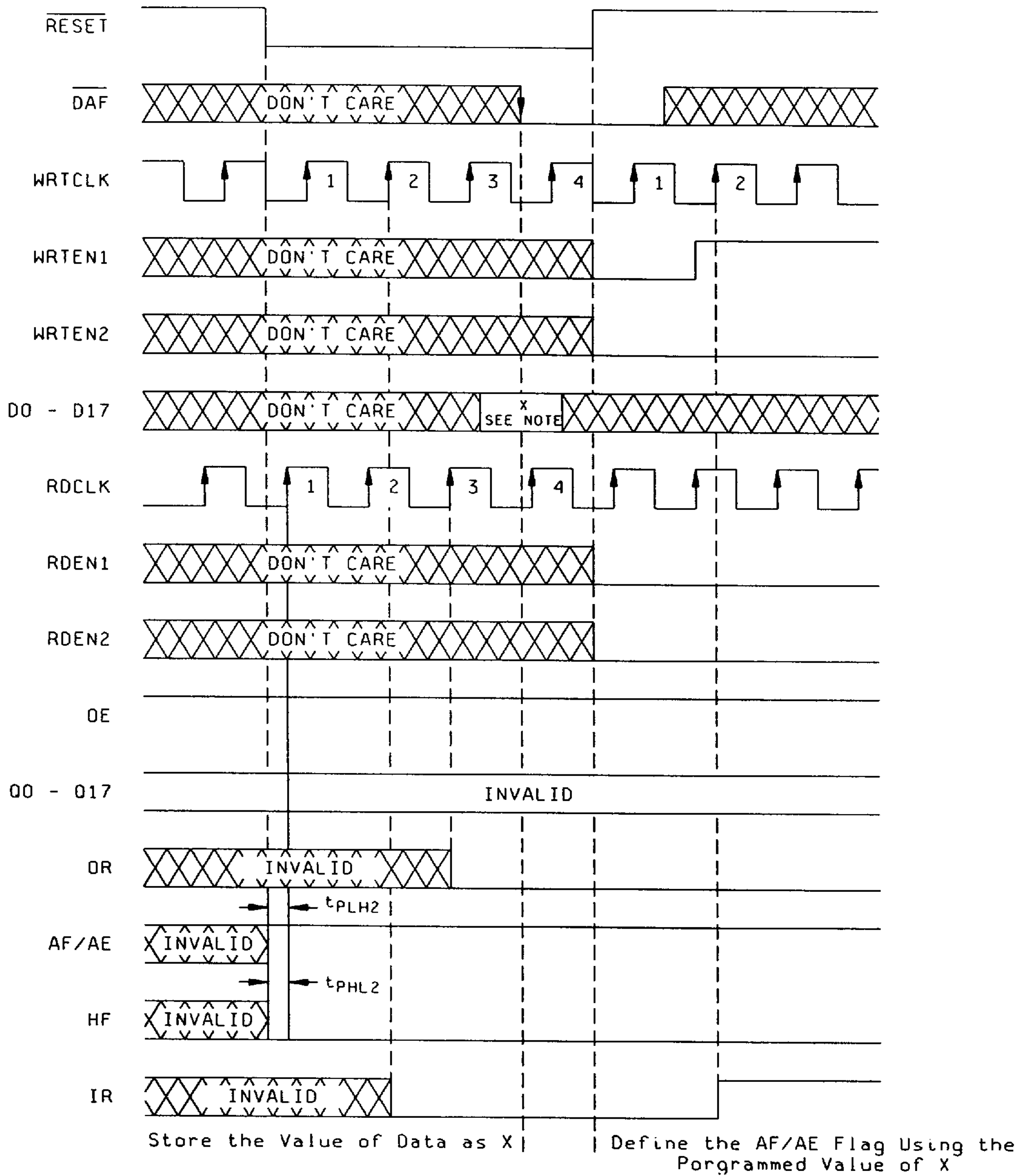
RESET CYCLE: DEFINE AF/AE USING A PROGRAMMED VALUE OF X



NOTE: X is the binary value on D8 - D0.

FIGURE 4. Test load circuit and voltage timing waveforms - Continued.

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RESET CYCLE: DEFINE AF/AE USING THE DEFAULT VALUE

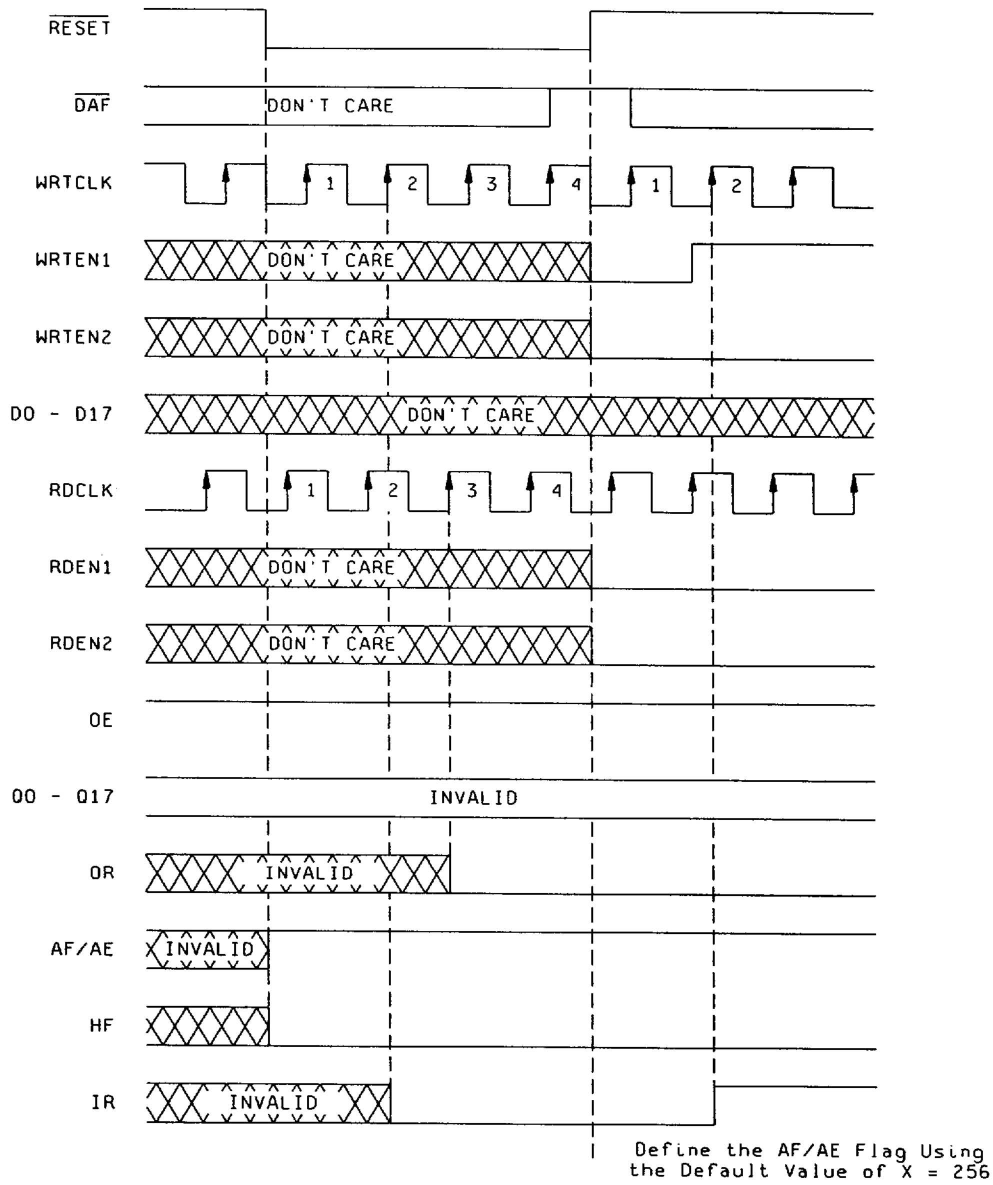

FIGURE 4. Test load circuit and voltage timing waveforms - Continued.

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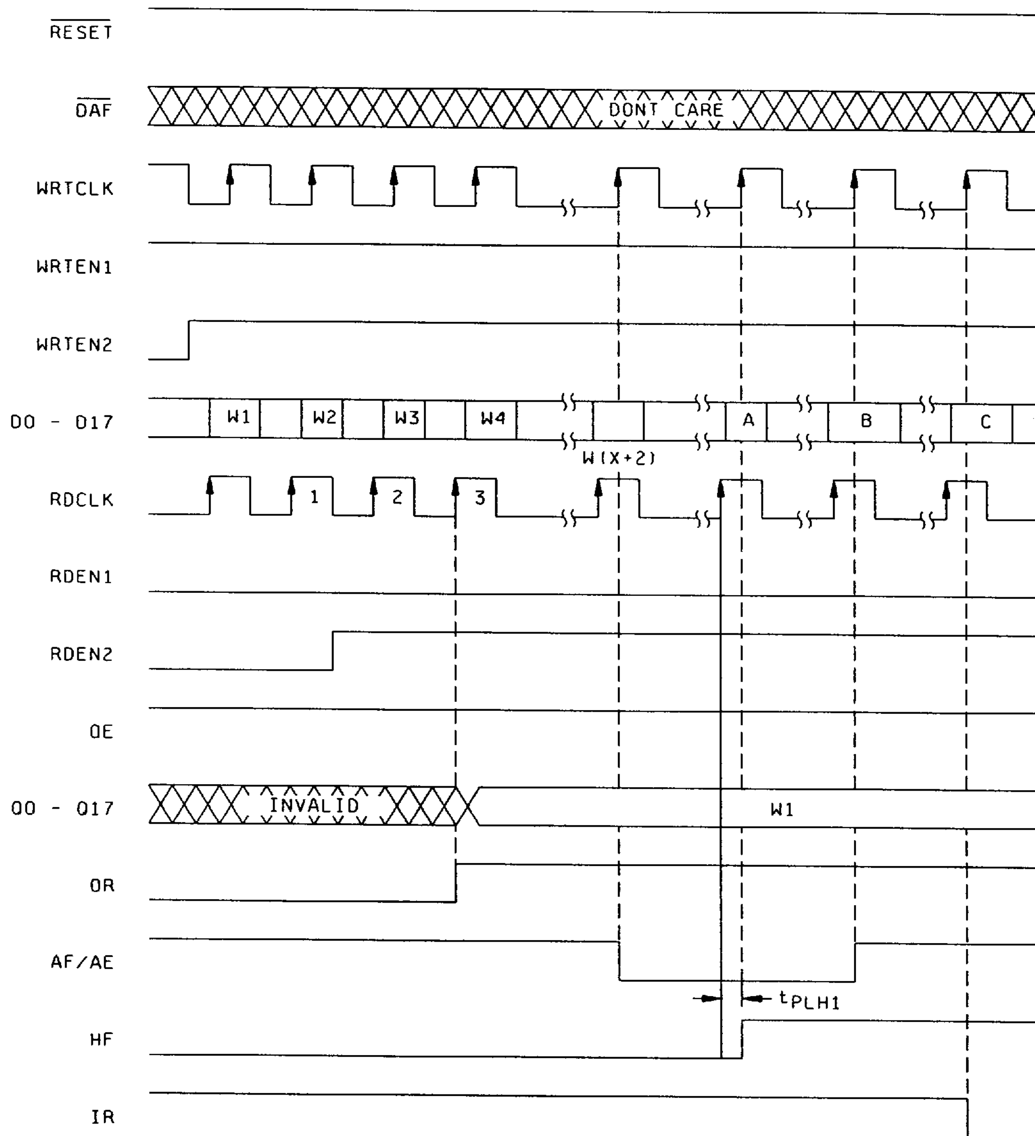
WRITE CYCLE TIMING AND DATA-WORD NUMBERS FOR FLAG TRANSITIONS



Transition word		
A	B	C
W513	W(1025 - X)	W1025

FIGURE 4. Test load circuit and voltage timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-95627
		REVISION LEVEL B	SHEET 14

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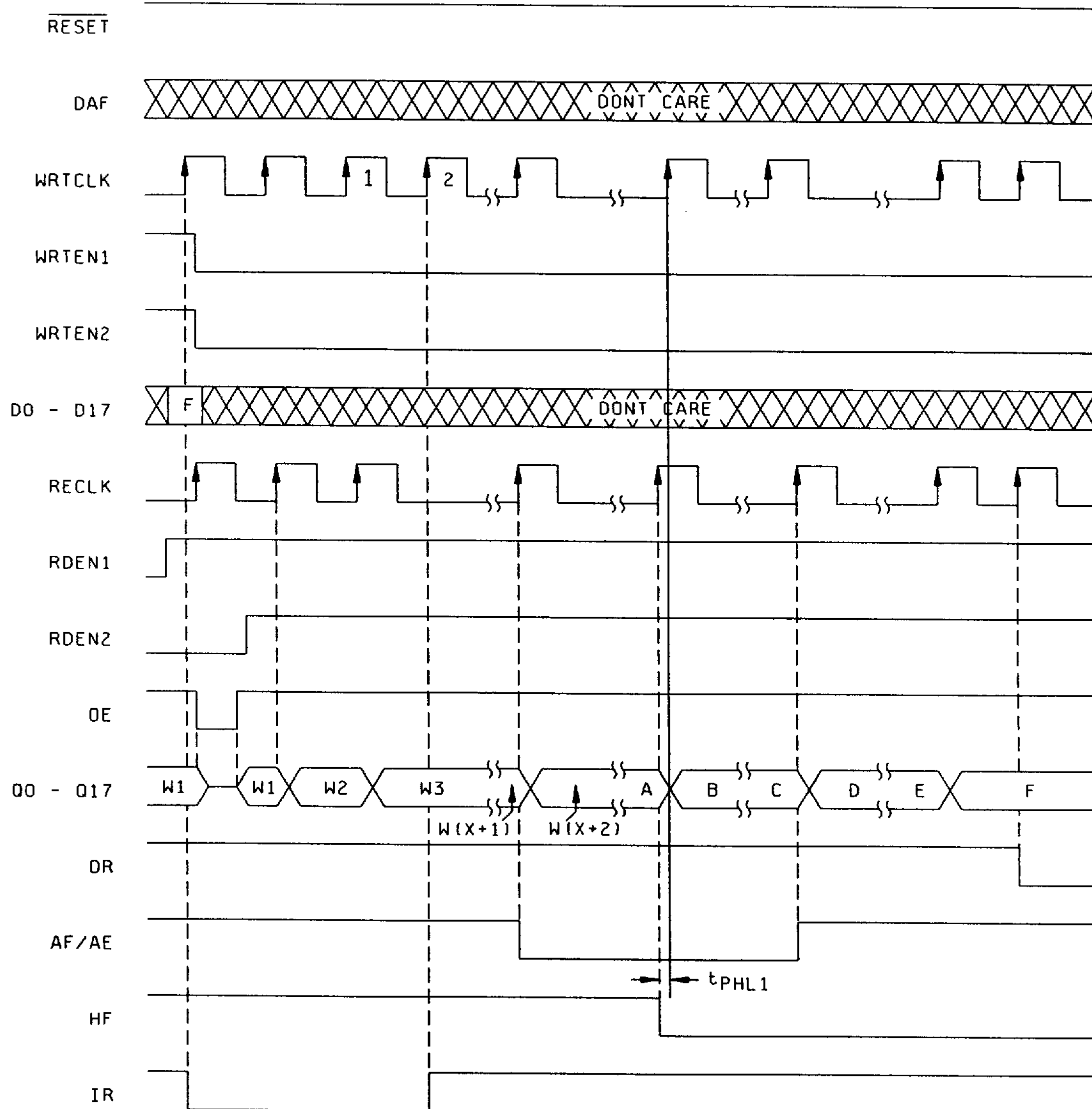
READ CYCLE TIMING AND DATA WORD NUMBERS FOR FLAG TRANSITIONS



Transition word					
A	B	C	D	E	F
W513	W514	W(1024-X)	W(1025-X)	W1024	W1025

FIGURE 4. Test load circuit and voltage timing waveforms - Continued.

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PULSE DURATION, SETUP, AND HOLD TIMING

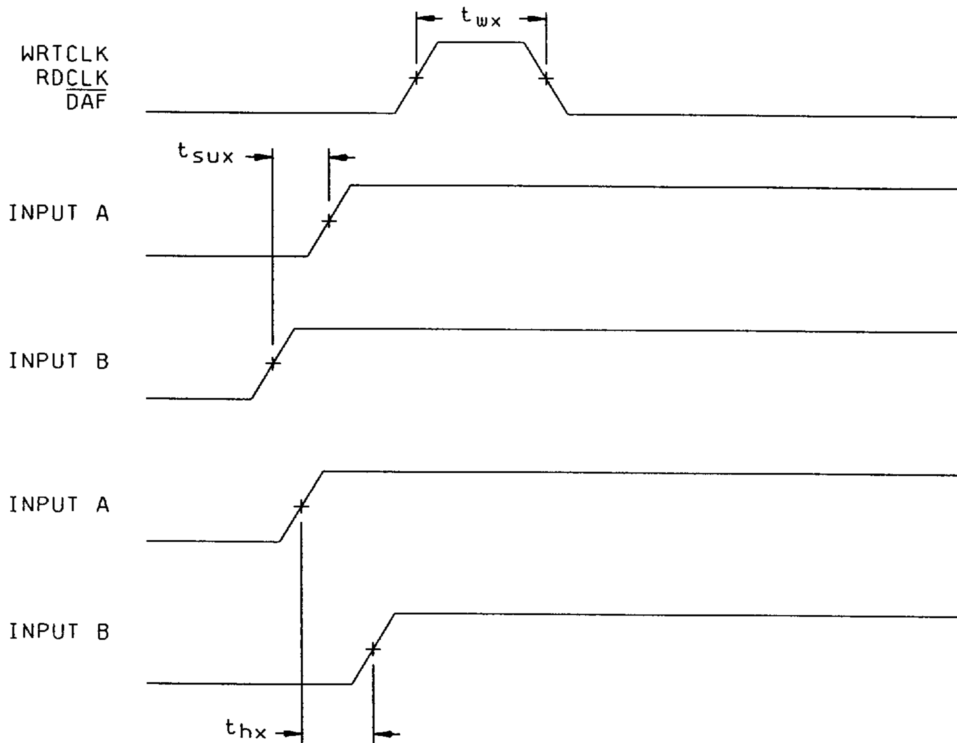

FIGURE 4. Test load circuit and voltage timing waveforms - Continued.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class M	Device class N	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)				1,7,9
2	Static burn-in I and II (method 1015)	Required		Required	Required
3	Same as line 1				1*,7* Δ
4	Dynamic burn-in (method 1015)	Not Required		Not Required	Required
5	Same as line 1				1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	2,8A,10	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	2,8A,10	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B		1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B		2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9		1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

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TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_I	±10%
I_{OZH}, I_{OZL}	±10%

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

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4.2.2 Additional criteria for device classes N, Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes N, Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_O measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

(1) The following shall apply to device class N only. Sample size is five devices with no failures. For C_{IN} and C_O, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN} and C_O tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DSCC-VA the device functions listed in each functional group and the test results for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

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4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and as follows.

Pin name	I/O	Description
AF/AE	I/O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset or the default value of 256 can be used. AF/AE is high when the number of words in memory is less than or equal to X. AF/AE is also high when the number of words in memory is greater than or equal to (1024-X). Programming procedure for AF/AE is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user defined value or the default of X = 256. instructions to program AF/AE using both methods are as follows: User-defined X Step 1: Take $\overline{DAF}$ from high to low. The low-to-high transition of $\overline{DAF}$ input stores the binary value on the data inputs as X. The following bits are used, listed from the most significant bit to least significant bit (D8-D0). Step 2: If $\overline{RESET}$ is not already low, take $\overline{RESET}$ low. Step 3: With $\overline{DAF}$ held low, take $\overline{RESET}$ high. This defines AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{DAF}$ low. Default X To redefine AF/AE using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.
$\overline{DAF}$	I	Define-almost-full. The high-to-low transition of $\overline{DAF}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{DAF}$ held low, a low pulse on $\overline{RESET}$ defines the almost-full/almost-empty (AF/AE) flag using X.
D0-D17	I	Data inputs for 18-bit-wide data to be strored in the memory. A high-to-low transition on $\overline{DAF}$ captures data for the almost-empty/almost-full offset (X) from D8-D0.
HF	O	Half-full flag. HF is high when the FIFO contains 512 or more words and is low when the number of words in memory is less than half the depth of the FIFO.
IR	O	Input-ready flag. IR is ready when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{RESET}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	I	Output enable. The Q0-Q17 outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from the memory.
OR	O	Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0-Q17	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0-Q17 on the rising edge of the third RDCLK pulse to occur after the first valid data write. RDEN1 and RDEN2 do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	I	Read clock. Data is read out of memory on the low-to-high transition at RDCLK if OR, OE, RDEN1, and RDEN2 are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to the RDCLK signal.
RDEN1, RDEN2	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.

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6.5 Abbreviations, symbols, and definitions - continued.

Pin name	I/O	Description
$\overline{\text{RESET}}$	I	Reset. A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, IR are low, AF/AE is high. The FIFO must be reset upon power-up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines AF/AE using the almost-full/almost -empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using the default value of X = 256.
WRTCLK	I	Write clock. Data is written to memory on the low-to-high transition of RDCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	I	Write enable. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-06-23

Approved sources of supply for SMD 5962-95627 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9562701NXD	01295	ACT7881PCB 2/
5962-9562701QYA 3/	01295	SNJ54ACT7881HV

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Devices may not be marked with the PCB suffix due to space constraints.

3/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

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