



## ADE8165

### FEATURES

#### Narrow-band power-line communications IC

- Integrates PHY through networking layer
- Simple host interface

#### Application layer

- Supports DL/T 645-1997 or -2007 China-specific protocol as well as passthrough option

#### Networking layer

- Master/slave architecture
- Designed to work with ADE8155 slave PLC modem ICs
- Supports
  - Dynamic routing
  - Automatic discovery of authenticated devices
  - Logical address management

#### Data link layer

- Automatic baud rate negotiation
- Up to 63-byte packet support

#### Physical layer

- CPFSK modulation
- Choice of two frequency bands
  - Carrier frequencies: 105.5 kHz and 118.7 kHz
  - Carrier frequencies: 74.9 kHz and 84.2 kHz
- Up to 800 bps on a 1-phase network and 2400 bps on a 3-phase network
- Zero-crossing synchronized receive/transmit
- 6-byte physical address for logical address assignment

#### Communication interface

##### UART

- Option to use DL/T 645-1997 or -2007 China-specific application layer interface

#### Package and temperature range

- 40-lead 6 mm × 6 mm LFCSP
- Fully specified for -40°C to +85°C operation

### GENERAL DESCRIPTION

The ADE8165<sup>1</sup> incorporates a high performance ADC and DAC to create a very robust CPFSK power-line communications IC complete with networking functionality. The ADE8165 master modem IC is designed to work with the ADE8155 slave modem IC for a complete power-line communication system.

In an advanced metering infrastructure (AMI) scenario, the ADE8155 slave modem IC is used to connect the energy meter to the power line. Then the ADE8165 master PLC modem is used near the transformer to communicate with multiple meters on one phase. The power-line communication is independent on each phase; therefore, three ADE8165 master PLC modem ICs are used in a PLC module within the concentrator to read meters on all three phases.

A UART communication interface is supported.

For more information on the ADE8165, contact your local sales office at Analog Devices, Inc.

<sup>1</sup> US patents pending.

### FUNCTIONAL BLOCK DIAGRAM

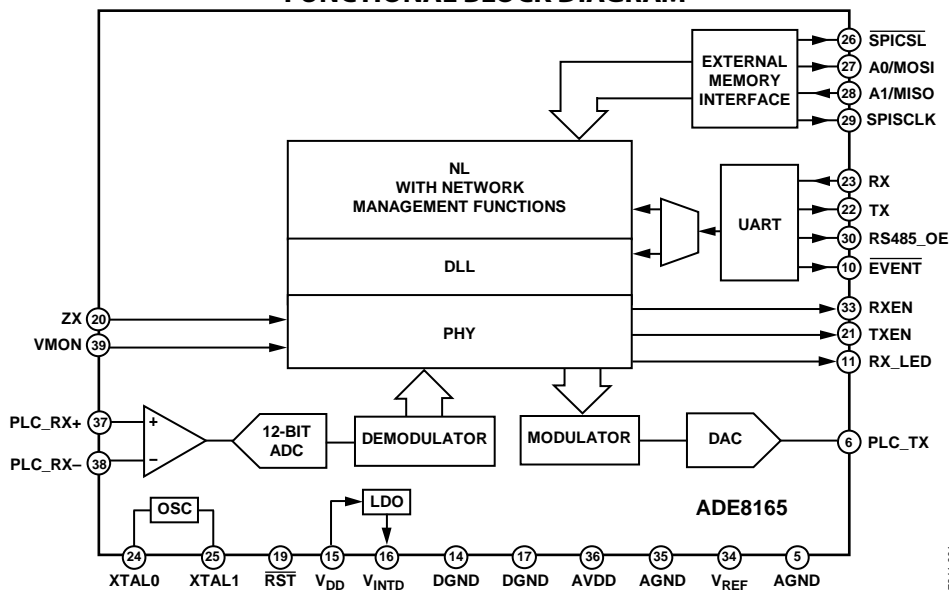


Figure 1.

#### Rev. Sp0

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**NOTES**