Step-Up Converter and LDO Combo

Features

- Built-In a 500mA LDO and Synchronous Step-Up DC-DC Converter
- Built-In PWM/PFM Operating Mode
- Provided Dual Input Power Sources
- Connect FB to OUT for 3.3V Output Voltage or GND for 2.5V Output Voltage or an External Resistor Divider for Adjustable Output Voltage.
- Fixed 300KHz Operating Frequency
- High Efficiency Up to 94% at 200mA Output Current
- 0.6V to 4.5V Operating Voltage
- 1V Start Up Input Voltage
- Low Battery Voltage Detection
- Reverse Voltage Protection
- Internal Synchronous Rectifier
- Automatic Detection Input Voltage
- Compact SOP-8-P and TSSOP-8 Packages
- Lead Free Available (RoHS Compliant)

Applications

- Dual Mode Power System
- USB Peripheral
- Camcorders and Digital Camera
- Hand-held Instrument
- PDAs

General Description

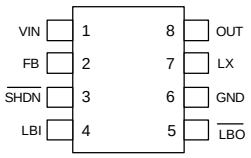
The APW7075 is a PWM/PFM, high-efficiency and step-up DC-DC converter with an integrated LDO input switch for dual mode application. During battery mode operation, the APW7075 acts as synchronous rectifier and step-up DC-DC converter with a fixed or adjustable output voltage. When the VIN pin sense 5V input voltage, the APW7075 is switched to LDO operation mode, maintaining the constant output voltage.

The input voltage ranges from 0.6 V to 4.5V for step-up DC-DC converter. The start-up is guaranteed at1V and the device is operating down to 0.6V. When the device is at LDO operating mode, the suitable output voltage 3.3V and loading current 500mA for maximum power consumption are guaranteed.

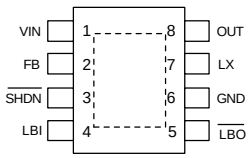
The APW7075 is suited for dual mode and portable battery powered appliance with low-battery detector. In dual-mode applications, the APW7075 draws power from any available 5V USB connection and reverts to battery power when the USB power is removed.

Pin Description

TSSOP-8 Top View



SOP-8-P Top View



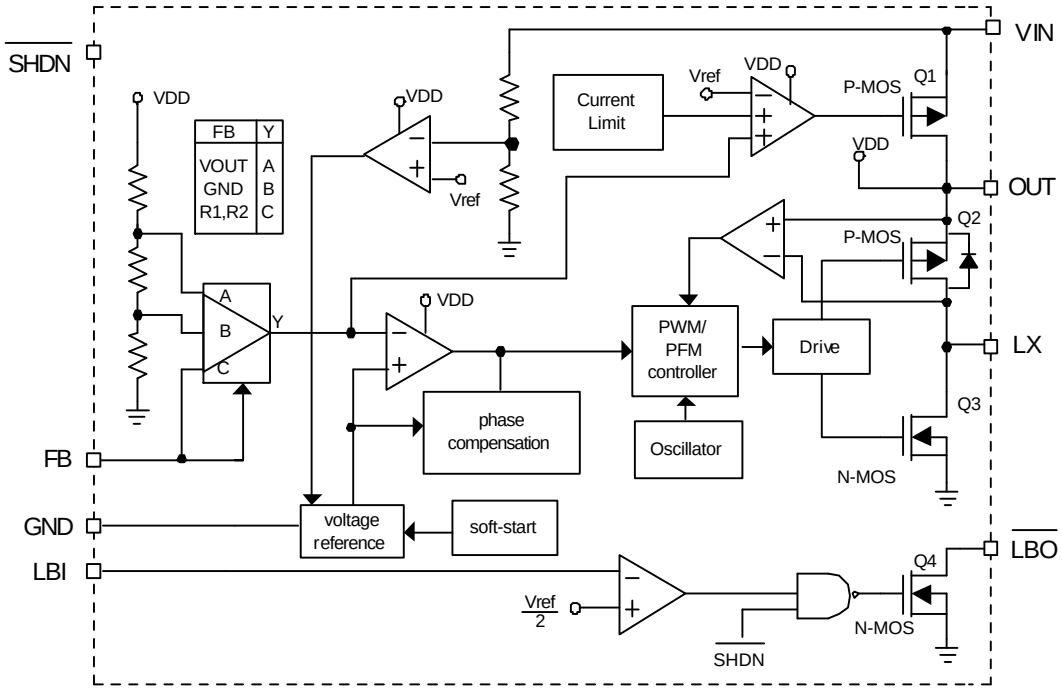
= Thermal Pad
(connected to GND plane for better heat dissipation)

Ordering and Marking Information

APW7075 □□-□□□ Lead Free Code Handling Code Temp. Range Package Code	Package Code KA : SOP-8-P O : TSSOP-8 Temp. Range C : 0 to 70 °C Handling Code TU : Tube TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
APW7075 KA : APW7075 XXXXX	XXXXX - Date Code
APW7075 O : APW7075 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{OUT}	Supply voltage(OUT to GND)	-0.3 to 6.0	V
V_{IO}	Input / output pins	-0.3 to 6.0	V
T_A	Operating Ambient Temperature Range	0 to 85	°C
T_J	Junction Temperature Range	0 to 150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature	300, 10 seconds	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance – Junction to Ambient SOP-8 SOP-8-P TSSOP-8	 124 80 160	°C/W

Electrical Characteristics

V_{BAT} = 2V, FB = OUT (V_{OUT} = 3.3V), R_L = ∞, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

Symbol	Parameter	Test Conditions	APW7075			Unit
			Min.	Typ.	Max.	
Step-up section						
V_{BAT}	Minimum Operating Input Voltage (Note1)		0.6			V
	Operating Voltage		0.6		4.5	V
	Start-up Voltage	R_L = 3KΩ		0.9	1	V
F_{SW}	Operating Frequency	V_{OUT} = 3.3VX96%		300		kHz
D_{MAX}	Maximum PWM Duty Cycle	V_{OUT} = 3.3VX96%		90		%
Power MOSFET						
$R_{DS(on)}$-N	Active Switch ON Resistance	I_{LX} = 100mA		0.3	0.6	Ω
$R_{DS(ON)}$-P	Synchronous Switch on Resistance	I_{LX} = 100mA		0.6	0.9	Ω
Control						
V_{OUT}	Output Voltage	FB = OUT, I_{LOAD} = 0mA	3.234	3.3	3.366	V
		FB = GND, I_{LOAD} = 0mA	2.45	2.5	2.55	V
	Output Voltage Range	External divider	2.5		5.5	V
$V_{OUT(drop)}$	V_{OUT} Dropping Voltage (Note 2)	V_{OUT} = 3.3V, C_{OUT} = 100µF			150	mV

Electrical Characteristics (Cont.)

Unless otherwise noted these specifications apply over full temperature, 3.9V≤VIN<5.5V, C_{OUT}≥10µF, SHDN=V_{IN} ,Typical values are at T_A=+25°C.)

Symbol	Parameter	Test Conditions	APW7075			Unit
			Min.	Typ.	Max.	
T_{SS}	Soft-start Time	V_{OUT} = 3.3V		30	100	ms
V_{REF}	FB Input Threshold	I_{LOAD} = 0mA	1.176	1.2	1.224	V
I_{FB}	FB Input Current	V_{FB} = 1.4V		0.03	50	nA
I_{DD}	Operating Current (Note3)	V_{OUT} = 3.3VX96%, I_{LOAD} = 0mA		70	140	µA
	Shutdown Current	$V_{\overline{SHDN}}$ = 0		0.1	5	µA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = 0 or V_{OUT}		0.07	50	nA
$\overline{SHDN}$	Logic LOW (V_{IL})			0.8	0.3	V
	Logic HIGH(V_{IH})		1.4	0.8		V
	LBI Input Hysteresis			10		mV
V_{LBI}	LBI Threshold		0.588	0.6	0.612	V
I_{LBI}	LBI Input Current	V_{LBI} = 0.8V		1	50	nA
$V_{\overline{LBO}}$	$\overline{LBO}$ Logic Low	V_{LBI} = 0, I_{SINk} = 1mA		0.2	0.4	V
$I_{\overline{LBO}}$	$\overline{LBO}$ Off Leakage Current	$V_{\overline{LBO}}$ = 5.5V, V_{LBI} = 5.5V		0.07	1	µA
LDO Section (Note4)						
$V_{IN(upper)}$	Upper V_{IN} Threshold Voltage	V_{IN} increasing	3.75	3.9	4.05	V
$V_{IN(lower)}$	Lower V_{IN} Threshold Voltage	V_{IN} decreasing	3.65	3.8	3.95	V
V_{TH}	VIN Threshold Hysteresis			100		mV
V_{OUT}	Output Voltage		V_{OUT}-2	V_{OUT}	V_{OUT}+2	V
I_{LIM}	Current Limit	V_{IN} = 5V		1		A
I_{SHORT}	Short Current	V_{OUT} = 0V		110		mA
I_{OUT}	Load Current		500			mA
V_{DROP}	Dropout Voltage	I_{LOAD} = 500mA		0.6	0.9	V
Iq	Quiescent Current	No load		800	1000	uA
		I_{LOAD} = 500mA		1.1	1.5	mA
REG_{LINE}	Line Regulation	4V<V_{IN}<5.5V, I_{LOAD} = 0mA		4	10	mV
REG_{LOAD}	Load Regulation	V_{IN} = 5V, 0mA<I_{LOAD}<500mA		20	30	mV

Note1: The min. operating voltage is dependent on the duty cycle.

Note2: The dropped output voltage is that the input power (VIN pin) is switched to battery power (LX pin), when the VIN power is removed.

Note3: Device is boostrapped (power to the IC comes from OUT). This correlates directly with the actual battery supply.

Note4: If the LDO mode is used, the output voltage should be under 3.8V.

Pin Function Description

VIN (Pin 1)

Input supply voltage for dual-mode application. Connect a schokkty diode (current rating >500mA) to USB port or 5V adapter. If the LDO mode is not used, tie the VIN pin to ground.

FB (pin 2)

Internal 1.2V reference voltage. Connect to OUT for 3.3V output,. Connect to GND for 2.5V output. Use a resistor divider to set the output voltage from 2.5V to 5.5V.

$\overline{SHDN}$ (pin 3)

Shutdown input. High = operating mode; Low = shutdown mode.

LBI (Pin 4)

Low-battery comparator input. Internally set to trip at 0.6V.

$\overline{LBO}$ (pin 5)

Open-drain low battery comparator output. Connect $\overline{LBO}$ to OUT through a 100KΩ resistor. Output is low as V_{LBI} < 0.6V. Open-drain device is turned on during shutdown.

OUT (pin 8)

Power output. OUT provides bootstrap power to the IC.

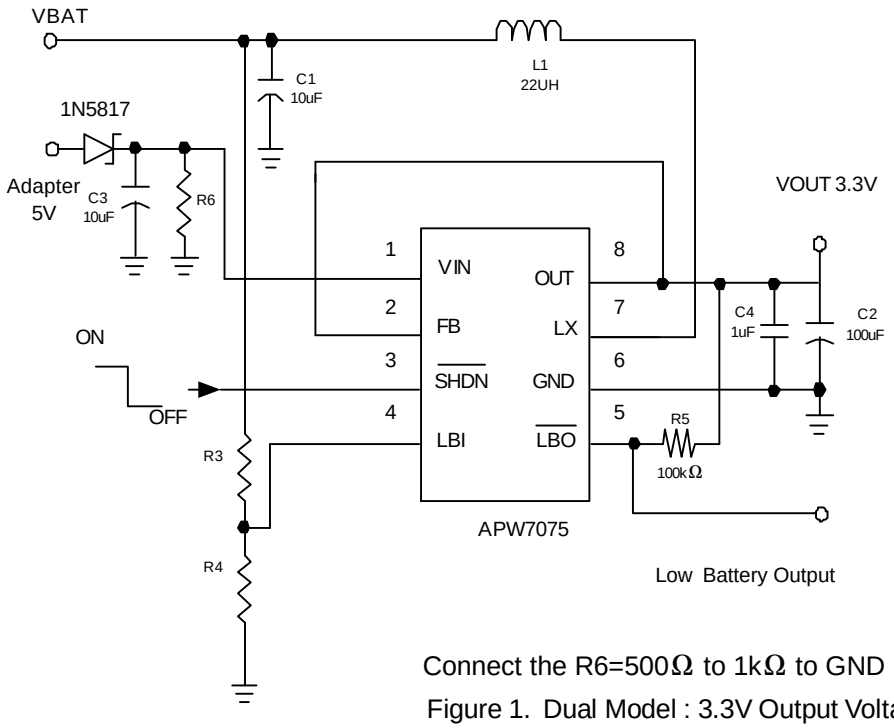
GND (Pin 6)

Ground pins of the circuitry and all ground pins must be soldered to PCB with proper power dissipation.

LX (pin 7)

N-channel and P-channel power MOSFET drain connection.

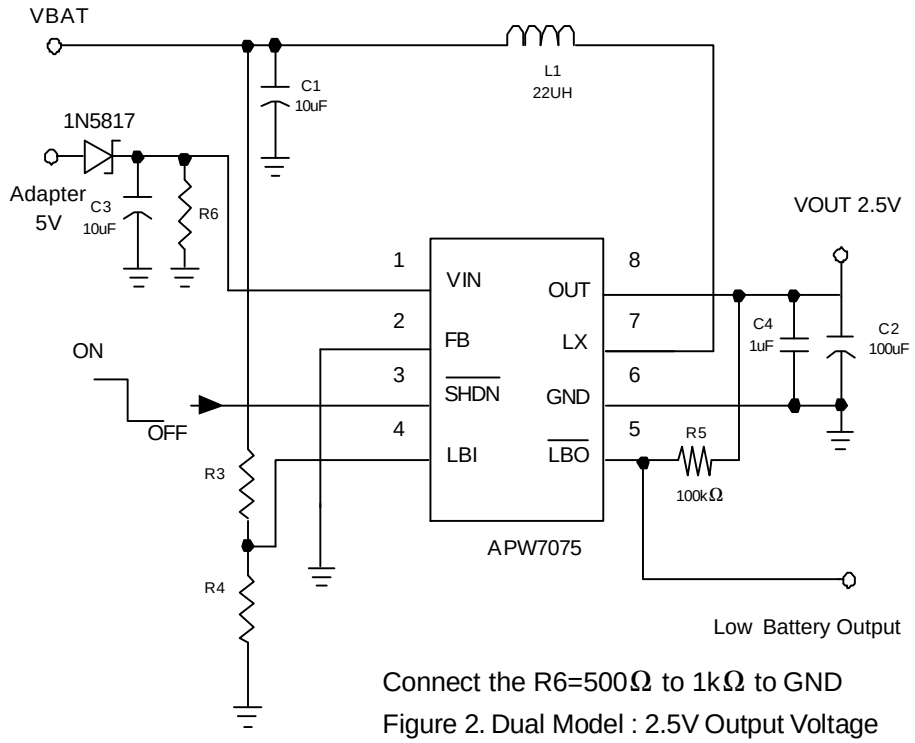
Application Schematic



Connect the R6=500Ω to 1kΩ to GND

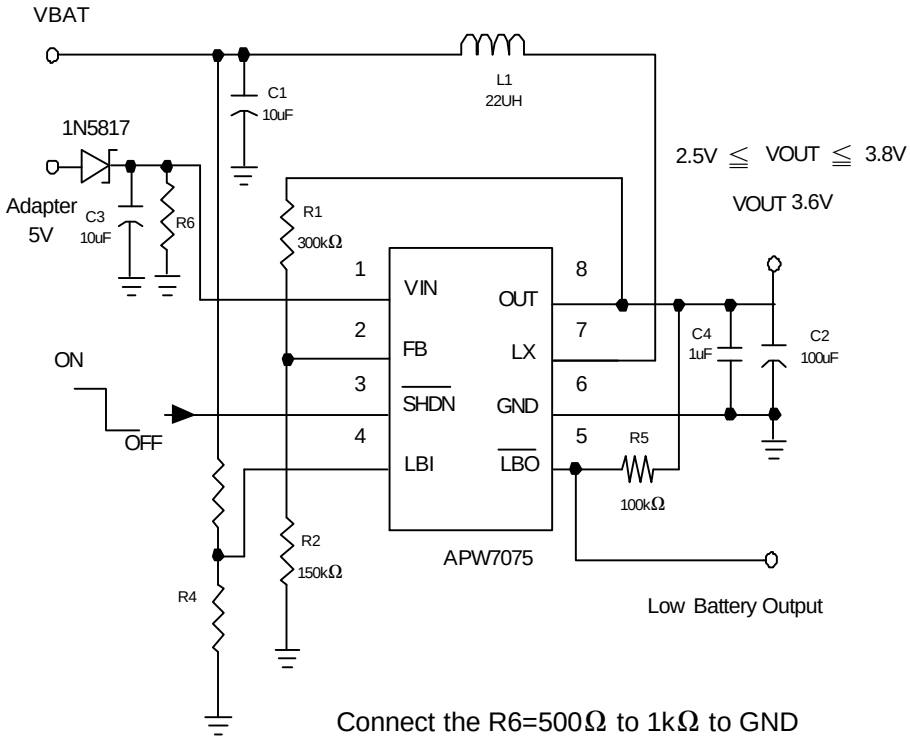
Figure 1. Dual Model : 3.3V Output Voltage

Application Schematic (Cont.)



Connect the R6=500Ω to 1kΩ to GND

Figure 2. Dual Model : 2.5V Output Voltage



Connect the R6=500Ω to 1kΩ to GND

Figure 3. Dual Model: Adjustable Output Voltage

Application Schematic (Cont.)

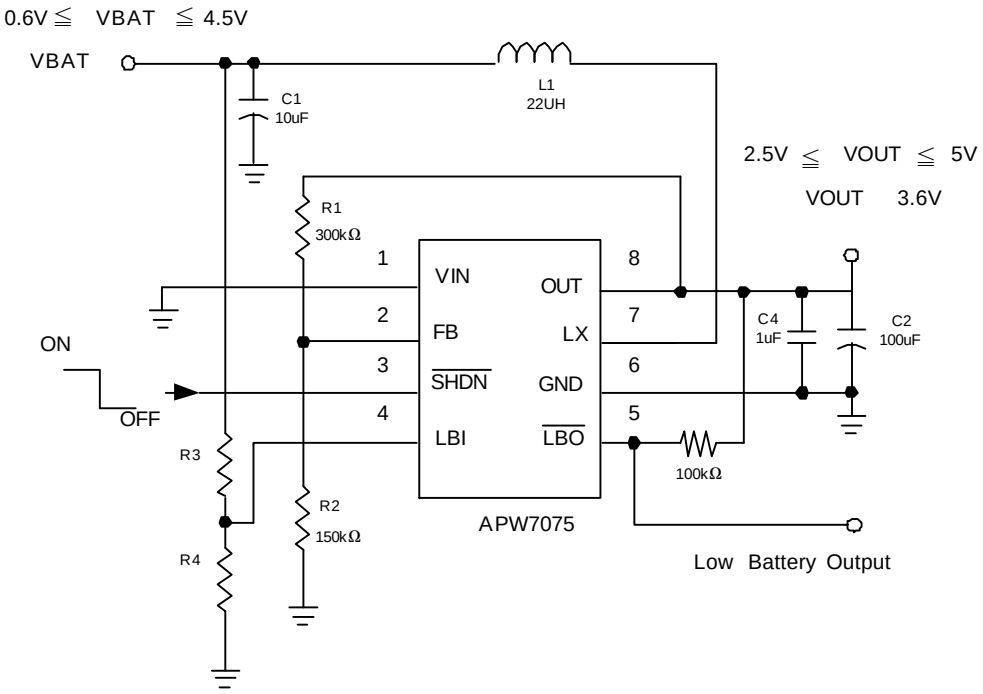
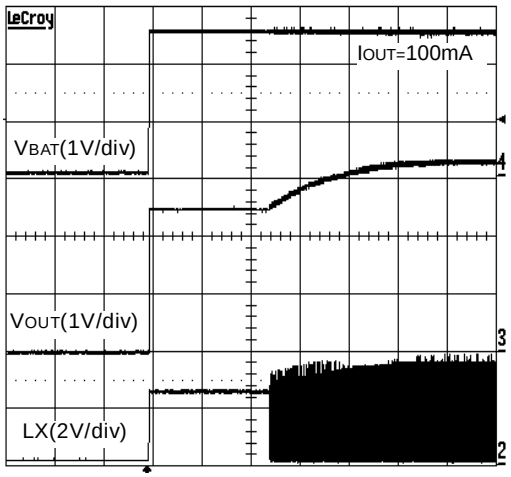


Figure 4. Single Boost Converter

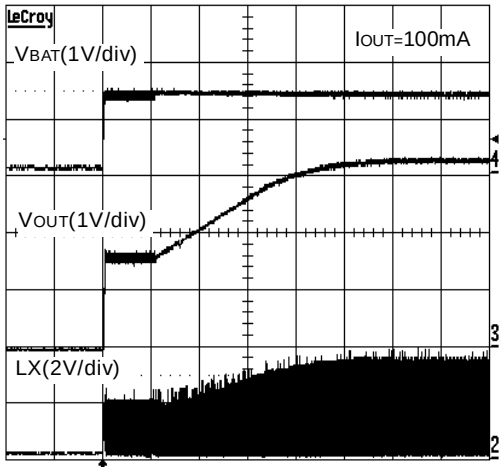
Typical Characteristics

Power Up ($V_{BATTERY}$=2.4V)



Time(10ms/div)

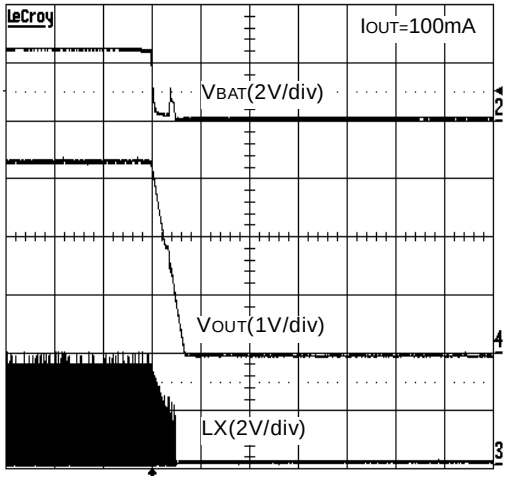
Power Up ($V_{BATTERY}$=1.2V)



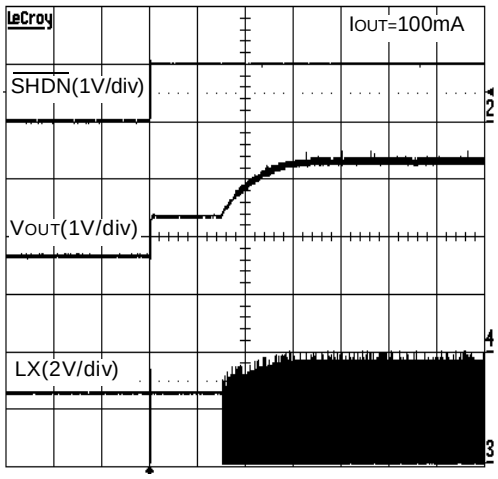
Time(10ms/div)

Typical Characteristics (Cont.)

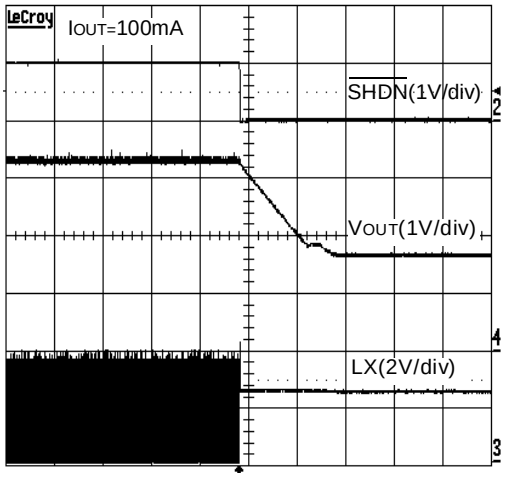
Power Down



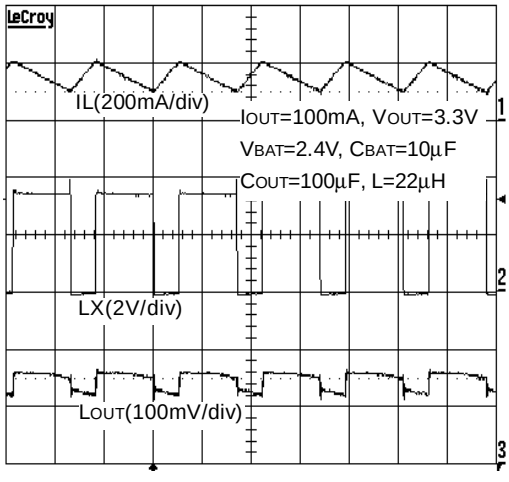
Enable



Shutdown

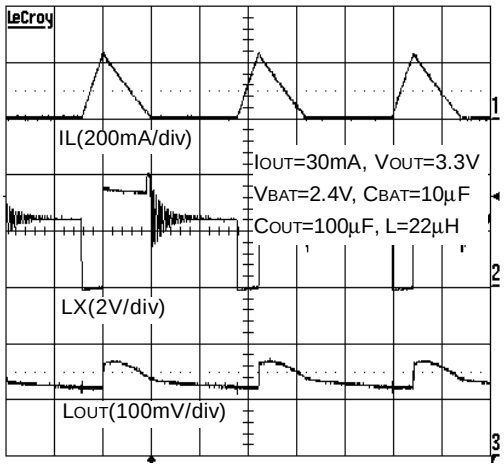


Heavy Load Operating Waveforms

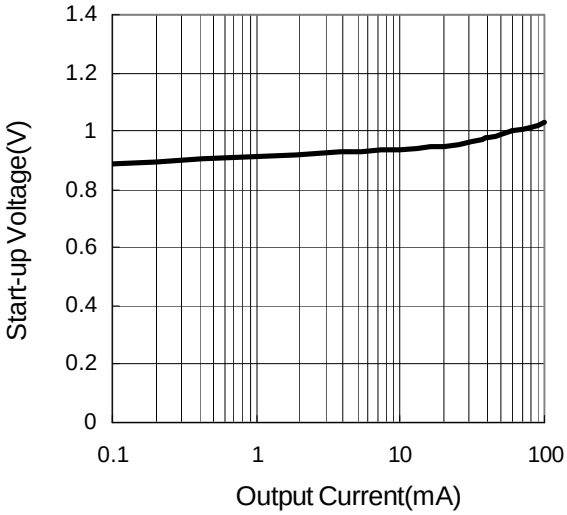


Typical Characteristics (Cont.)

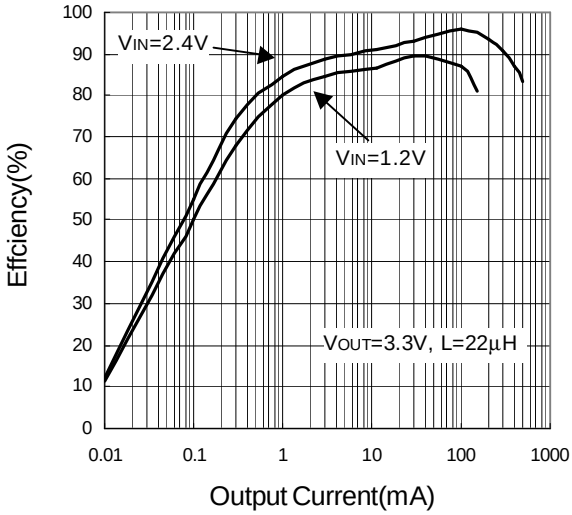
Light Load Operating Waveforms



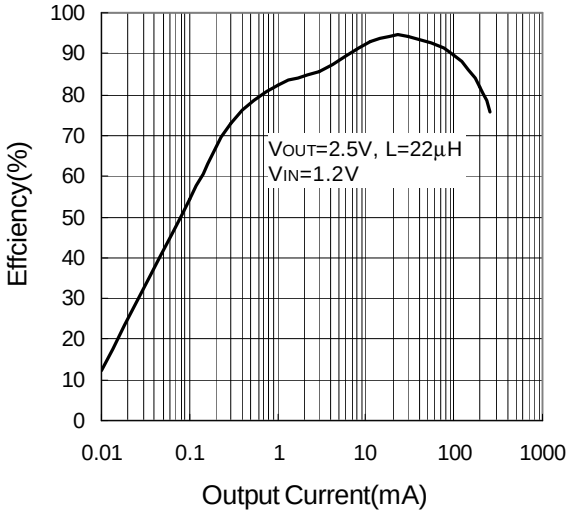
Output Current vs. Start-up Voltage



Effciency vs. Output Current

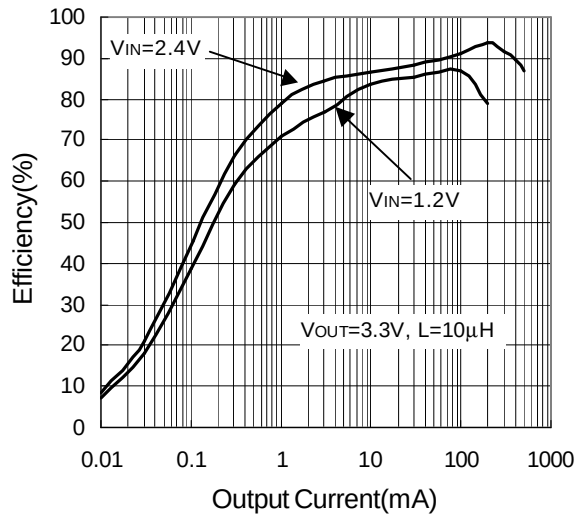


Effciency vs. Output Current

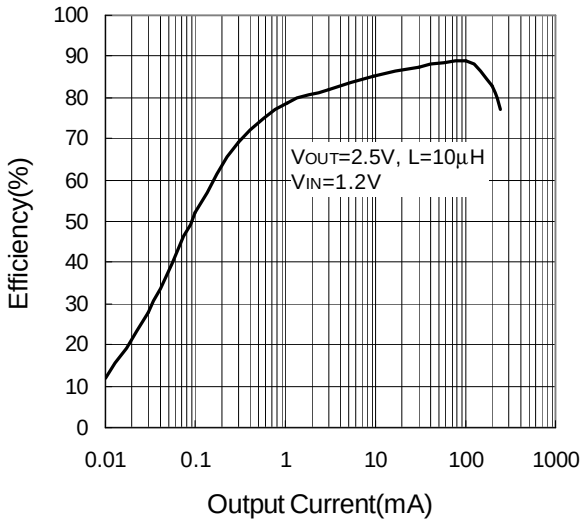


Typical Characteristics (Cont.)

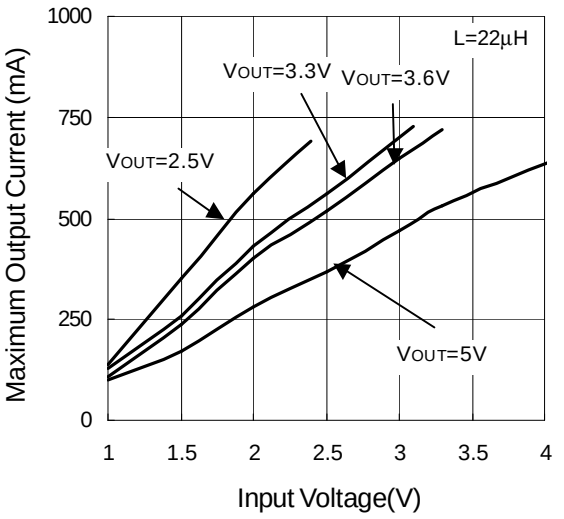
Efficiency vs. Output Current



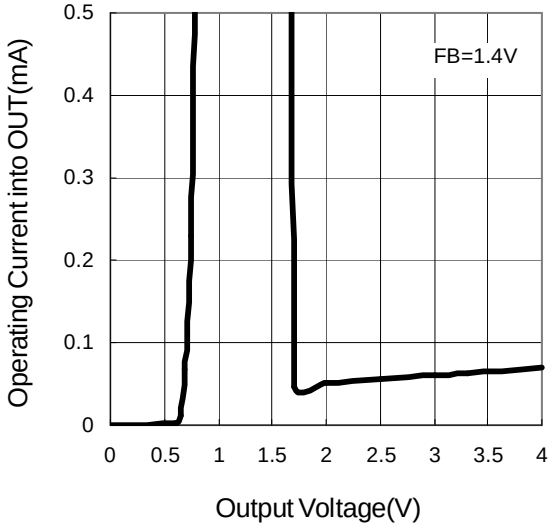
Efficiency vs. Output Current



Maximum Output Current vs.Input Voltage

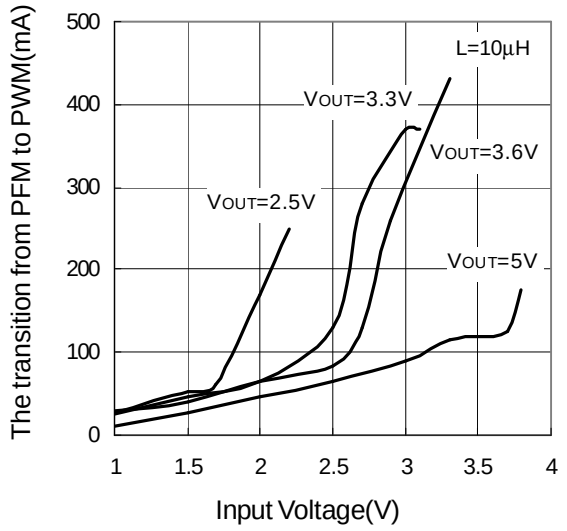


Operating Curretnt into OUT vs. Output Voltage

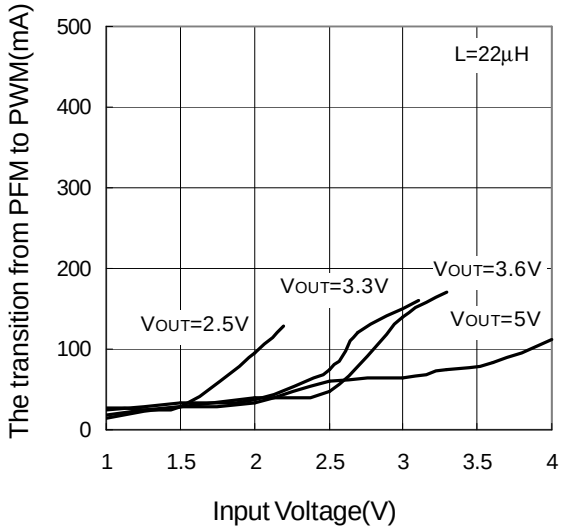


Typical Characteristics (Cont.)

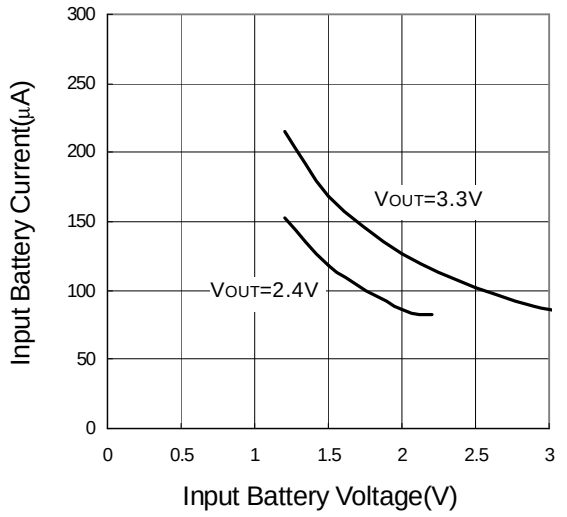
Transition from PFM to PWM vs. Input Voltage



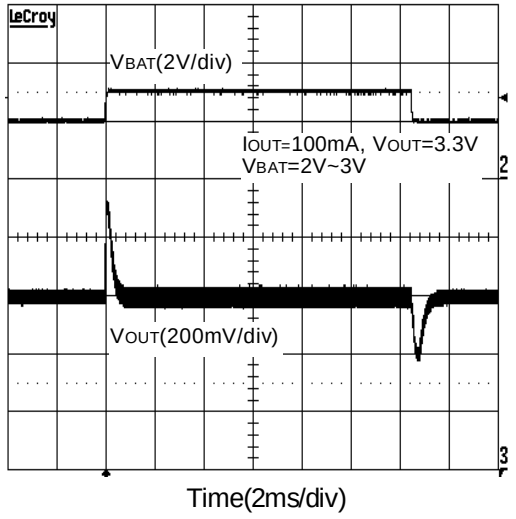
Transition from PFM to PWM vs. Input Voltage



Input Battery Current vs. Input Battery Voltage

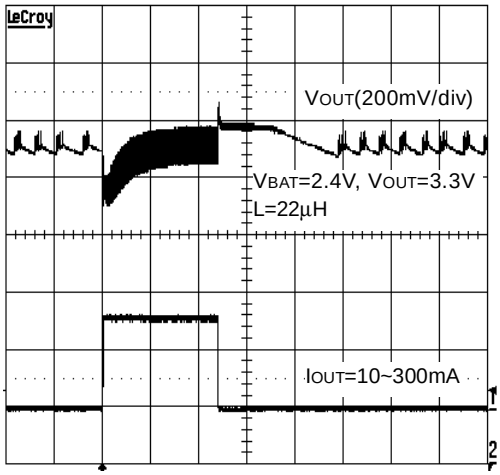


Line Transient Response

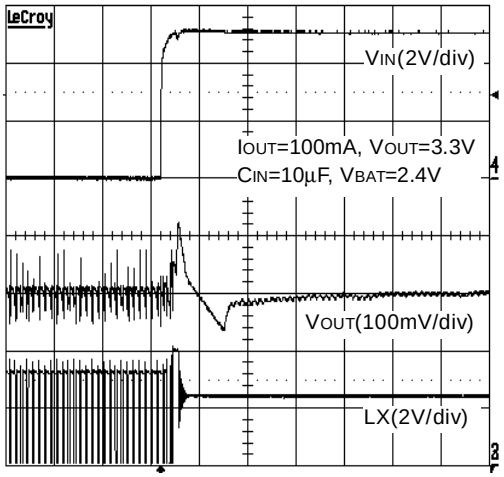


Typical Characteristics (Cont.)

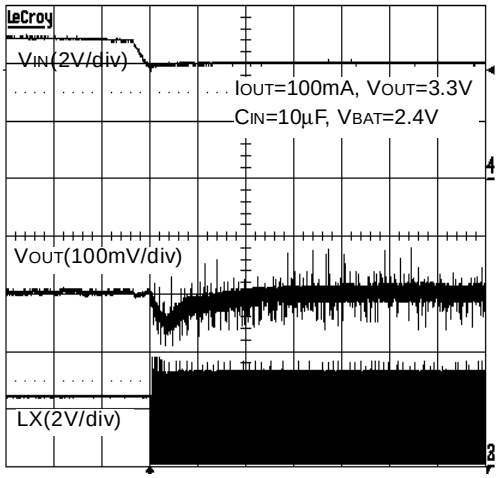
Load Transient Response



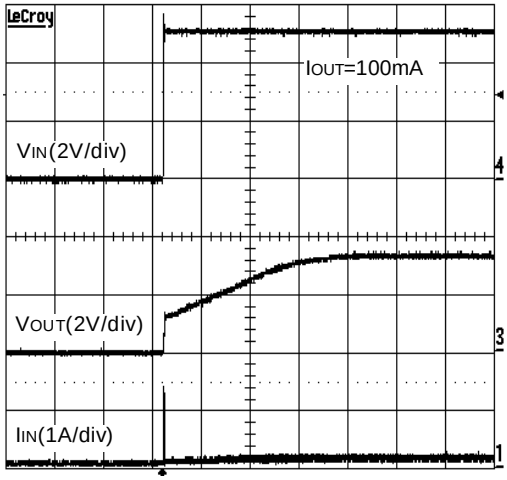
PWM to LDO



LDO to PWM

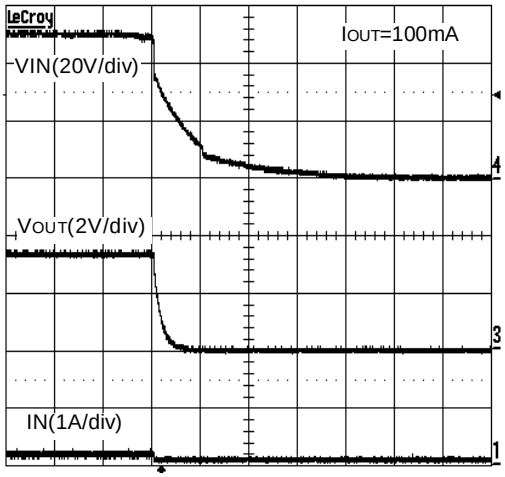


LDO Power Up

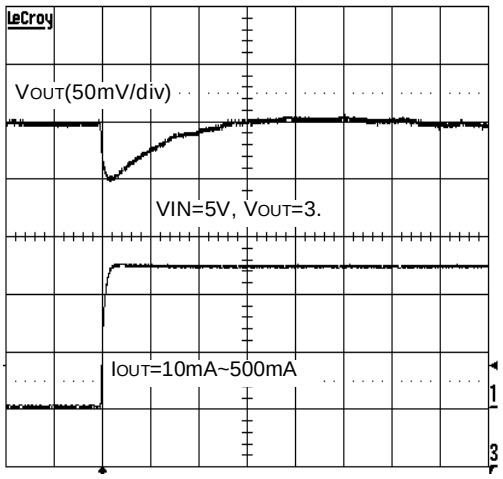


Typical Characteristics (Cont.)

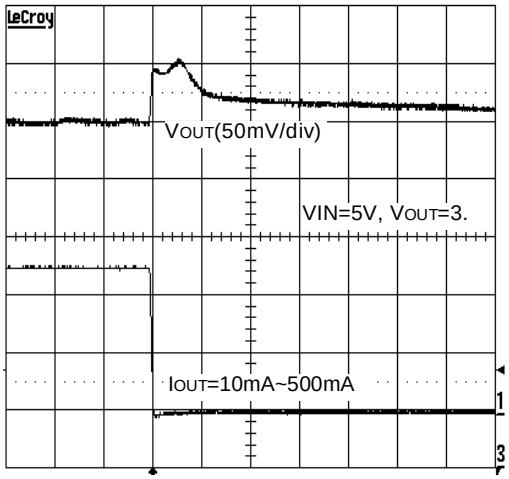
LDO Power Down



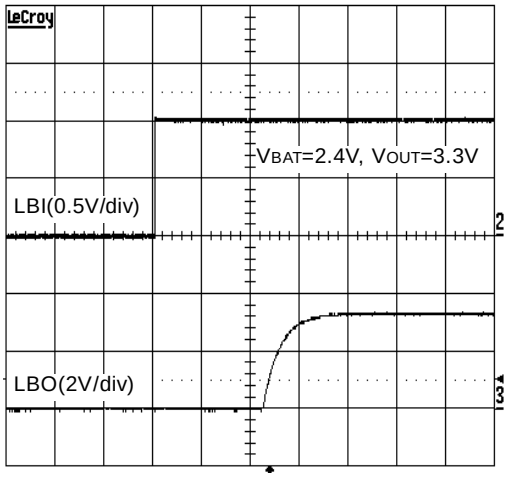
LDO Load Transient Response



LDO Load Transient Response

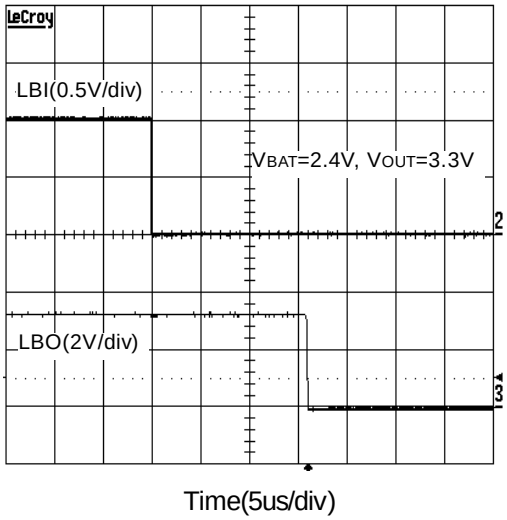


LBO Rising Delay Time

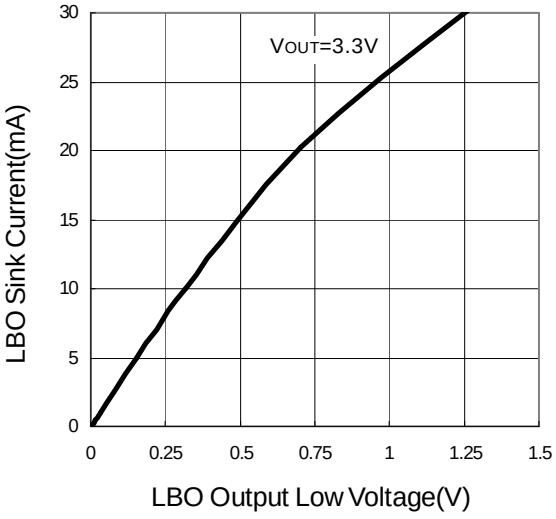


Typical Characteristics (Cont.)

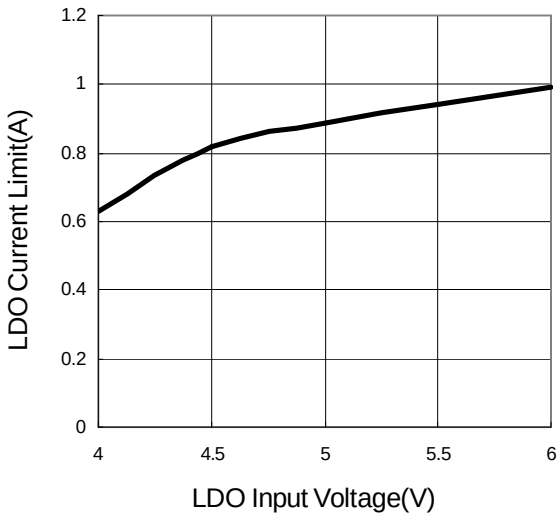
LBO Falling Delay Time



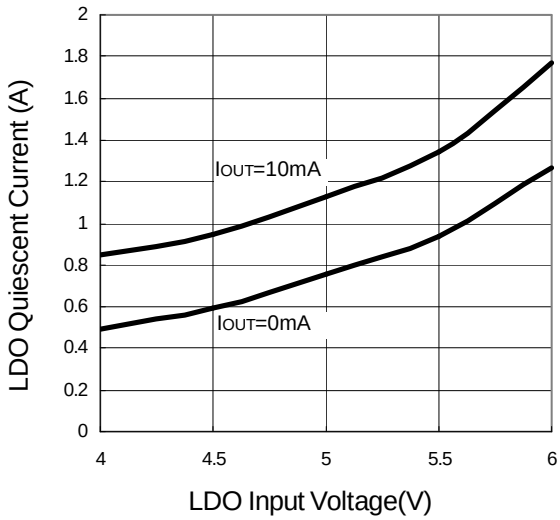
LBO Output Sink Current vs. LBO Low Voltage



LDO Current Limit vs. LDO Input Voltage

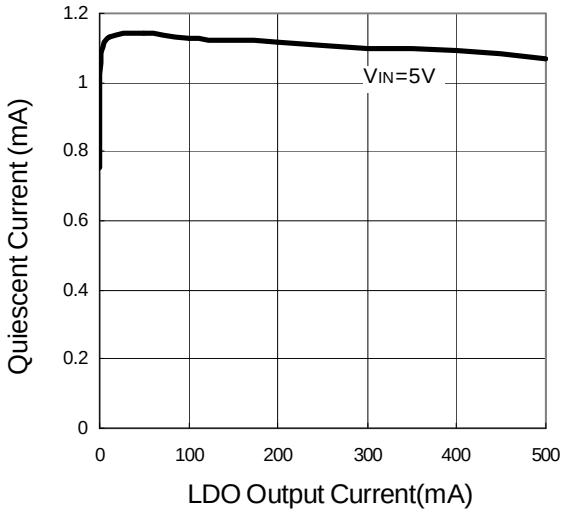


LDO Quiescent Current vs. LDO Input Voltage

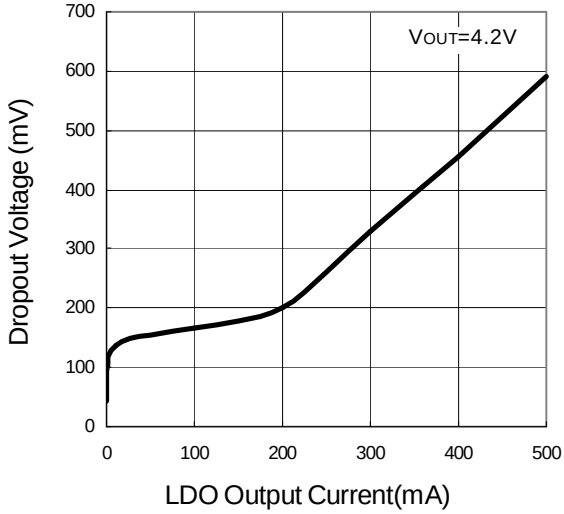


Typical Characteristics (Cont.)

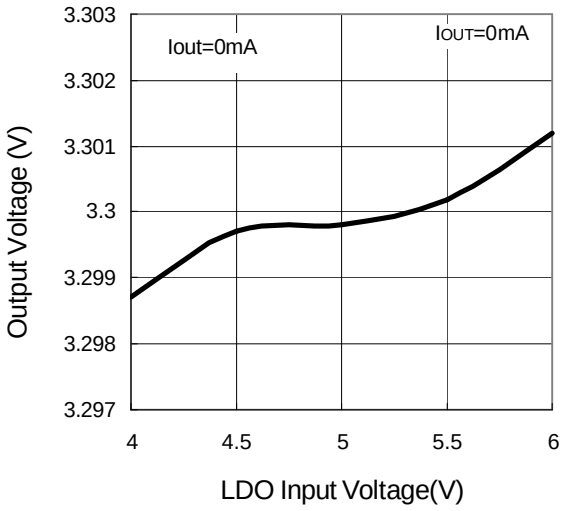
Quiescent Current vs. LDO Output Current



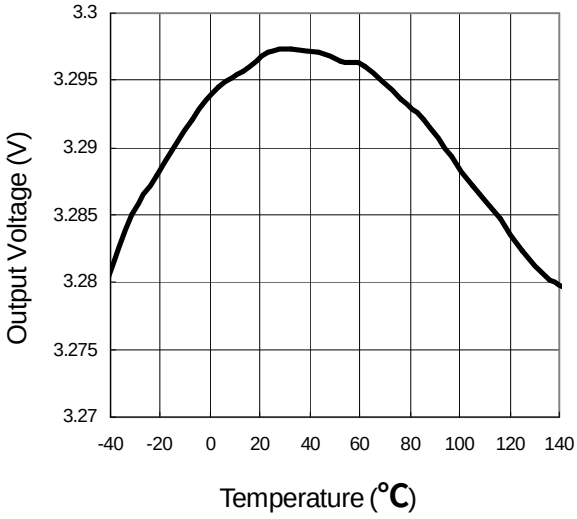
Dropout Voltage vs. LDO Output Current



Output Voltage vs. LDO Input Voltage



Output Voltage vs. Temperature



Function Description

PFM Control Scheme

The APW7075 features the PFM control scheme to improve the efficiency during light load. In PFM mode, the inductor stores the energy during internal N-channel MOSFET turns on, and the energy is transferred to output capacitors and load during internal P-channel MOSFET turns on. If the energy which is charged to output capacitors exceeds the requirement of load, the current will reverse from output capacitors to inductor and input capacitors. The PFM comparator compares the source (OUT) and drain (LX) of the internal P-channel MOSFET. When the current that flows through the internal P-channel MOSFET is backward (from OUT to LX), the internal P-channel MOSFET will be turned off, and the output capacitor supplies the load and maintains the output voltage. During PFM mode, the IC switches only as need to serve the load, reducing the switching frequency and associated losses in the internal switches and the external inductor. Some jitter is normal during transition from PFM to PWM mode; the transition of the PFM to PWM is dependent on the inductance values, VIN, and VOUT. The output ripple is higher during PFM operation, a larger output capacitor can be used to minimize the output ripple.

Synchronous Rectification

The APW7075 has an internal N-channel and a P-channel MOSFET, it is no need for external components, the internal low $R_{DS(ON)}$ P-channel MOSFET replaces the discrete Schottky diode, and it is reducing cost and board space. During the cycle off time, the P-channel MOSFET turns on, and the power dissipation on the P-channel MOSFET is lower than discrete Schottky diode, thus the conversion efficiency can be improved.

Shutdown

The APW7075 has an active high enable function. Force $\overline{SHDN}$ high (>1.4V) to enable the step-up converter, $\overline{SHDN}$ low (<0.3V) to disable the step-up converter and the device enters shutdown mode. In shutdown mode, the converter stops switching and all internal control circuits are turned off, but the output is still applied by input voltage through the body diode of P-channel MOSFET, it is about Vin-0.6V. Note that when the output is applied from the VIN (LDO mode), the shutdown function is disabled.

Soft Start

The APW7075 provides the soft-start function to get the controlled output voltage rise. When battery voltage (<1.8V) is supplied to the device and exceeds the start-up voltage, the internal N-channel and P-channel MOSFETs start to switch and pump up the output voltage to 1.8V(if the battery voltage is over 1.8V, the output voltage will equal battery voltage during this time), which control circuitry can operate normally . The soft start controls the rise of internal reference voltage, when the internal reference voltage exceeds the feedback voltage which is divided by the resistor from output voltage, the soft-start circuit will control the output voltage until the output voltage is in regulation. The soft-start interval is approximately 30ms.

Function Description (Cont.)

LDO

The output voltage has two operation modes. When VIN exceeds 3.9V, the output will become the LDO regulator and the step-up converter will be disabled. The LDO output is a P-channel low dropout regulator with 1A current limit. When the VIN is below 3.8V, the output will return to the step-up converter, and the LDO mode will be disabled. Note that when LDO mode is used, the output voltage should be under 3.8V

Low Battery Detection

The low battery detection is used to monitor the battery voltage and to generate a signal. This function includes two pins, LBI is the inverting input of the comparator and $\overline{LBO}$ is an open drain output (see block diagram). When the LBI voltage drops below the threshold voltage 0.6V, the open drain device will turn on and $\overline{LBO}$ becomes low. The Low battery threshold voltage can be programmed with a resistive divider from battery to LBI pin to ground. Since the $\overline{LBO}$ is an open drain output, it usually requires an external pull-up resistor.

Application Information

Output Voltage Selection

The output voltage of APW7075 can be adjusted by an external resistor divider, or connect FB pin to OUT for 3.3V and to ground for 2.5V (see Application Schematic). The internal reference voltage is 1.2V and the allowed output voltage is from 2.5V to 5.5V. The following equation can be used to calculate the output voltage:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 1.2V$$

Programming Low Battery Threshold Voltage

The low battery threshold voltage can be programmed with a resistive divider from battery to LBI pin to ground (see Application Schematic). The internal reference voltage is 0.6V, and the low battery threshold voltage must be below the battery voltage. The following equation can be used to calculate the low battery threshold voltage:

$$V_{BAT-TH} = \left(1 + \frac{R3}{R4}\right) \times 0.6V$$

Inductor Selection

The APW7075 works well with a 22uH inductor in most applications. The inductance values determine the inductor ripple current and affect the output current. Higher inductance values reduce ripple and improve efficiency. Lower inductance values have fast response but increase the ripple and reduce the efficiency. The maximum allowed LX current is 1A (the maximun. output current shows in Typical Characteristics) and so the peak inductor current cannot exceed it. The following equations calculate the inductor current, and output current.

$$I_{OUT} = IL \times (1-D)$$

$$\Delta IL = (V_{OUT} - V_{IN}) \times \frac{(1-D)}{L \times f}$$

Where:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Function Description (Cont.)

Inductor Selection (Cont.)

The inductor's DC resistance affects the efficiency; larger resistance dissipates more power, it should be as small as possible. It is important to choose the inductor's saturation current rating greater than the peak current which the inductor will flow in the application.

Boost Converter Input Capacitor Selection

At least a 10uF input capacitor is recommended to stabilize the battery voltage and minimize the peak current ripple from the battery.

LDO Input Capacitor Selection

The LDO input capacitor with larger values and lower ESRs provide better PSRR and line transient response. At least a 10uF capacitor is recommended.

Output Capacitor Selection

The output capacitor is used for supplying the output during internal N-channel MOSFET turns on time. Larger capacitance and lower ESR reduce the output voltage ripple. The output voltage supplies the power to the IC and so the output voltage ripple must be as small as possible to provide better PSRR. In general, a 100uF to 220uF low ESR Tantalum capacitor is recommended, a 1uF ceramic capacitor in parallel for bypassing the noise is also recommended. The following equation calculates the output ripple.

$$Voripple = I_{OUT} \times \left(\frac{V_{OUT} - V_{BAT}}{C_{OUT} \times F_{SW} \times V_{OUT}} + ESR \right)$$

Layout Considerations

The correct PCB layout is important for all switching converters. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Figure. 5 illustrates the layout guidelines, the bold lines indicate the high current paths; these traces must be short and wide. The input capacitors, output capacitors, and the inductor should be as close to the IC as possible. Use a common ground plane for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground planes at a node close to the GND pin of IC. The feedback and LBI resistor dividers should be placed as close to the IC as possible.

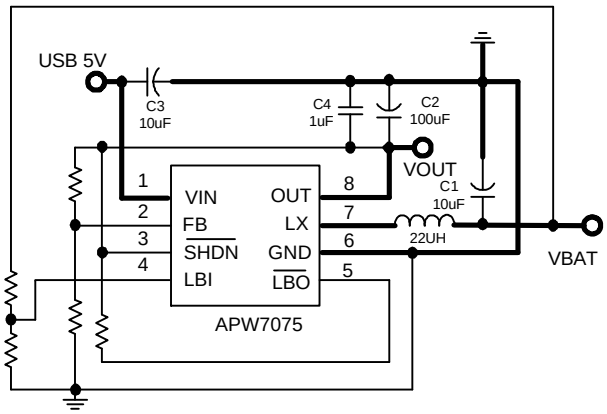
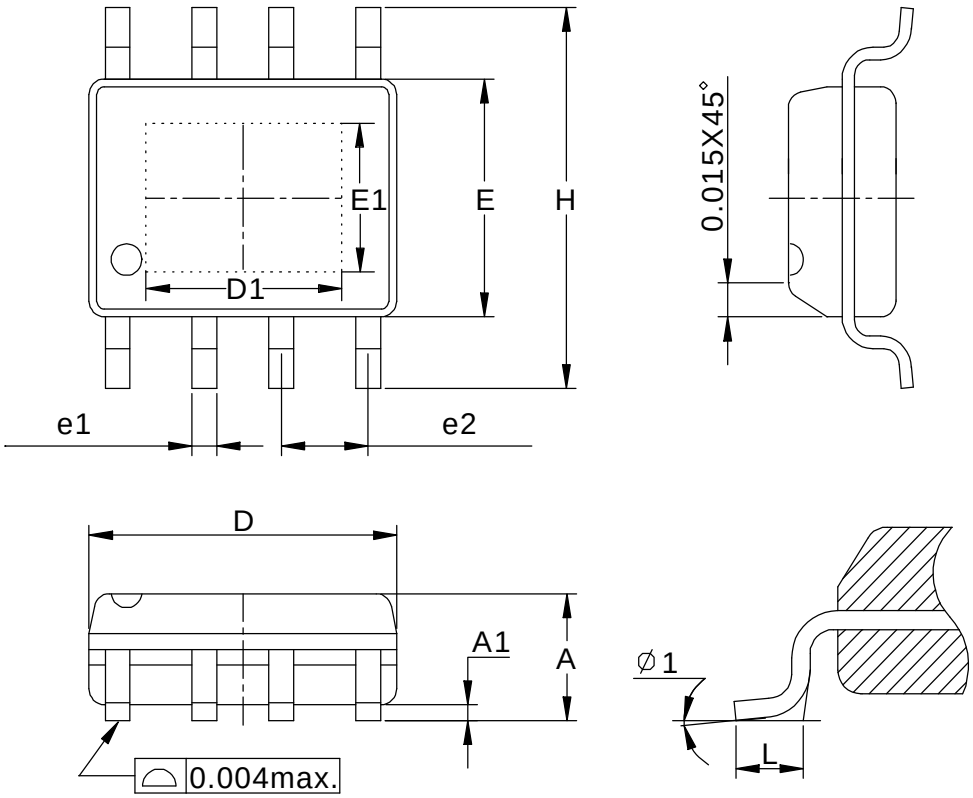


Figure 5. Recommended Layout Diagram

Packaging Information

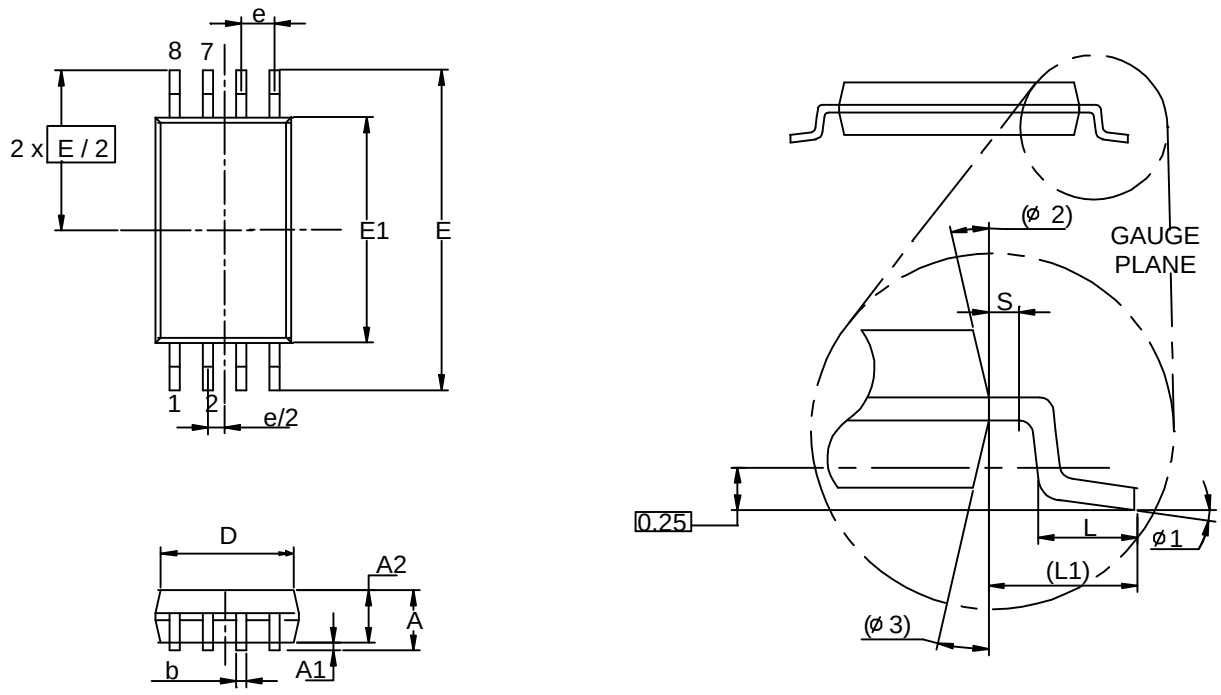
SOP-8-P pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0	0.15	0	0.006
D	4.80	5.00	0.189	0.197
D1	3.00REF		0.118REF	
E	3.80	4.00	0.150	0.157
E1	2.60REF		0.102REF	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Packaging Information

TSSOP-8

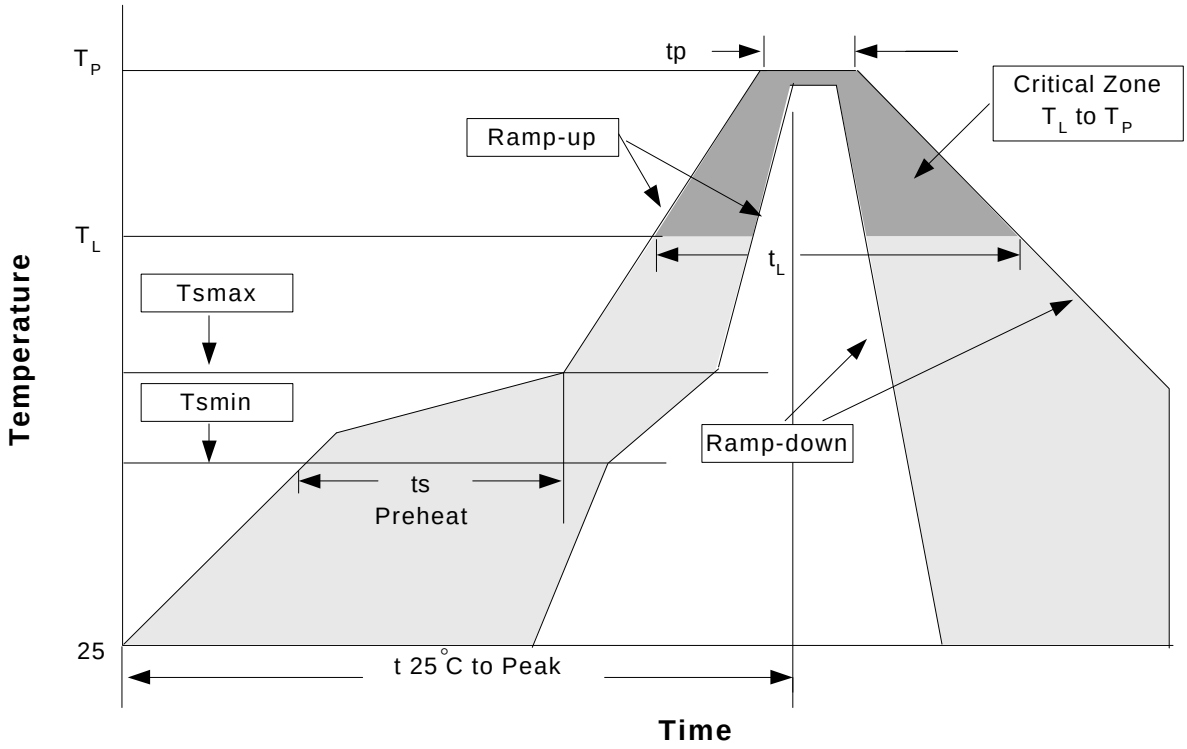


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		1.2		0.047
A1	0.00	0.15	0.000	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
D	2.9	3.1	0.114	0.122
e	0.65 BSC		0.026 BSC	
E	6.40 BSC		0.252 BSC	
E1	4.30	4.50	0.169	0.177
L	0.45	0.75	0.018	0.030
L1	1.0 REF		0.039REF	
R	0.09		0.004	
R1	0.09		0.004	
S	0.2		0.008	
ϕ1	0°	8°	0°	8°
ϕ2	12° REF		12° REF	
ϕ3	12° REF		12° REF	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

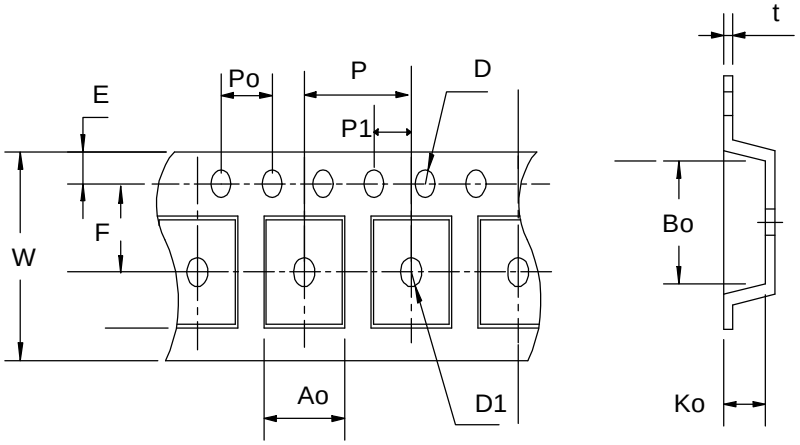
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

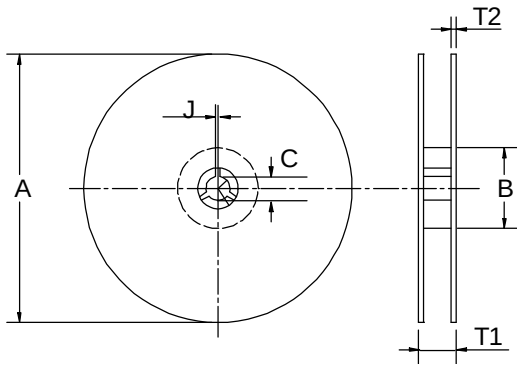
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP- 8-P	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013
Application	A	B	C	J	T1	T2	W	P	E
TSSOP-8	330 ± 1	62 +1.5	12.75+ 0.15	2 + 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0. 1	1.5 + 0.1	1.5 + 0.1	4.0 ± 0.1	2.0 ± 0.1	7.0 ± 0.1	3.6 ± 0.3	1.6 ± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP-8-P	12	9.3	2500
TSSOP-8	12	9.3	2500

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