Semiconductor Corporation

CS6159

Low Power PCM Line Interface

Features

- Provides CMOS Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Internal generation of transmitted pulse width and pulse shape.
- Low power - typically 180 mW
- Small package - 300 mil DIP & SOIC
- Minimum External Components

General Description

The CS6159 combines the analog transmit and receive line interface functions for a T1 or PCM-30 interface in a 24-pin skinny-DIP or SOIC device. The line interface operates from a single 5 Volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for line lengths ranging from 0 to 655 feet from a DSX-1 cross connect.

Applications

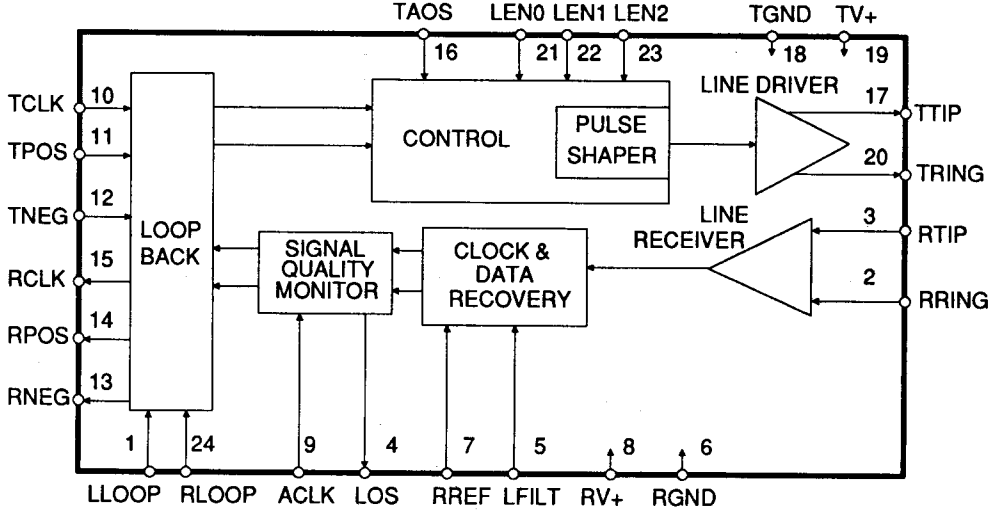
- Central Office Exchanges
- Digital Access and Cross Connect Systems
- Customer Premises Equipment
- PABX's

Ordering Information

CS6159-IP1	24 Pin Plastic DIP (300 mils)	T1 & PCM-30
CS6159-IS1	24 Pin Plastic SOIC	T1 & PCM-30

3

Block Diagram



Preliminary Product Information | This document contains information on a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+, TV+	-	6.0	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	(RV+)+ 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Consumption (Note 4) 100% ones density & max. line length @ 5.25V	P_C	-	-	335	mW
Normal Power Consumption (Note 4) 50% ones density & 300 ft. line length @ 5.0V	P_C	-	180	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation at 1.544 Mbps while driving 54 Ω load over operating temperature range. Includes CS6159 and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load. Power dissipation at 2.048 Mbps will be 30% higher.

DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+, RV+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage Pins 1, 9-12, 16, 21-24	V_{IH}	2.0	-	-	V
Low-Level Input Voltage Pins 1, 9-12, 16, 21-24	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 5) I_{OUT}= - 40 uA Pins 4, 13-15	V_{OH}	4.0	-	-	V
Low-Level Output Voltage I_{OUT}= +1.6 mA Pins 4, 13-15	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA

Notes: 5. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40 µA).

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C; TV+,RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
TRANSMITTER					
AMI Output Pulse Amplitudes					
Line Length Selections LEN2/1/0 = 0/0/0 & 0/1/0 (Measured at xfmr output)		2.7	3.0	3.3	V
All line length settings except, LEN2/1/0 = 0/0/0, 0/1/0 & 0/0/1 (Measured at the DSX; Normalization factor for Figure 4)		2.4	3.0	3.6	V
Load Presented To Transmitter Output		-	54	-	Ohms
Jitter Added by the Transmitter (Note 6)	10Hz - 8kHz	-	0.005	-	UI
	8kHz - 40kHz	-	0.008	-	UI
	10Hz - 40kHz	-	0.010	-	UI
	Broad Band	-	0.015	-	UI
Power in 2kHz band about 772kHz	(Note 7)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power at 772kHz)	(Note 7)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 7)	-	0.2	0.5	dB
RECEIVER					
Sensitivity Below DSX (0dB = 2.4V)		-10	-	-	dB
Loss of Signal Threshold		-	0.325	-	V
Data Decision Threshold	T1 pulse settings	-	65	-	% of
	CCITT LEN2/1/0 = 000	-	50	-	Peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance (Notes 8, 9)	10kHz - 100kHz	0.4	-	-	UI
	10Hz and below	300	-	-	
PLL 3 dB Bandwidth	(Note 9)	-	20	-	kHz
PLL Jitter Peaking	(Note 9)	-	1.4	-	dB

Notes: 6. Input signal to TCLK is jitter free.
7. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.
8. See Figure 7.
9. Contact the factory for the recommended external component values. Assumes 1-in-8 input data pattern.

T1 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+,RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{in}	-	1.544	-	MHz
ACLK Frequency	(Note 10)	f_{out}	-	1.544	-	MHz
RCLK Cycle Width		t_{pw1}	646	648	650	ns
		t_{pwh1}	-	324	-	ns
	(Notes 12, 13, 15)	t_{pwl1}	-	324	-	ns
RCLK Duty Cycle	(Notes 12, 13, 15)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Falling Setup Time	(Note 15)	t_{su1}	240	324	-	ns
RCLK Falling to RPOS/RNEG Hold Time	(Note 15)	t_{h1}	240	324	-	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns

PCM-30 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+,RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{in}	-	2.048	-	MHz
TCLK Duty Cycle for LEN2/1/0 = 0/0/0	(Note 11)	t_{pwh2}/t_{pw2}	44	50	56	%
ACLK Frequency	(Note 10)	f_{out}	-	2.048	-	MHz
RCLK Cycle Width		t_{pw1}	484	488	492	ns
		t_{pwh1}	-	244	-	ns
	(Notes 12, 13, 15)	t_{pwl1}	-	244	-	ns
RCLK Duty Cycle	(Notes 12, 13, 15)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Falling Setup Time	(Note 15)	t_{su1}	160	244	-	ns
RCLK Falling to RPOS/RNEG Hold Time	(Note 15)	t_{h1}	160	244	-	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns

Notes: 10. ACLK provided by an external source or TCLK.
11. The transmitted pulse width for LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK.
12. RCLK cycle width will vary with extent by which received pulses are displaced by jitter.
13. Max & Min RCLK duty cycles and cycle widths are for worst case jitter conditions.
14. At max load of 1.6 mA and 50 pF.
15. Not production tested. Guaranteed by design and/or characterization. Not applicable during loss of signal.

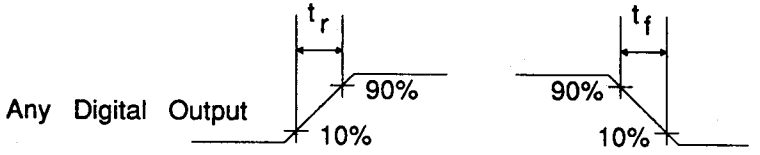


Figure 1. - Signal Rise and Fall Characteristics

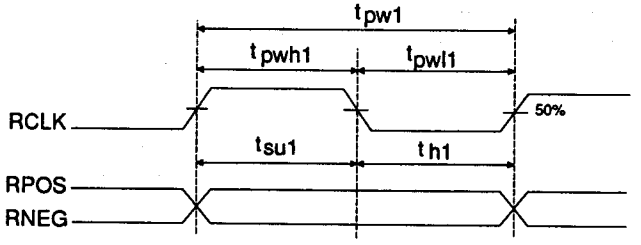


Figure 2. - Recovered Clock and Data Switching Characteristics

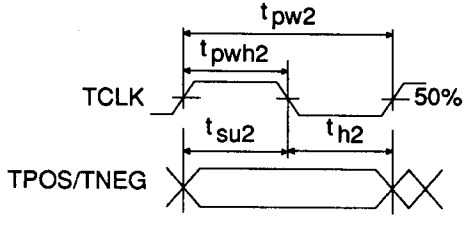


Figure 3. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (dual unipolar) data from a T1 or PCM-30 transceiver and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 or PCM-30 G.703 pulse shapes may be selected. For T1 applications, line lengths from 0 to 655 feet (as measured from the CS6159 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by digital "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 Volt supply, a 1.36:1, step-up transformer is required. The line driver is designed to drive a 54 Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit Line Length Selection

The transmitter has a 13-phase delay line which divides each TCLK cycle into 13 phases. For T1 applications, these phases are used to trigger different portions of the output waveform. For T1 DSX-1 applications, the line length selection offers a five partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS6159 modifies the output pulse to meet the requirements of ANSI T1.102, Bellcore TR-TSY-000499, AT&T Compatibility Bulletin 119 and the CCITT G.703 1.544 Mbps template. The exact pulse shape achieved at the DSX-1 can be affected by details of the board layout, transformer selection, and other factors. For cable types other than ABAM, it is recommended that the line length settings be evaluated. It is possible that an alternative interpretation of the LEN2/1/0 distance ranges is more appropriate. A typical output pulse is shown in Figure 4.

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	1	1	0-133 FEET	DSX-1 ABAM
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1		Reserved
0	0	0	PCM-30 G.703	2.048 MHz CCITT
0	1	0	FCC Part 68, Option A	CSU NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 1 - Line Length Selection

The T1 Network Interface pulse shapes meet FCC Part 68 for 0 dB line build out and ANSI T1.403 pulse shapes as shown in Table 1.

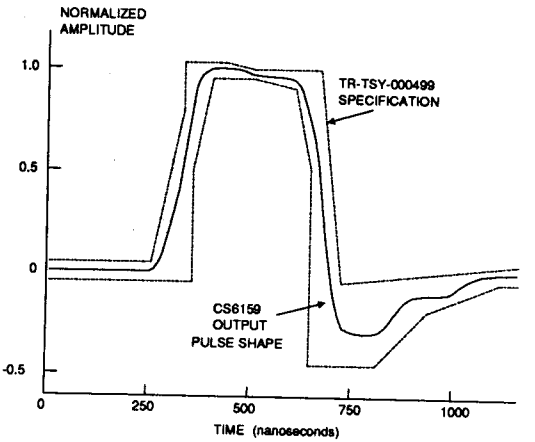


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

	For coaxial cable, 75 ohm load and transformer specified in Table A1.	For shielded twisted pair, 120 ohm load and transformer specified in Table A1.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05 *	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

* When configured with a 0.47 uF nonpolarized capacitor in series with the Tx transformer primary as shown in Figure A1.

Table 2 - CCITT G.703 Pulse Specifications

The PCM-30 G.703 pulse shape is also supported with line length selection LEN2/1/0 = 000. In this case only, the width of this pulse is determined by the high cycle of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 5, and specified in Table 2, assuming the transmitter is terminated correctly and the TCLK duty cycle and frequency are appropriate. The rising and falling edge of TCLK control the time at which the rising and falling edges of the output pulse occur. Transmitter termination information is provided in the applications section which appends this data sheet. Note that the pulse shape LEN2/1/0 = 010 generates the same amplitudes as the G.703 pulse (LEN2/1/0 = 000), but the pulse width is determined internally by the transmit delay line and will be approximately 263 ns when TCLK is 2.048 MHz.

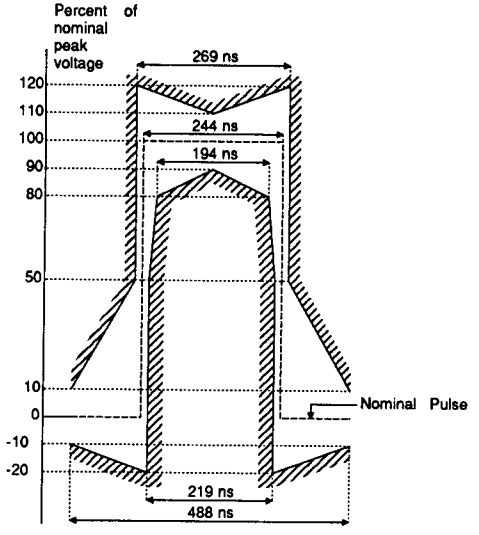


Figure 5 - Mask of the Pulse at the 2048 kbps Interface

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver typically is sensitive to signals down to approximately 325 mV in peak amplitude and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center-tapped on the CS6159 side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43801, 43802, AT&T 62411

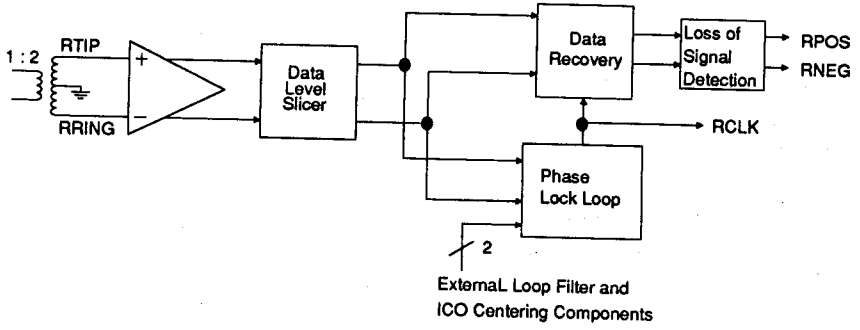


Figure 6. - Receiver Block Diagram

December 1988, Bellcore TR-TSY-000499 (Categories I & II), and CCITT REC. G.823. The center frequency of the PLL is controlled by the line length selection. Selection LEN2/1/0=000 sets the center frequency for PCM-30 operation. All other line length selections set the center frequency for T1 operation.

A block diagram of the receiver is shown in Figure 6. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. For all cases except where the PCM-30 pulse shape (LEN2/1/0 = 000) is selected, the comparator thresholds are dynamically established by peak detectors to be 65% of peak level. When the PCM-30 pulse shape is selected, the comparator threshold is 50% of peak level to improve signal to noise performance for long cable lengths.

The receiver uses a Phase Lock Loop (PLL) to recover the clock. The PLL has its center

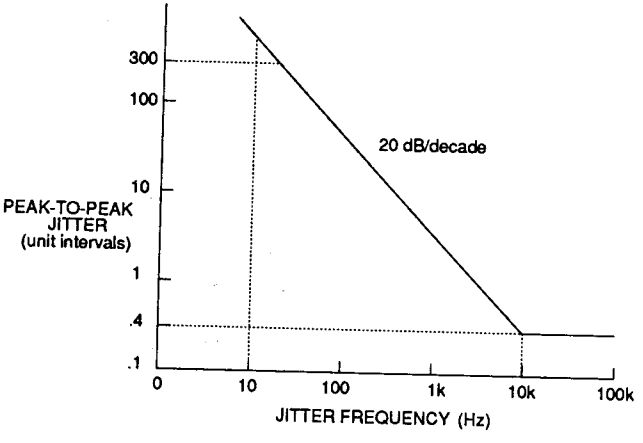


Figure 7. - Input Jitter Tolerance of Receiver

frequency set by an external resistor and by the line-length select inputs. This insures immunity to false lock over time and temperature variations.

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.325 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. Upon LOS the receiver substitutes ACLK for the incoming signal at RCLK (if ACLK is present) and forces RPOS and RNEG to zero. Therefore, RCLK will always be within required frequency limits (e.g.,± 50ppm). LOS returns to logic zero upon detection of 12.5% ones density. When LOS goes low, RCLK outputs the recovered clock, and RPOS and RNEG output the recovered data.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG, and outputs it at RCLK, RPOS and RNEG. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 1, high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

Remote Loopback

In remote loopback, the RCLK, RPOS and RNEG output signals are also sent back out on the line via TTIP and TRING. These signals are the recovered clock and data unless loss of signal has occurred and ACLK is present (see Loss of Signal section above). Transmitter inputs, TCLK, TPOS, TNEG, and TAOS, are ignored during remote loopback. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In remote loopback, the recovered clock is used to calibrate the transmitter delay line.

Power On Reset/Reset

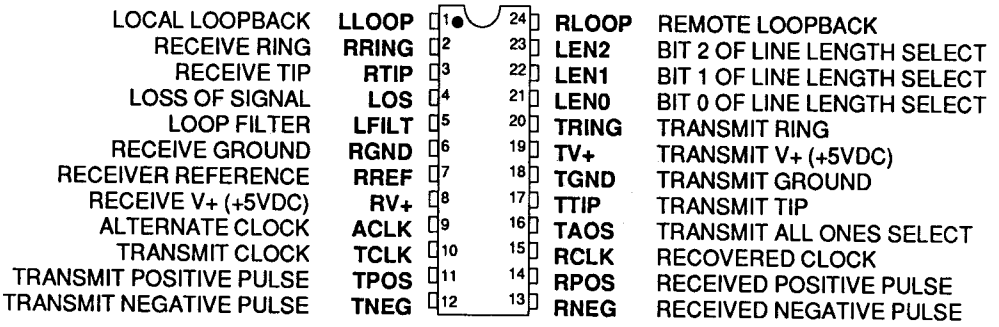
Upon power-up, the CS6159 is held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the transmitter delay line commences. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the transmitter delay line is continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset a CS6159 when in operation. However, a manual reset is made by simultaneously setting both RLOOP and LLOOP high for least 200 ns. Reset will initiate on the falling edge of RLOOP and LLOOP.

Power Supply

The device operates from a single 5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. However, these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. If the same power bus is used, the receive power supply should be decoupled from ground with a 68 µF tantalum capacitor and a mylar or ceramic 0.1 µF capacitor. A 1.0 µF mylar or ceramic capacitor should be used on the transmit power supply. These capacitors should be located physically close to the device. If separate power busses are used for TV+/TGND and RV+/RGND, an additional 68 µF capacitor should be used on the transmit supply. TV+ must not exceed RV+ by more than 0.3V.

PIN DESCRIPTIONS



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 19.
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 18.
Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 8.
Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 6.
Power supply ground for the device, except transmit drivers; typically 0 volts.

Control

LLOOP - Local Loopback, Pin 1.
Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 24.
Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Inputs on TCLK, TPOS, TNEG, and TAOS are ignored

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 21, 22 and 23.
Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection. Also controls the receiver slicing levels and receive PLL center frequency.

TAOS - Transmit All Ones Select, Pin 16.

Setting TAOS to logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.

Inputs

ACLK - Alternate External Clock Input, Pin 9.

Either a 1.544 MHz (or 2.048 MHz for CCITT) clock can be input to ACLK, which is substituted for RCLK upon loss of signal. If ACLK is grounded, no substitution takes place.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 10, 11 and 12.

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

3

RTIP, RRING - Receive Tip, Receive Ring, Pins 3 and 2.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK

RREF, LFILT - Receiver Reference, Loop Filter, Pins 7 and 5.

External components are connected to these pins to set the center-frequency of the PLL, and to provide a loop filter. Contact the factory for the recommended component values.

Status

LOS - Loss of Signal, Pin 4.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. LOS returns to a logic 0 when a 12.5% ones density signal returns.

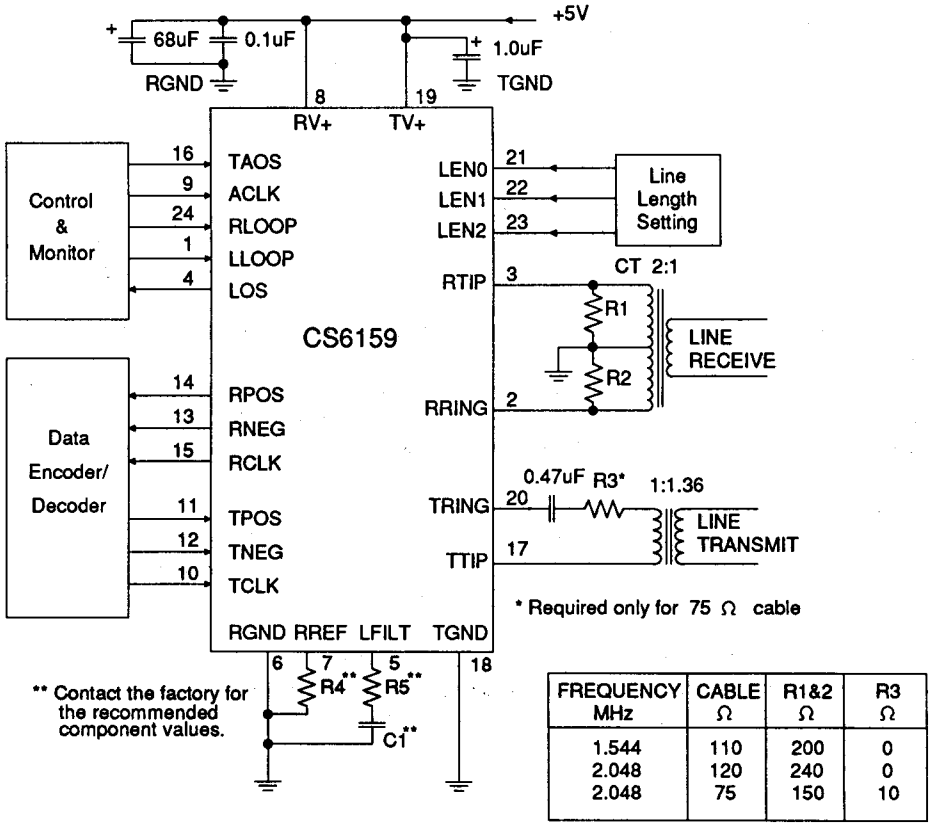
Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data, Pins 15, 14 and 13.

The recovered clock and NRZ data outputs of the receiver. RPOS and RNEG are stable and valid on the falling edge of RCLK. A positive pulse (with respect to ground) received on the RTIP pin is recovered by the receiver and causes a logic 1 to be output on RPOS. A positive pulse received on the RRING pin is recovered by the receiver and causes a logic 1 to be output on RNEG.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 17 and 20.

The AMI signal is driven to the line through these pins. This output is designed to drive a 54 Ω load. A 1.36:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, a 10 Ω resistor should be added as shown in Figure A1. The transmitter will drive twisted-shielded pair cable, terminated with 100 Ω or 120 Ω, without additional components.



FREQUENCY MHz	CABLE Ω	R1&2 Ω	R3 Ω
1.544	110	200	0
2.048	120	240	0
2.048	75	150	10

Figure A1: Typical Connection Diagram

APPLICATIONS

Line Interface

Figure A1 shows the typical application configuration for the CS6159. For T1 applications, the receiver transformer is center-tapped and center-grounded with 200 Ω resistors between the center tap and each leg on the CS6159 side. These resistors provide the 100 Ω termination for the T1 line.

When terminating 2.048 MHz twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

For transmitting data at 2.048 MHz onto a 75 Ω coax cable, a 10 Ω resistor is used between TTIP (or TRING) and the transformer. The resistor serves two functions. First, it provides the appropriate 54 Ω load to TTIP and TRING. Second, the resistor attenuates the signal slightly to meet the G.703 pulse amplitude requirements. Note that the 10 Ω resistor should not be used when interfacing to G.703 120 Ω cable. For the receiver, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Figure A1 shows a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any buildup in the

core of the transformer due to any DC imbalance that may be present at the differential outputs, TTIP and TRING. If DC saturates the transformer, a DC offset will result during the transmission of a space (zero) as the transformer tries to dump the charge and return to equilibrium. The blocking capacitor will keep DC current from flowing in the transformer.

Transformers

The CS6159 requires two transformers. A 1:1.36 step-up transformer is used with the transmitter while a 1:2 center-tapped transformer is used with the receiver. The same transformers may be used with the CS6159 in both T1 and CEPT applications, although some CEPT applications may be subject to more stringent safety requirements in other countries imposing additional constraints upon the transformers. Contact the appropriate PTT or regulatory agency for more information on applicable performance and safety requirements. The recommended transmitter and receiver transformer specifications and approved vendor part numbers are summarized below.

Key receiver transformer specifications:

Turns ratio: 1:2 center-tapped (or 1:1:1).

Other specifications: not critical.

The transformers listed in Table A1 have been approved for use with the CS6159 receiver.

RECEIVER

Manufacturer	Part #
Pulse Engineering	PE-64931
Schott Corp.	67124670

Table A1. - Approved Receiver Transformers

Key transmitter transformer specifications:

Turns ratio: 1:1.36

Primary inductance: 600 µH min measured at 10kHz and 0.005 VRMS.

Leakage inductance: 1.3 µH max with secondary shorted.

Interwinding capacitance: 23 pF max, primary to secondary.

ET-Constant: 16 V-µs min. for T1,
12 V-µs for CEPT.

The transformers listed in Table A2 have been approved for use with the CS6159 transmitter.

TRANSMITTER

Manufacturer	Part #
Pulse Engineering	PE-64937
Schott	67112020

Table A2. - Approved Transmitter Transformers

Interfacing The CS6159 With The CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A2.

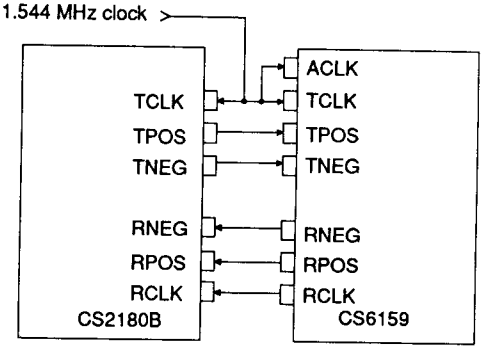


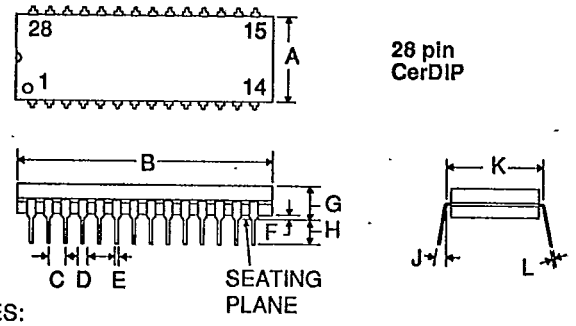
Figure A2. - Interfacing the CS6159 with CS2180B

CRYSTAL

MECHANICAL DATA

T-90-20

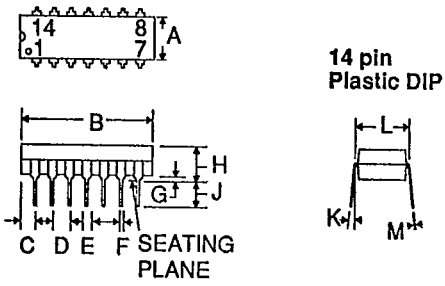
MECHANICAL DATA



28 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	36.45	37.85	1.435	1.490
C	2.54 BSC		0.100 BSC	
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

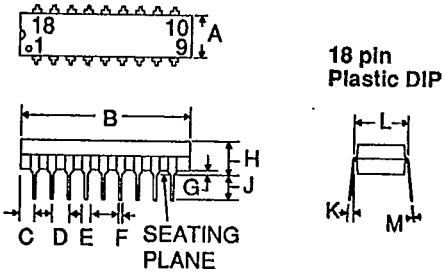
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



14 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.54	19.56	0.730	0.770
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

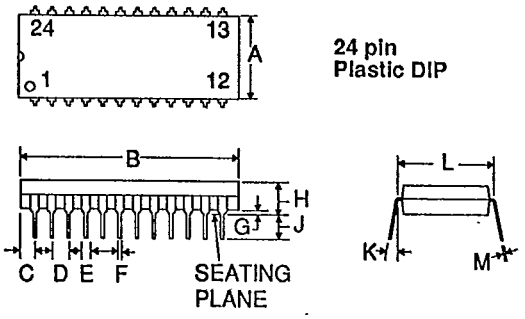
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



18 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	22.22	23.24	0.875	0.915
C	1.02	1.52	0.040	0.060
D	2.54 BSC		0.100 BSC	
E	1.27	1.78	0.050	0.070
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.56	4.57	0.140	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

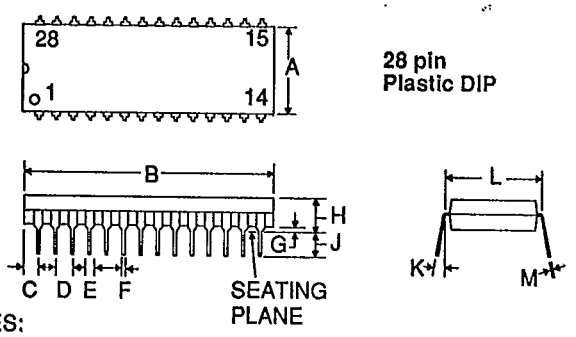
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

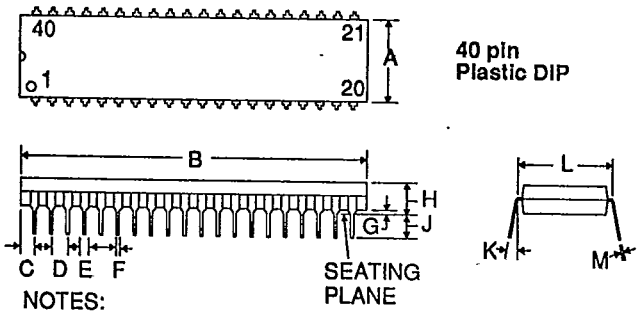
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



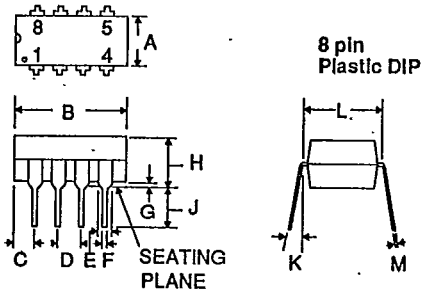
40 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	51.69	52.45	2.035	2.065
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

12

T-90-20



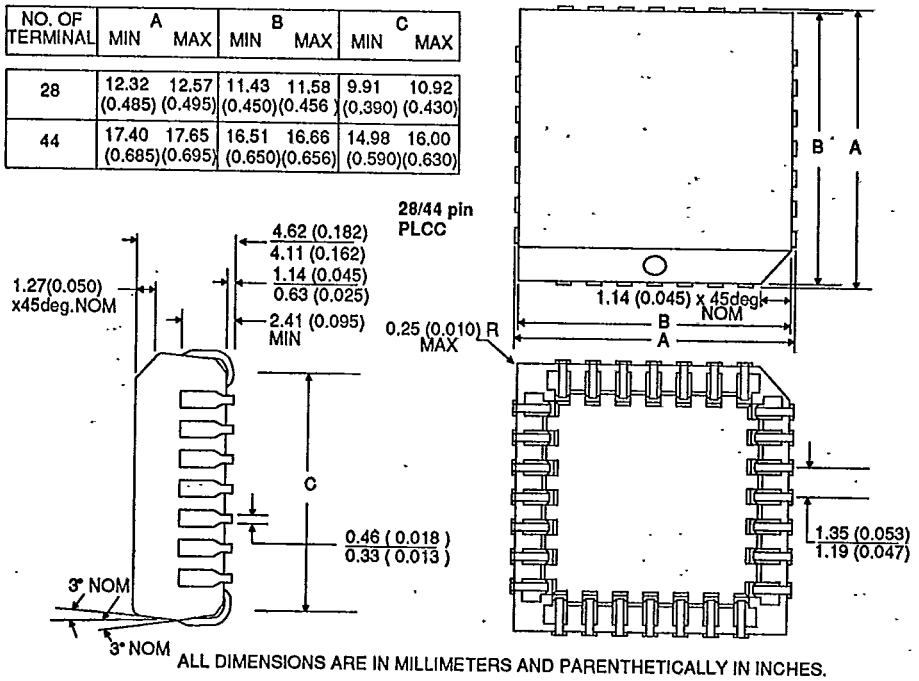
8 pin
Plastic DIP

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)

28/44 pin
PLCC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.