



Integrated Device Technology, Inc.

16K x 32 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4031

FEATURES:

- High density 512K static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line Package)
- Ultra-fast access time: 8ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ($\pm 10\%$) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

PIN CONFIGURATION⁽¹⁾

PD0	2	1	GND	PD1	3	PD0 - GND
I/O0	4	5	I/O8	PD1 - OPEN		
I/O1	6	7	I/O9			
I/O2	8	9	I/O10			
I/O3	10	11	I/O11			
VCC	12	13	A0			
A7	14	15	A1			
A8	16	17	A2			
A9	18	19	I/O12			
I/O4	20	21	I/O13			
I/O5	22	23	I/O14			
I/O6	24	25	I/O15			
I/O7	26	27	GND			
WE	28	29	NC			
NC	30	31	CS2			
CS1	32					
		33	CS4			
CS3	34	35	NC			
NC	36	37	OE			
GND	38	39	I/O24			
I/O16	40	41	I/O25			
I/O17	42	43	I/O26			
I/O18	44	45	I/O27			
I/O19	46	47	A3			
A10	48	49	A4			
A11	50	51	A5			
A12	52	53	VCC			
A13	54	55	A6			
I/O20	56	57	I/O28			
I/O21	58	59	I/O29			
I/O22	60	61	I/O30			
I/O23	62	63	I/O31			
GND	64					

ZIP
TOP VIEW

NOTE:

1. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the depth of the module. If PD0 reads GND and PD1 reads Open, then the module has 16K depth.

DESCRIPTION:

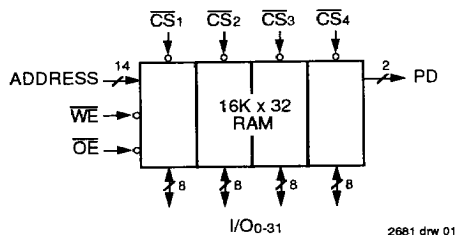
The IDT7MP4031 is a 16K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 16K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high performance, high reliability BiCEMOS™ or CEMOS™ technology. The IDT7MP4031 is available with access time as fast as 8ns with minimal power consumption.

The IDT7MP4031 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line Package). The dual row configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low profile package is ideal for systems with minimum board spacing.

All inputs and outputs of the IDT7MP4031 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 16K depth.

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

I/O0-31	Data Input/Output
A0-13	Addresses
CS1-4	Chip Select
WE	Write Enable
OE	Output Enable
PD0-1	Depth Identification
VCC	Power
GND	Ground

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COMMERCIAL TEMPERATURE RANGE

APRIL 1992

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DSC-7054/3

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CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	V(IN) = 0V	15	pF
CIN(A)	Input Capacitance (Address & Control)	V(IN) = 0V	70	pF
COUT	Output Capacitance	V(OUT) = 0V	15	pF

NOTE:

1. This parameter is guaranteed by design, but not tested.

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH ⁽²⁾	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTES:

1. VIL (min) = -1.5V for pulse width less than 10ns.
2. I/O pins must not exceed VCC +0.5V.

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	7MP4031S	7MP4031B	Unit
				Max.	Max.	
ILI	Input Leakage (Address and Control)	VCC = Max.; VIN = GND to VCC	—	40	80	μA
ILI	Input Leakage (Data)	VCC = Max.; VIN = GND to VCC	—	5	10	μA
ILO	Output Leakage	VCC = Max.; CS = VIH, VOUT = GND to VCC	—	5	10	μA
VOL	Output Low	VCC = Min., IOL = 8mA	—	0.4	0.4	V
VOH	Output High	VCC = Min., IOH = -4mA	2.4	—	—	V

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Symbol	Parameter	Test Conditions	7MP4031B	7MP4031S	Unit
			8 - 15ns Max.	20 - 35ns Max.	
ICC	Dynamic Operating Current	VCC = Max.; CS = VIL; f = fMAX Output Open	1600	1200	mA
ISB	Standby Supply Current	CS ≥ VIH, VCC = Max. f = fMAX, Outputs Open	—	480	mA
ISB1	Full Standby Supply Current	CS ≥ VCC - 0.2V; f = 0, VIN > VCC - 0.2V or < 0.2V	—	160	mA

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TRUTH TABLE

Mode	CS	OE	WE	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATAOUT	Active
Write	L	X	L	DATAIN	Active
Read	L	H	H	High-Z	Active

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. I/O pins must not exceed VCC +0.5V.

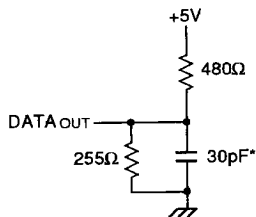
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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

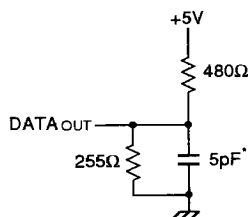
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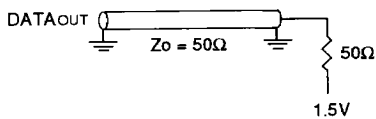
Figure 1. Output Load

*Including scope and jig.



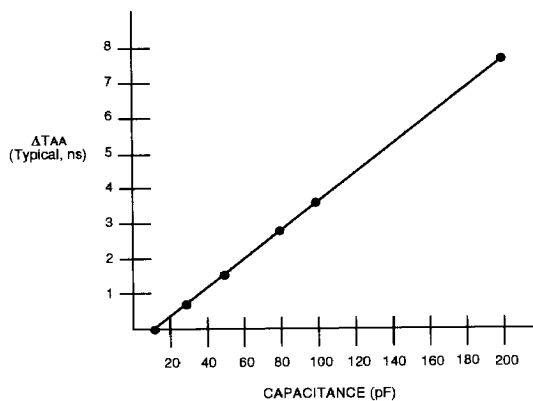
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Figure 2. Output Load
(for tCHZ, tCLZ, tOHZ, tOLZ, tWHZ and tOW)



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Figure 3. Alternate Output Load



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Figure 4. Alternate Lumped Capacitive Load,
Typical Derating

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4031BxxZ						Unit
		-8 ⁽²⁾		-10 ⁽²⁾		-12		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	8	—	10	—	12	—	ns
tAA	Address Access Time	—	8	—	10	—	12	ns
tACS	Chip Select Access Time	—	8	—	10	—	12	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low Z	1	—	1	—	1	—	ns
tOE	Output Enable to Output Valid	—	4	—	5	—	6	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low Z	1	—	1	—	1	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High Z	—	6	—	7	—	8	ns
tOHZ ⁽¹⁾	Output Disable to Output in High Z	—	3	—	3	—	3	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
Write Cycle								
tWC	Write Cycle Time	8	—	10	—	12	—	ns
tcw	Chip Select to End of Write	8	—	8	—	9	—	ns
tAW	Address Valid to End of Write	8	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	8	—	9	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
twHz ⁽¹⁾	Write Enable to Output in High Z	—	3	—	3	—	3	ns
tDW	Data to Write Time Overlap	5	—	5	—	6	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tow ⁽¹⁾	Output Active from End of Write	3	—	3	—	3	—	ns

NOTES:

1. This parameter is guaranteed, but not tested.
2. Preliminary specifications only.

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AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C to +70°C)

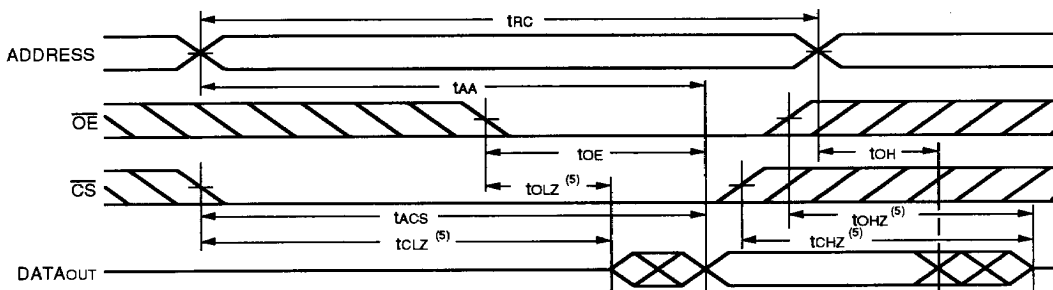
Symbol	Parameter	7MP4031BxxZ		7MP4031SxxZ						Unit
		-15		-20		-25		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	ns
tAA	Address Access Time	—	15	—	20	—	25	—	35	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	15	—	20	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High Z	—	7	—	8	—	10	—	15	ns
tOHZ ⁽¹⁾	Output Disable to Output in High Z	—	7	—	8	—	10	—	15	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	35	ns
Write Cycle										
tWC	Write Cycle Time	14	—	17	—	20	—	30	—	ns
tCW	Chip Select to End of Write	14	—	17	—	20	—	25	—	ns
tAW	Address Valid to End of Write	14	—	17	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High Z	—	6	—	7	—	7	—	10	ns
tDW	Data to Write Time Overlap	10	—	10	—	13	—	15	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

NOTE:

1. This parameter is guaranteed, but not tested.

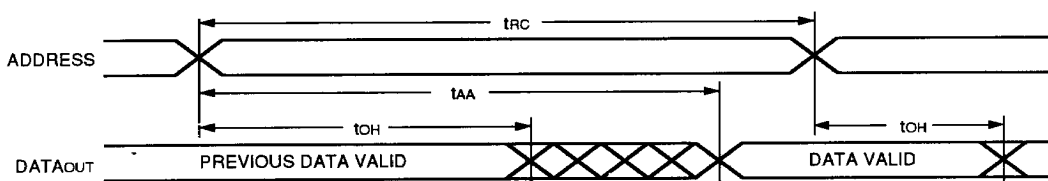
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TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



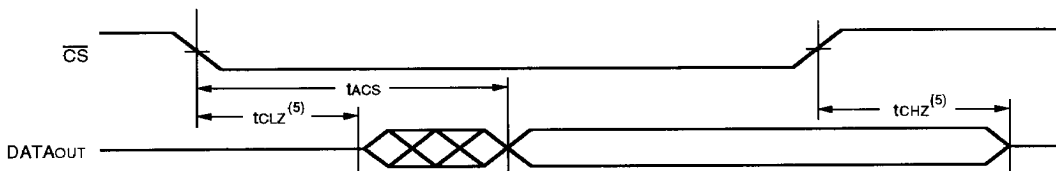
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TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)



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TIMING WAVEFORM OF READ CYCLE NO. 3^(1,3,4)

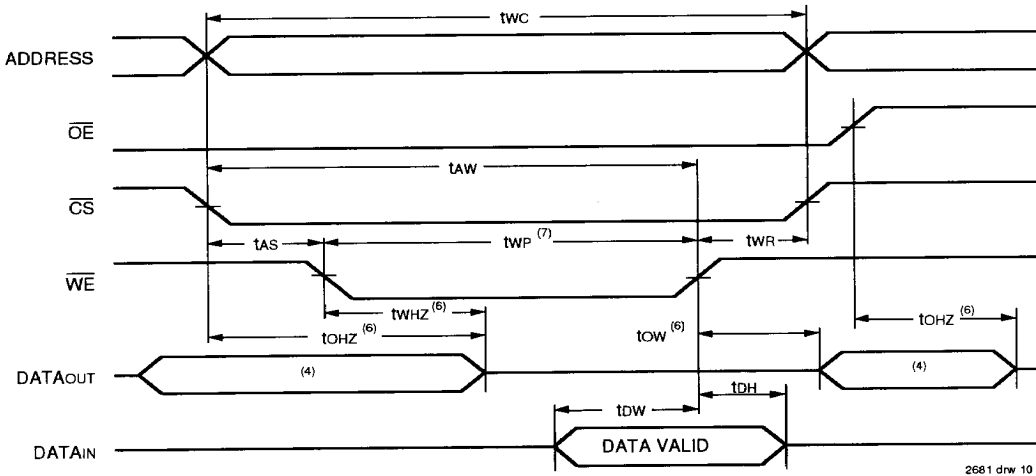


2681 drw 09

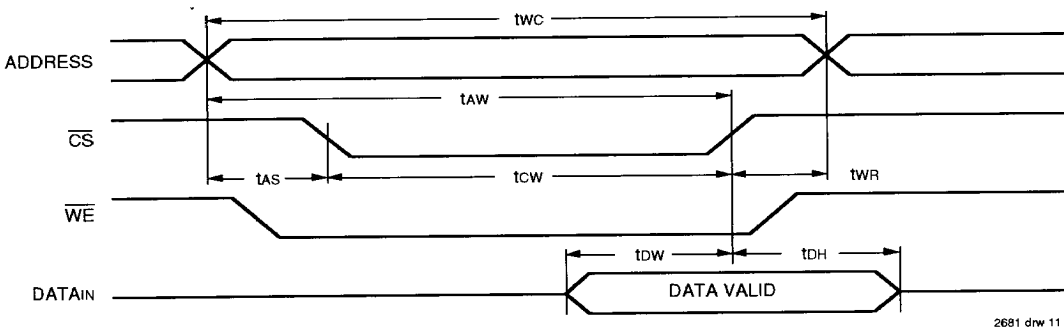
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200mV$ from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



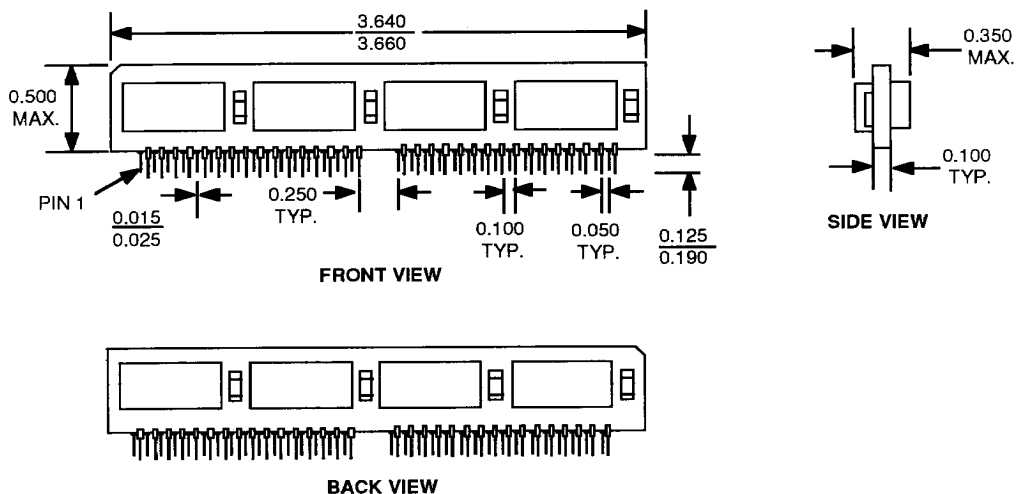
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{OW}$) to allow the I/O drivers to turn off data and to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

PACKAGE DIMENSIONS



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