Integrated Device Technology, Inc.

256K x 8 CMOS STATIC RAM MODULE

IDT7MP4034

FEATURES:

- High density separate I/O, 2 megabit CMOS static RAM module
- Fast access time: 10ns (max.)
- Low profile 42-pin ZIP (Zig-zag In-line vertical Package)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

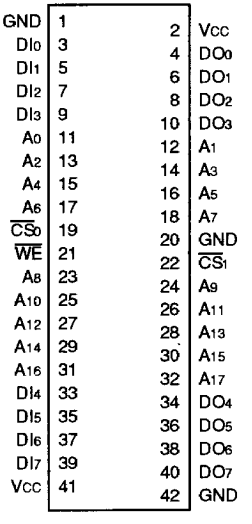
DESCRIPTION:

The IDT7MP4034 is a separate I/O, 256K x 8 CMOS static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 1 static RAMs in plastic SOJ packages. Availability of two chip select lines (one for each group of four RAMs) provides nibble access and allows the user to configure the memory into a 256K x 8 or a 512K x 4 organization. The IDT7MP4034 is available with access times as fast as 10ns with minimal power consumption.

The IDT7MP4034 is packaged in a 42-pin FR-4 ZIP (Zig-zag In-line vertical Package). The memory configuration results in a package 2.65 inches long and 0.35 inches wide. At only 0.5 inches high, this low profile package is ideal for high performance systems with minimum board spacing.

All inputs and outputs of the IDT7MP4034 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation.

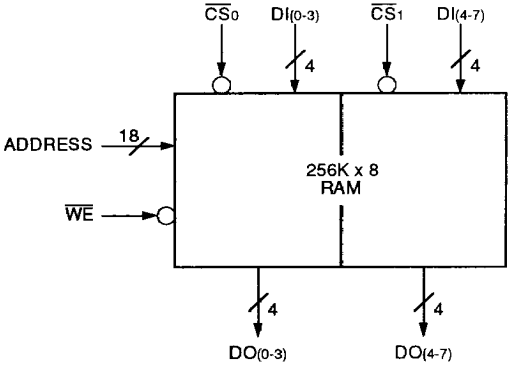
PIN CONFIGURATION



ZIP
TOP VIEW

2745 drw 01

FUNCTIONAL BLOCK DIAGRAM



2745 drw 02

PIN NAMES

DI0-7	Data Inputs
DO0-7	Data Outputs
A0-17	Address Inputs
$\overline{CS}_{0-1}$	Chip Selects
$\overline{WE}$	Write Enable
VCC	Power
GND	Ground

2745 tbl 01

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7-32-1

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2745 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2745 tbl 04

NOTE:
1. V_{IL} = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2745 tbl 05

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	$DATA_{IN}$	Active

2745 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	92	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

2745 tbl 06

NOTE:
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, T_A = 0°C TO +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2745 tbl 07

Symbol	Parameter	Test Conditions	10-12ns Max.	15-45ns Max.	Unit
I_{CC}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max., f = f_{MAX}	1520	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	560	320	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} > V_{CC} - 0.2V or < 0.2V, f = 0	240	240	mA

2745 tbl 08

NOTE:
1. 10, 12, 15, and 17ns are preliminary specifications only.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2745 tbl 09

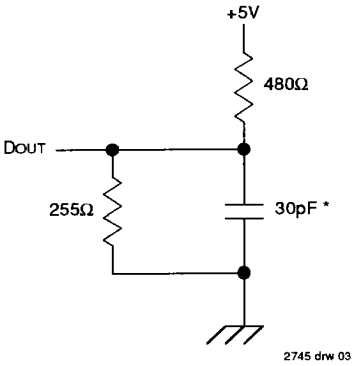

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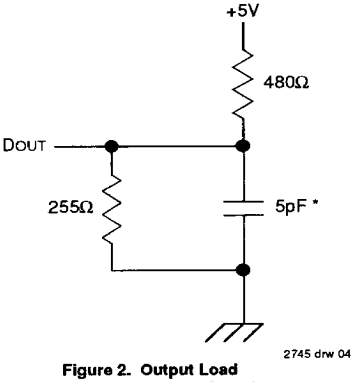
Figure 1. Output Load

* Including scope and jig.



2745 drw 04

Figure 2. Output Load (for tCHZ, tCLZ, tow and tWHZ)

AC ELECTRICAL CHARACTERISTICS(2)

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP4034SxxZ -10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-17 Min.	-17 Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	10	—	12	—	15	—	17	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	17	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	17	ns
tCLZ (1)	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	ns
tCHZ (1)	Chip Deselect to Output in High Z	—	10	—	10	—	10	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tPU (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD (1)	Chip Deselect to Power Down Time	—	10	—	12	—	15	—	17	ns
WRITE CYCLE										
tWC	Write Cycle Time	10	—	12	—	15	—	17	—	ns
tCW	Chip Select to End of Write	10	—	12	—	13	—	15	—	ns
tAW	Address Valid to End of Write	10	—	10	—	13	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	10	—	13	—	15	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ (1)	Write Enable to Output in High Z	—	5	—	5	—	8	—	9	ns
tDW	Data to Write Time Overlap	8	—	10	—	10	—	11	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW (1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

2745 tbl 10

NOTES:
1. This parameter is guaranteed by design but not tested.
2. 10,12,15, and 17ns are preliminary specifications only.

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

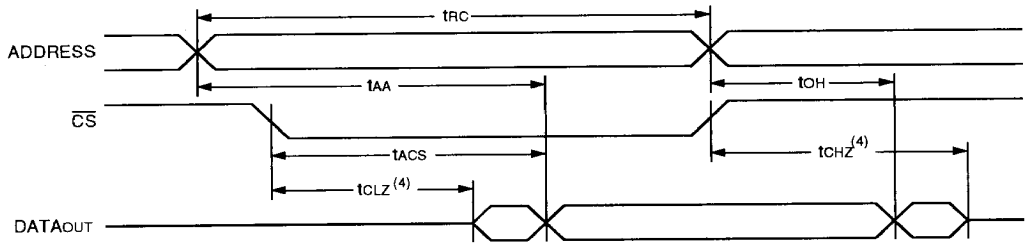
Symbol	Parameter	7MP4034SxxZ								
		-20		-25		-35		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Deselect to Output in High Z	—	10	—	13	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	20	—	25	—	35	—	45	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t_{CW}	Chip Select to End of Write	17	—	22	—	30	—	40	—	ns
t_{AW}	Address Valid to End of Write	17	—	22	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	17	—	22	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	10	—	13	—	20	—	25	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW} (1)	Output Active from End of Write	—	0	—	0	—	0	—	0	ns

2745 tbl 11

NOTE:
1. This parameter is guaranteed by design but not tested.

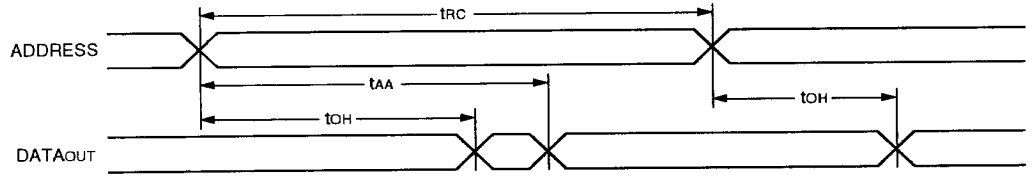
7-32-4

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



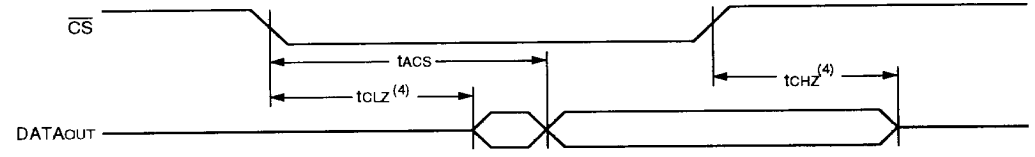
2745 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)



2745 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)



2745 drw 07

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NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

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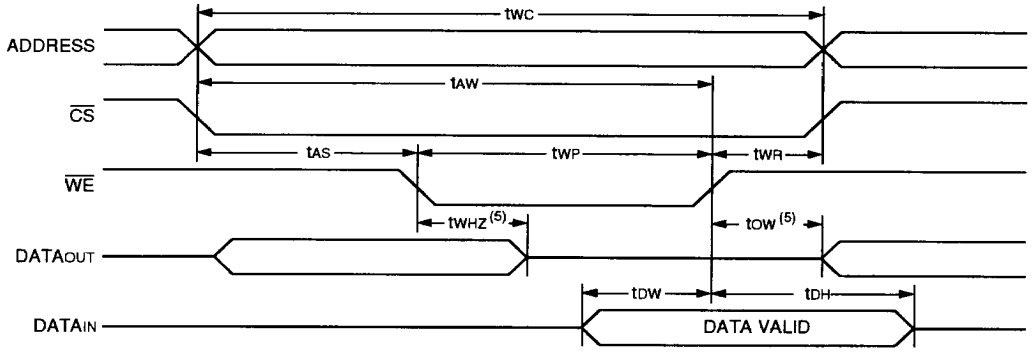
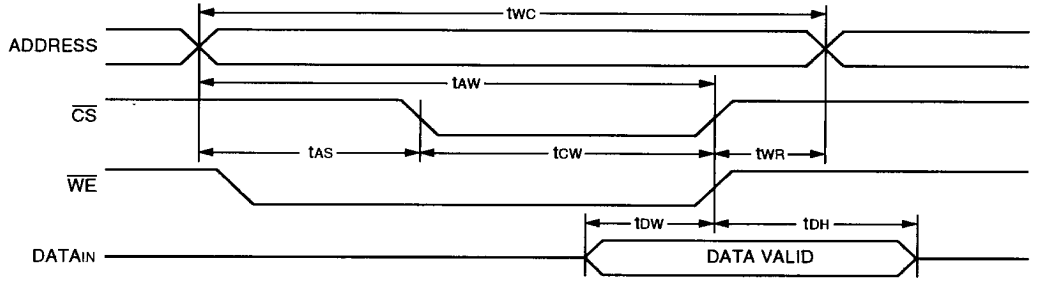
TIMING WAVEFORM OF WRITE CYCLE NO. 1[1, 2, 3] ($\overline{WE}$ CONTROLLED TIMING)



2745 drw 08

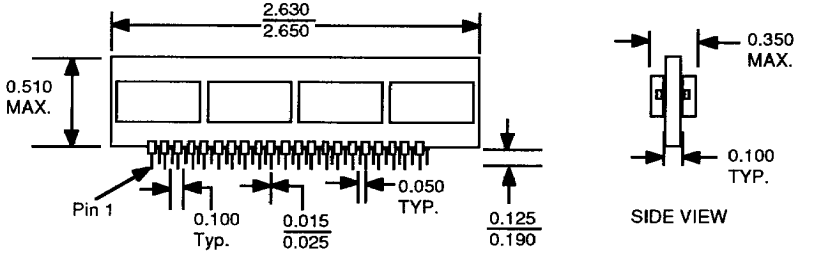
TIMING WAVEFORM OF WRITE CYCLE NO. 1[1, 2, 3, 4] ($\overline{CS}$ CONTROLLED TIMING)



2745 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneous with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

PACKAGE DIMENSIONS



2745 drw 10

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