M35501FP

FLD (VFD) DIGIT EXPANDER

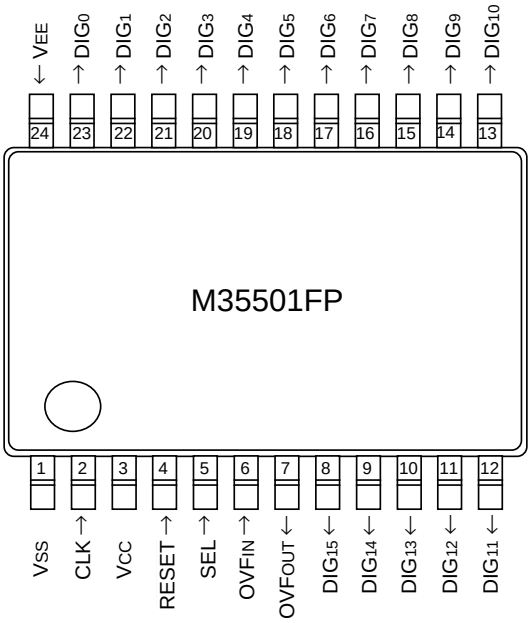
DESCRIPTION

The M35501FP generates digit signals for fluorescent display when connected to the output port of a microcomputer. There are up to 16 digit pins available, and more can be added by connecting additional M35501FPs. The number of fluorescent displays can be increased easily by connecting the M35501FP to the CMOS FLD (VFD; Vacuum Fluorescent Display) output pins of an 8-bit microcomputer in MITSUBISHI's 38B5 Group. The M35501FP is suitable for fluorescent display control on household electric appliances, audio products, etc.

FEATURES

- Digit output ..... 16 (maximum)
  - •Up to 16 pins can be selected
  - •More digits available by connecting additional M35501FPs
  - •Output structure: high-breakdown voltage, P-channel open-drain; built-in pull-down resistor between digit output pins and VEE pin
- Power-on reset circuit ..... Built-in
- Power source voltage ..... 4.0 to 5.5 V
- Pull-down power source voltage ..... Vcc – 43 V
- Operating temperature range ..... –20 to 85 °C
- Package 24P2E
- Power dissipation ..... 250µW (at 100 kHz operation clock)

PIN CONFIGURATION (TOP VIEW)



Outline: 24P2E-A
24-pin plastic-molded SSOP

Fig. 1 Pin configuration of M35501FP

FUNCTIONAL BLOCK

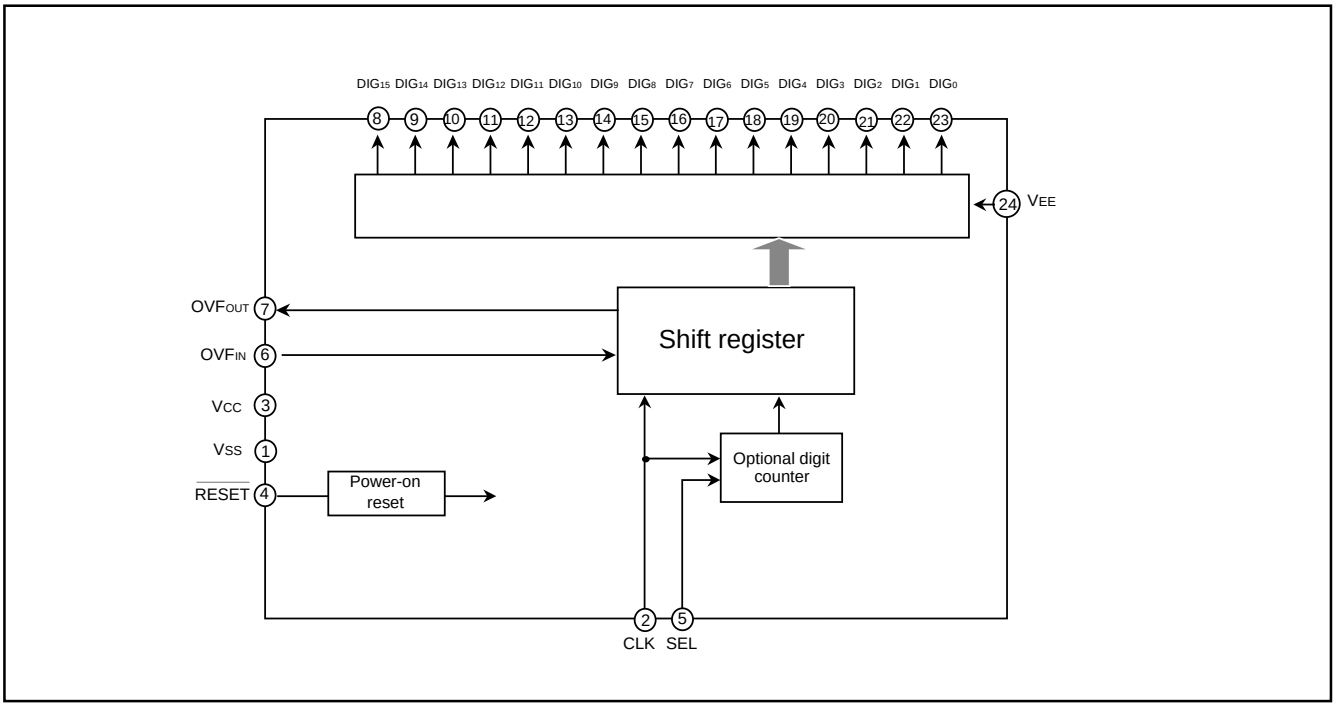


Fig. 2 Functional block diagram

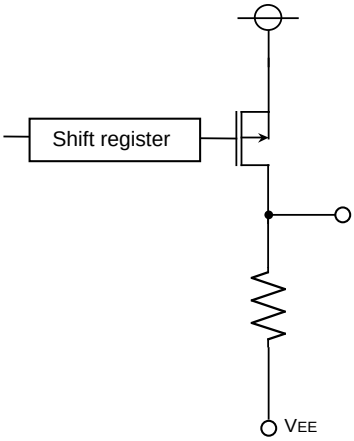
PIN DESCRIPTION

Table 1 Pin description

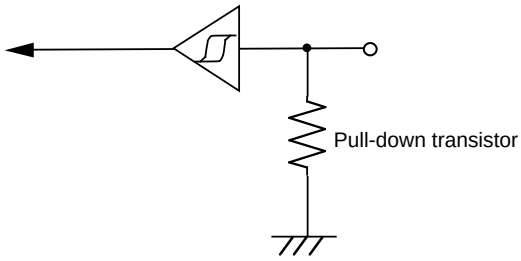
Pin	Name	Function	Output Structure	Fig. No.
VCC, VSS	Power source input	Apply 4.0–5.5 V to Vcc, and 0V to Vss.	–	–
$\overline{\text{RESET}}$	Reset input	Reset internal shift register (built-in power-on reset circuit).	CMOS input level Built-in pull-up resistor	3
CLK	Clock input	Digit output varies according to rising edge of clock input.	CMOS input level Built-in pull-down resistor	2
SEL	Select input	Use when specifying the number of digits.	CMOS input level Built-in pull-down resistor	2
OVFIN	Overflow signal input	Input "H" when using one M35501FP. Connect to OVFOUT pin of additional M35501FPs when using multiple M35501FPs (to use 17 digits or more).	CMOS input level	4
OVFOUT	Overflow signal output	Leave open when using one M35501FP. Connect to OVFIN pin of additional M35501FPs when using multiple M35501FPs (to use 17 digits or more).	CMOS output	5
DIG15–DIG0	Digit output	Output the digit output waveform of fluorescent display. Leave open when not in use (VEE level output).	High-breakdown-voltage P-channel open-drain output Built-in pull-down resistor	1
VEE	Pull-down power source input	Apply voltage to DIG0–DIG15 pull-down resistors.	–	–

PORT BLOCK

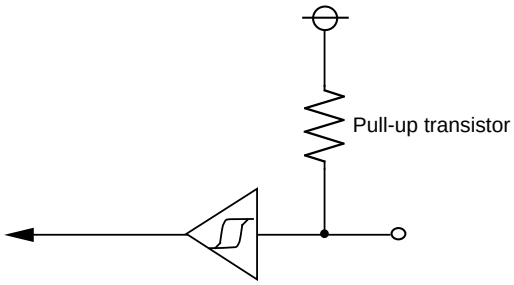
(1) DIG_0–DIG_{15}



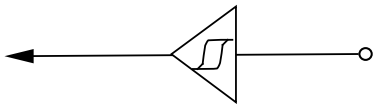
(2) SEL, CLK



(3) $\overline{RESET}$



(4) OVF_{IN}



(5) OVF_{OUT}

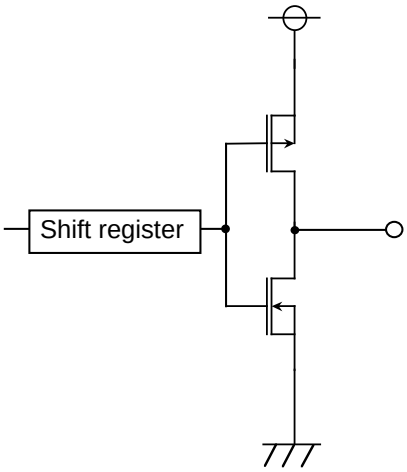


Fig. 3 Port block diagram

USAGE

Three usages of the M35501FP are described below.

(1) 16-Digit Mode: 16 digits selected

The number of digits is set to 16 by fixing the OVFIN pin to "H" and the SEL pin to "L." Figure 5 shows the output waveform.

(2) Optional Digit Mode: 1-16 digits selectable

When the number of CLK pin rising edges during an "H" period of the SEL pin is n and the OVFIN pin is fixed to "H," the number of digits set is n. If n is 16 or more, all 16 digits are set. Figure 6 shows the output waveform.

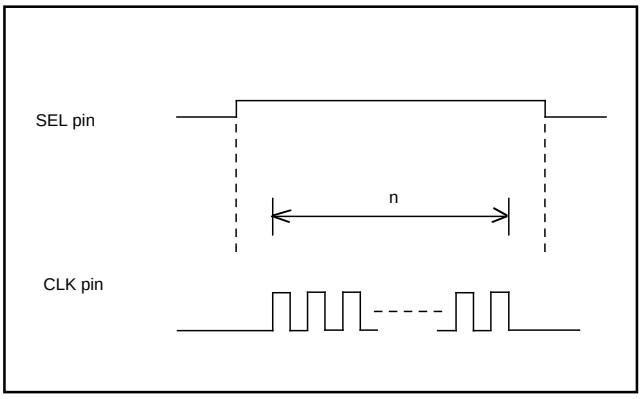


Fig. 4 Digit setting

(3) Cascade Mode: 17 digits or more selectable

17 digits or more can be used by connecting two M35501FPs or more. Figure 7 shows an example using three M35501FPs, offering 33 to 48 digit outputs.

Cascade mode will not operate if all M35501FPs are in 16-digit mode (SEL = "L"). Use the most significant M35501FP in the optional digit mode for DIG output. Figure 8 shows the output waveform.

DIGIT OUTPUT WAVEFORM

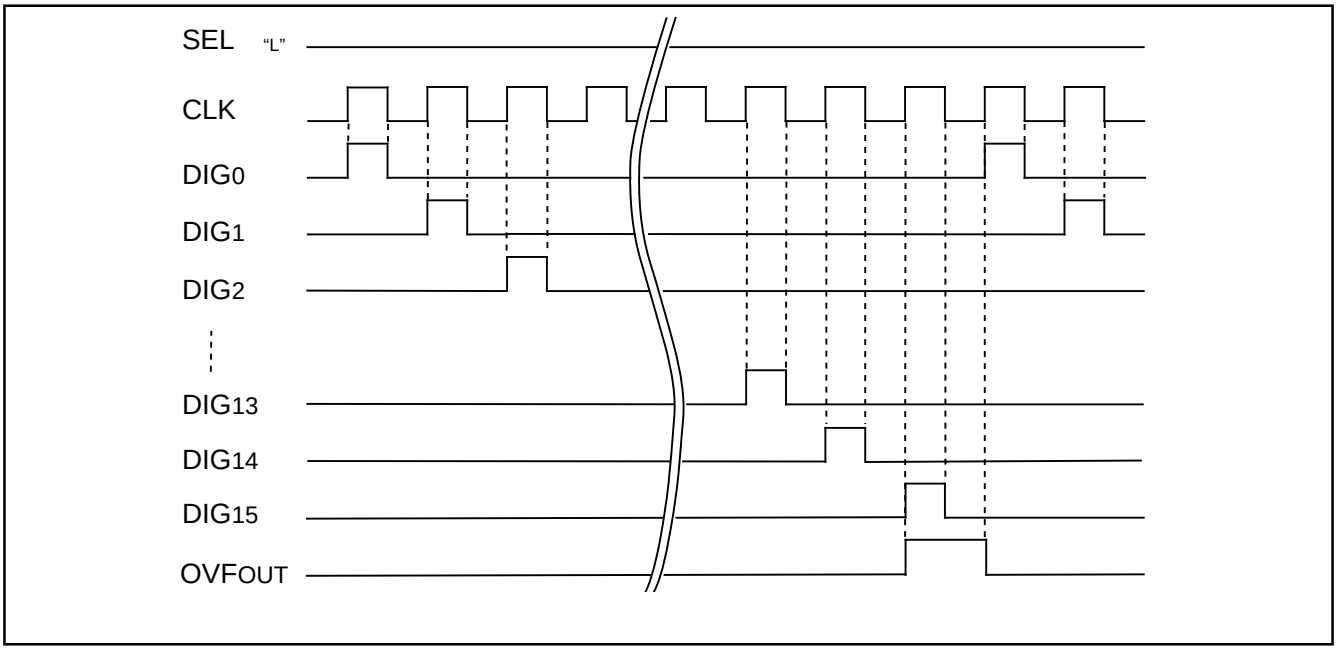


Fig. 5 16-digit mode output waveform

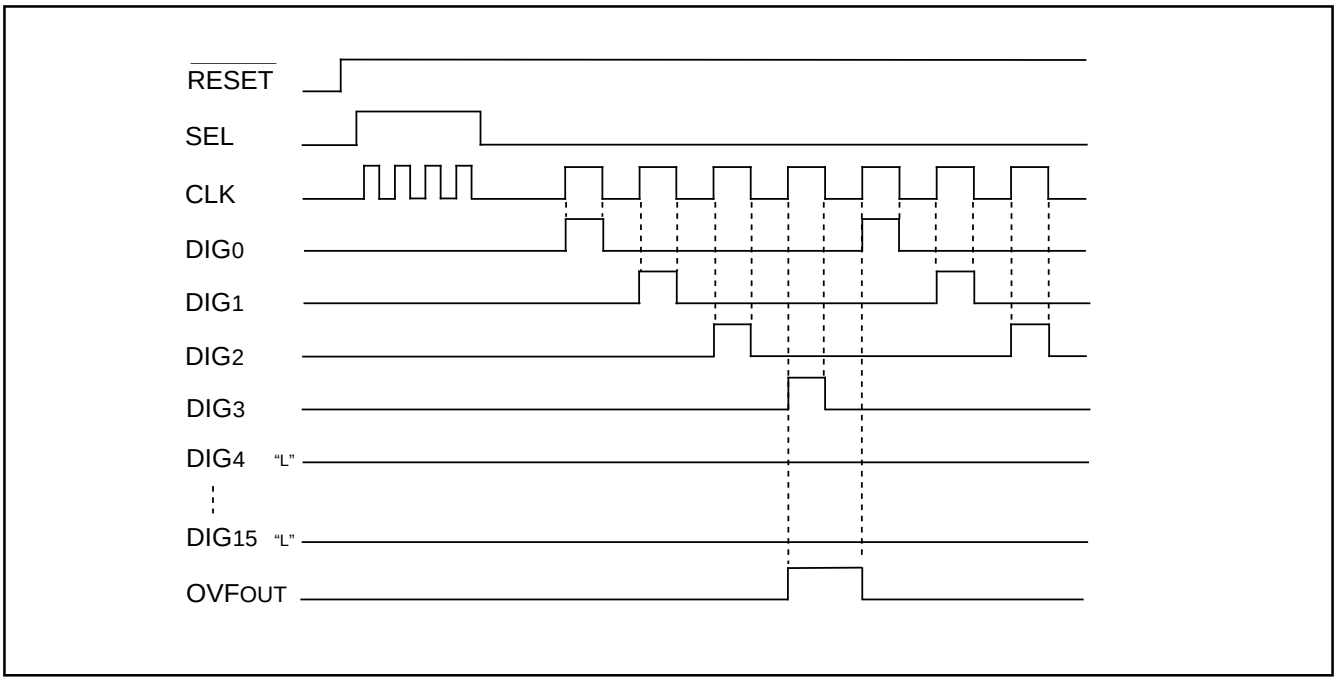


Fig. 6 Optional digit mode output waveform

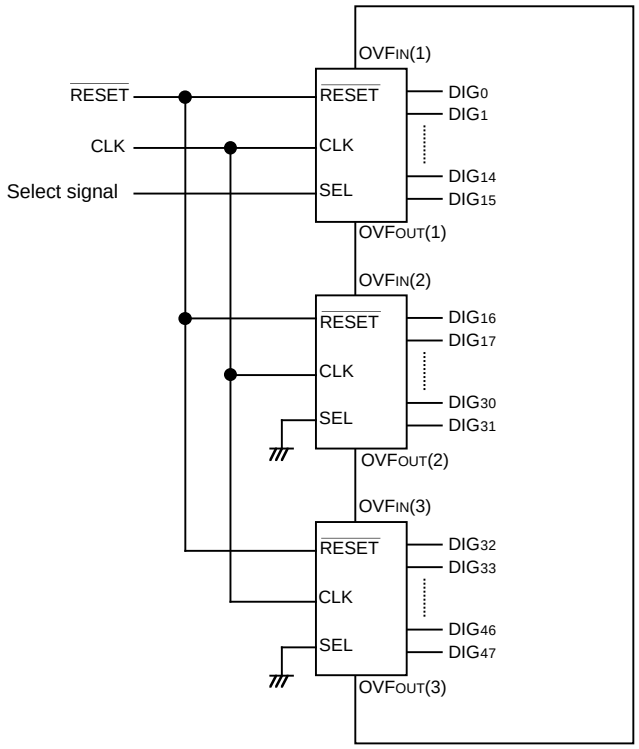


Fig. 7 Cascade mode connection example: 17 digits or more selected

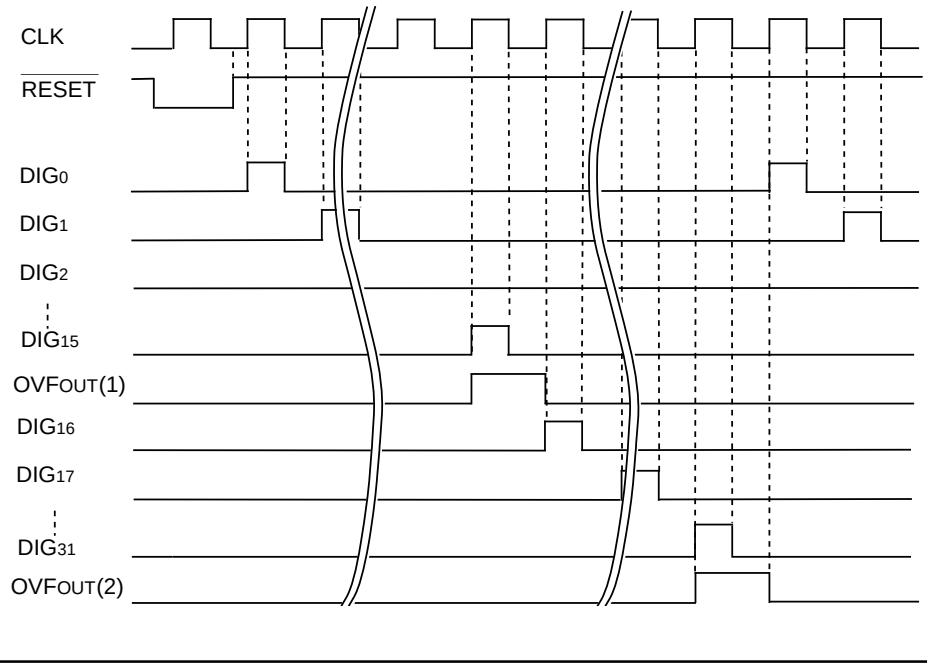


Fig. 8 Cascade mode output waveform

The number of fluorescent displays can be increased by connecting the M35501FP to the CMOS FLD output pins on a 38B5 Group microcomputer.

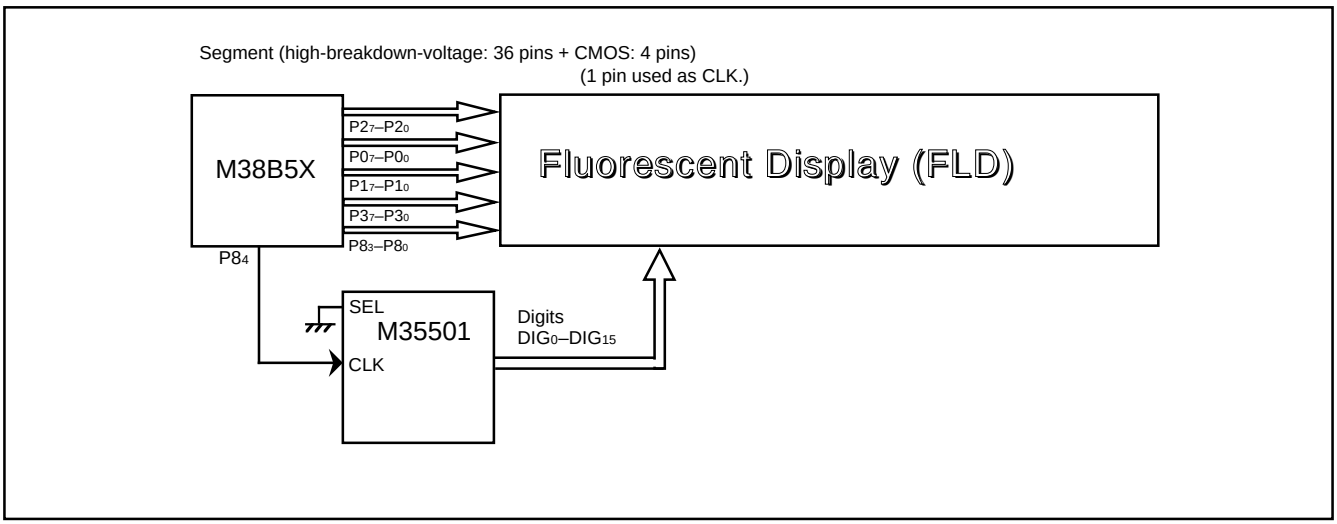


Fig. 9 Connection example with 38B5 Group microcomputer (1 to 16 digits)

This FLD controller can control up to 32 digits using the 32 timing mode of the 38B5 Group microcomputer.

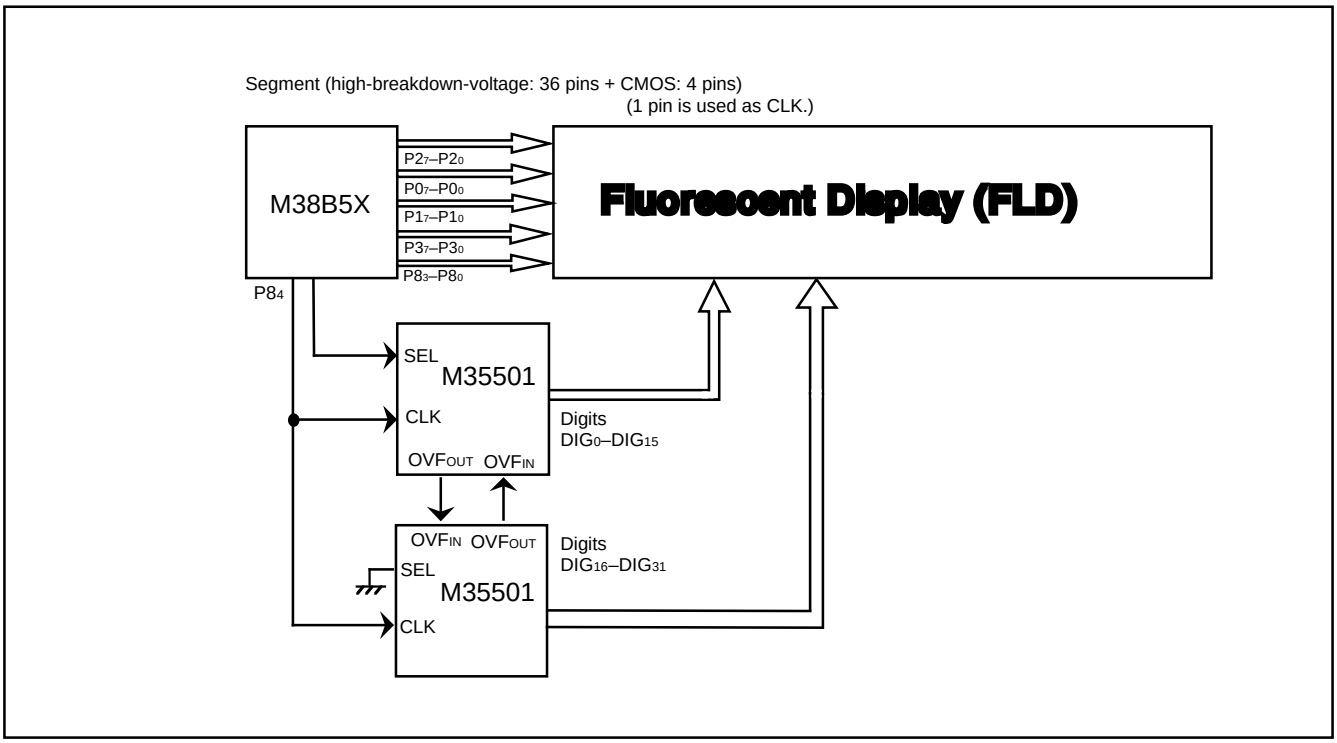


Fig. 10 Connection example with 38B5 Group microcomputer (17 to 32 digits)

RESET CIRCUIT

To reset the controller, the $\overline{\text{RESET}}$ pin should be held at "L" for 2 µs or more. Reset is released when the $\overline{\text{RESET}}$ pin is returned to "H" and the power source voltage is between 4.0 V and 5.5 V.

Notes1: Perform the reset release when CLK input signal is "L."
2: When setting the number of digits by SEL signal, optional digit counter is set to "0" by reset.

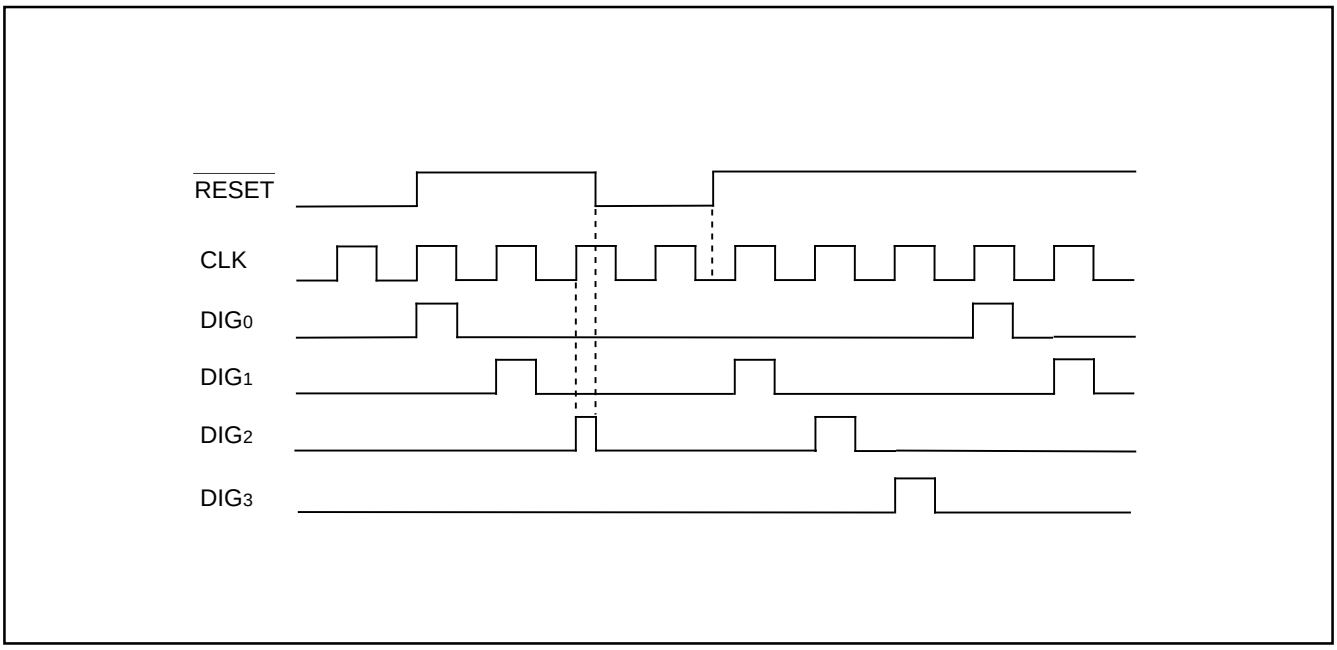


Fig. 11 Digit output waveform when reset signal is input

POWER-ON RESET

Reset can be performed automatically during power on (power-on reset) by the built-in power-on reset circuit. When using this circuit, set 100 μs or less for the period in which it takes to reach minimum operation guaranteed voltage from reset.

If the rising time exceeds 100 μs, connect the capacitor between the $\overline{\text{RESET}}$ pin and VSS at the shortest distance. Consequently, the $\overline{\text{RESET}}$ pin should be held at "L" until the minimum operation guaranteed voltage is reached.

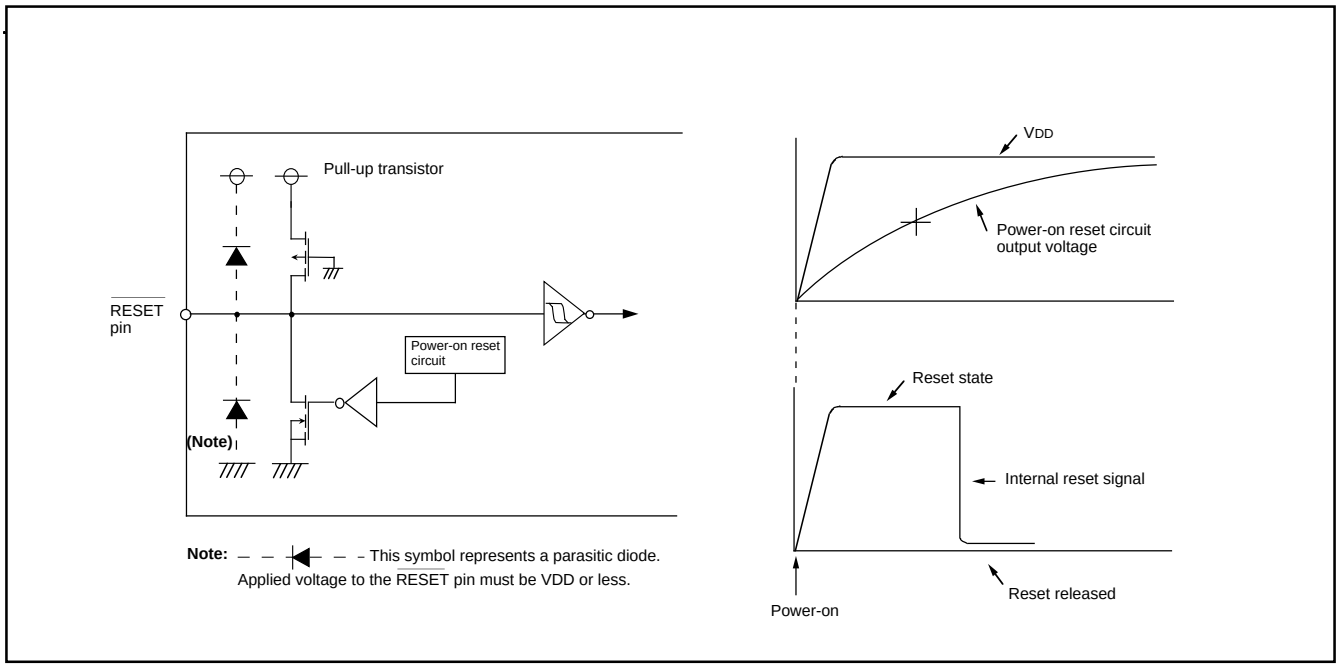


Fig. 12 Power-on reset circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	•All voltages are based on V_{SS}.	–0.3 to 7.0	V
V_{EE}	Pull-down power source voltage	•Output transistors are off.	V_{CC} –45 to V_{CC} +0.3	V
V_I	Input voltage CLK, SEL, OVF_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage DIG_0–DIG_{15}		V_{CC} –45 to V_{CC} +0.3	V
V_O	Output voltage OVF_{OUT}		–0.3 to V_{CC} +0.3	V
P_d	Power dissipation	Ta = 25 °C	250	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage	4.0	5.0	5.5	V
V_{SS}	Power source voltage		0		V
V_{EE}	Pull-down power source voltage	V_{CC} –43		V_{SS}	V
V_{IH}	"H" input voltage CLK, SEL, OVF_{IN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage CLK, SEL, OVF^{IN}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.2V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current DIG_0 – DIG_{15} **(Note 1)**			–36	mA
$I_{OH(peak)}$	"H" peak output current OVF_{OUT} **(Note 1)**			–10	mA
$I_{OL(peak)}$	"L" peak output current OVF_{OUT} **(Note 1)**			10	mA
$I_{OH(avg)}$	"H" average current DIG_0 – DIG_{15} **(Note 2)**			–18	mA
$I_{OH(avg)}$	"H" average current OVF_{OUT} **(Note 2)**			–5.0	mA
$I_{OL(avg)}$	"L" average current OVF_{OUT} **(Note 2)**			5.0	mA
CLK	Clock input frequency			2	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current is an average value measured over 100 ms.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	DIG output DIG_0–DIG_{15}	I_{OH} = –18 mA	V_{CC} –2.0			V
V_{OH}	"H" output voltage	OVF_{OUT}	I_{OH} = –10 mA	V_{CC} –2.0			V
V_{OL}	"L" output voltage	OVF_{OUT}	I_{OL} = 10 mA			2.0	V
V_{T+} — V_{T-}	Hysteresis	CLK, OVF_{IN} $\overline{RESET}$	V_{CC} = 5.0 V		0.4		V
I_{IH}	"H" input current	OVF_{IN} $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	CLK, SEL	V_I = V_{CC} V_{CC} = 5.0 V	30	70	140	µA
I_{IL}	"L" input current	OVF_{IN} CLK, SEL	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$	V_I = V_{SS} V_{CC} = 5.0 V	–60	–130	–185	µA
I_{LOAD}	Output load current	DIG_0 – DIG_{15}	V_{EE} = V_{CC} –43 V V_{OL} = V_{CC} Output transistors are off.	500	650	800	µA
I_{LEAK}	Output leakage current	DIG_0–DIG_{15}	V_{EE} = V_{CC} –43 V V_{OL} = V_{CC} –43 V Output transistors are off.			–10	µA
I_{CC}	Power source	V_{CC} = 5.0 V, CLK = 100 kHz Output transistors are off.			50		µA

TIMING REQUIREMENTS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{c(CLK)}$	Clock input cycle time	500			ns
$t_{wH(CLK)}$	Clock input "H" pulse width	200			ns
$t_{wL(CLK)}$	Clock input "L" pulse width	200			ns
$t_{su(SEL)}$	Select input setup time	500			ns
$t_{h(SEL)}$	Select input hold time	500			ns
$t_{h(CLK)}$	Clock input setup time	500			ns

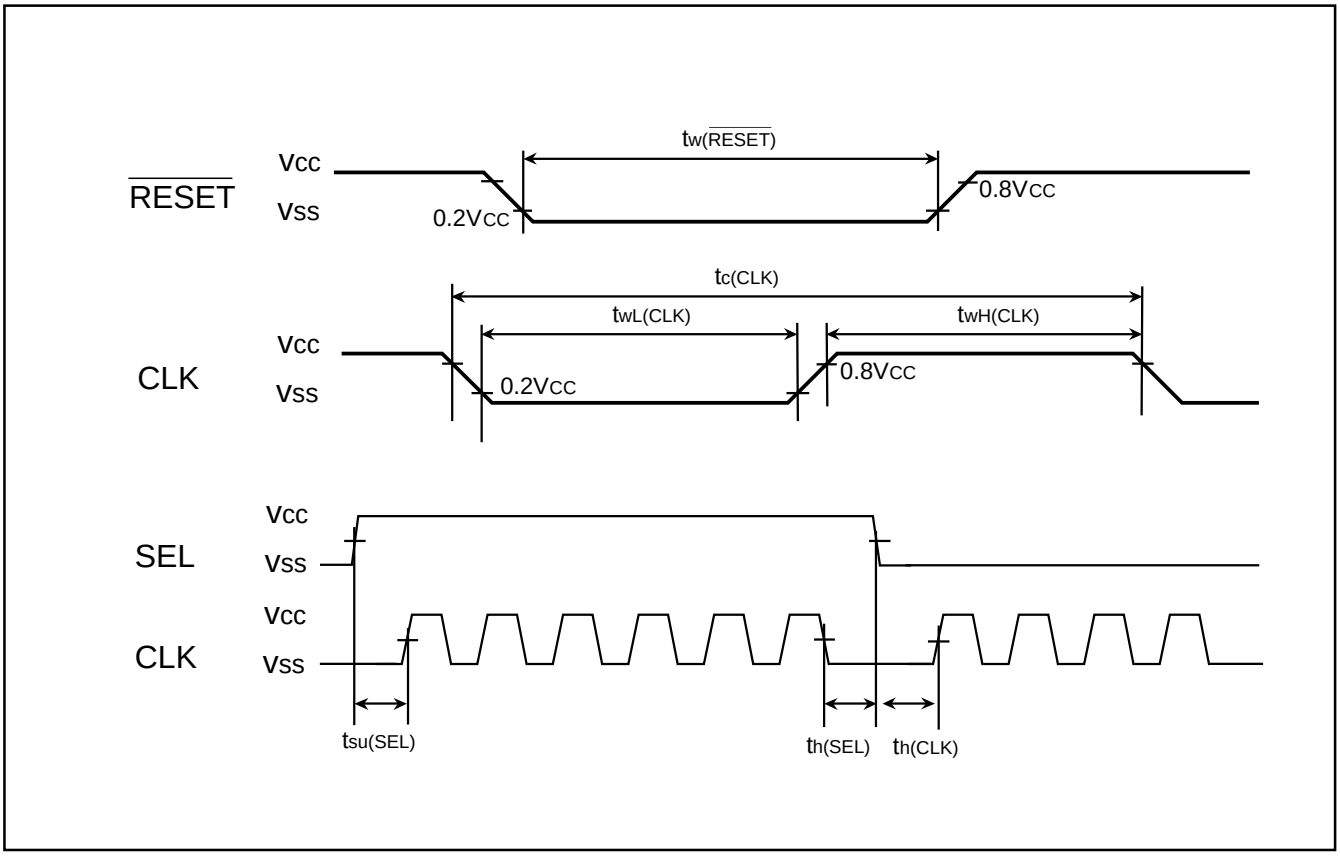


Fig. 13 Timing diagram

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Rev. No.	Revision Description	Rev. date
1.0	First Edition	980216