FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00004-0v01-E

Memory FRAM

CMOS

1 M Bit (64 K × 16)

MB85R1002A

■ DESCRIPTIONS

The MB85R1002A is an FRAM (Ferroelectric Random Access Memory) chip consisting of 65,536 words × 16 bits of nonvolatile memory cells created using ferroelectric process and silicon gate CMOS process technologies.
The MB85R1002A is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85R1002A can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
The MB85R1002A uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

■ FEATURES

- Bit configuration : 65,536 words × 16 bits
- Read/write endurance : 10^{10} times
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : − 40 °C to + 85 °C
- Data retention : 10 years (+ 55 °C)
- $\overline{LB}$ and $\overline{UB}$ data byte control
- Package : 48-pin plastic TSOP (1)

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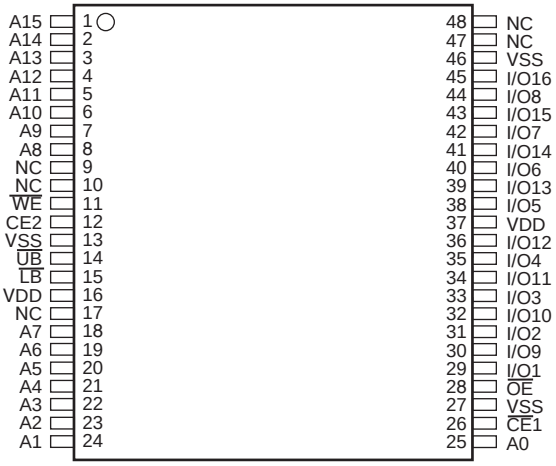
■ PIN ASSIGNMENTS

(TOP VIEW)

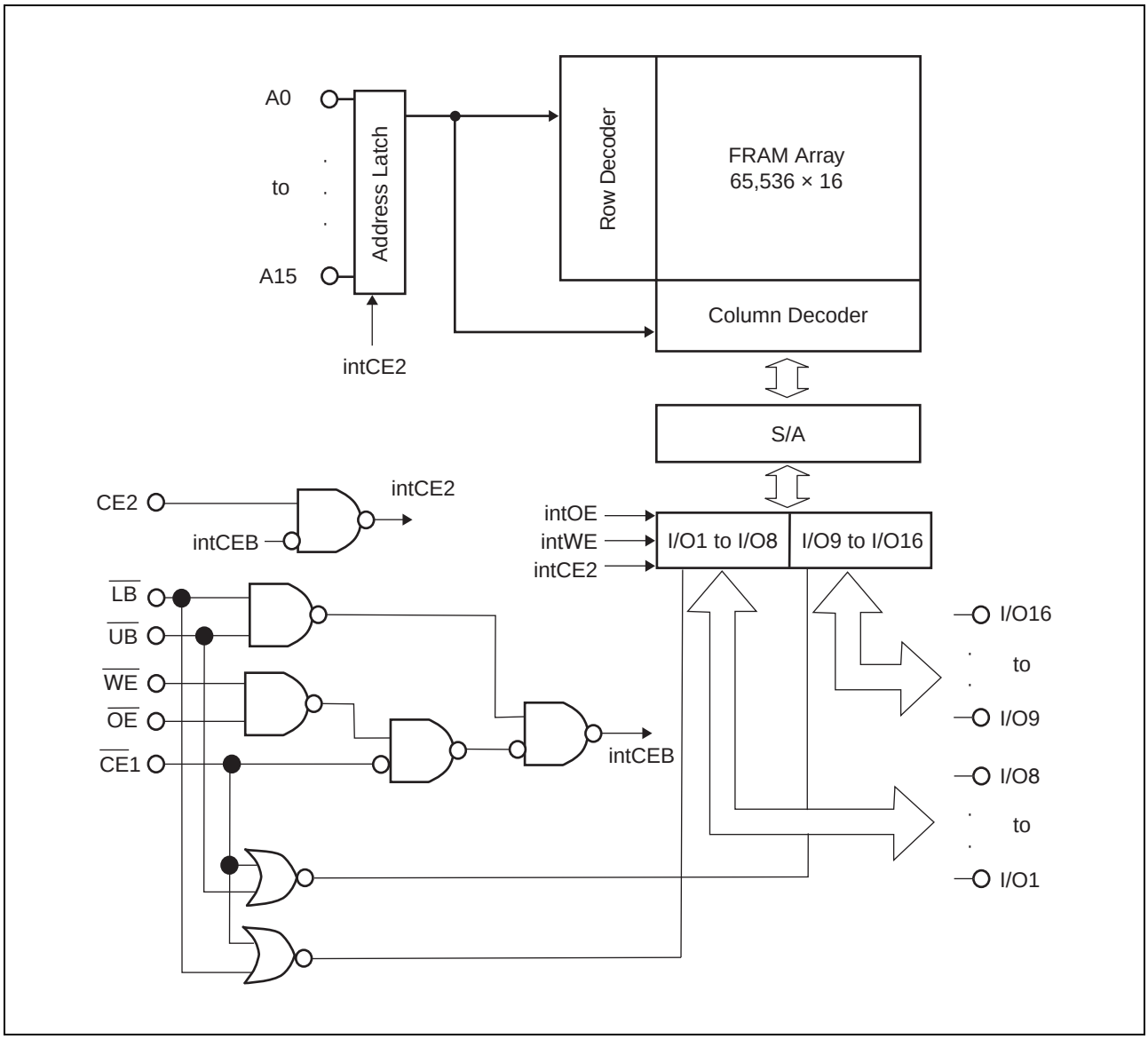


(FPT-48P-M48)

■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 8, 18 to 25	A0 to A15	Address Input pins
29 to 36, 38 to 45	I/O1 to I/O16	Data Input/Output pins
26	$\overline{CE1}$	Chip Enable 1 Input pin
12	CE2	Chip Enable 2 Input pin
11	$\overline{WE}$	Write Enable Input pin
28	$\overline{OE}$	Output Enable Input pin
14, 15	$\overline{LB}$, $\overline{UB}$	Data Byte Control Input pins
16, 37	VDD	Supply Voltage pins
13, 27, 46	VSS	Ground pins
9, 10, 17, 47, 48	NC	No Connect pins

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Mode	$\overline{CE}1$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	Supply Current
Standby Precharge	H	X	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
	X	L	X	X	X	X			
	X	X	H	H	X	X			
	X	X	X	X	H	H			
Read	↓ L	H ↑	H	L	L	L	Data Output	Data Output	Operation (I_{CC})
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Read (Pseudo-SRAM, $\overline{OE}$ control*1)	L	H	H	↓	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Write	↓ L	H ↑	L	X	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	
Write (Pseudo-SRAM, $\overline{WE}$ control*2)	L	H	↓	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	

Note: L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, Hi-Z = High Impedance

↓ : Latch address and latch data at falling edge, ↑ : Latch address and latch data at rising edge

*1 : $\overline{OE}$ control of the Pseudo-SRAM means the valid address at the falling edge of $\overline{OE}$ to read.

*2 : $\overline{WE}$ control of the Pseudo-SRAM means the valid address and data at the falling edge of $\overline{WE}$ to write.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}	—	—	TBD	µA
Output Leakage Current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}, $\overline{CE}1 = V_{IH}$ or $\overline{OE} = V_{IH}$	—	—	TBD	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}1$ = 0.2 V, CE2 = V_{CC} – 0.2 V, I_{out} = 0 mA*1	—	TBD	TBD	mA
Standby Current	I_{SB}	$\overline{CE}1 \geq V_{CC} - 0.2$ V	—	TBD	TBD	µA
		CE2 ≤ 0.2 V*2				
		$\overline{OE} \geq V_{CC} - 0.2$ V, $\overline{WE} \geq V_{CC} - 0.2$ V*2				
		$\overline{LB} \geq V_{CC} - 0.2$ V, $\overline{UB} \geq V_{CC} - 0.2$ V*2				
High Level Output Voltage	V_{OH}	I_{OH} = – 1.0 mA	$V_{CC} \times 0.8$	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.0 mA	—	—	0.4	V

*1 : During the measurement of I_{CC} , the Address, Data In were taken to only change once per active cycle.
Iout : output current

*2 : All pins other than setting pins should be input at the CMOS level voltages such as H ≥ V_{CC} – 0.2 V, L ≤ 0.2 V.

(2) Write Cycle

(within recommended operating conditions)

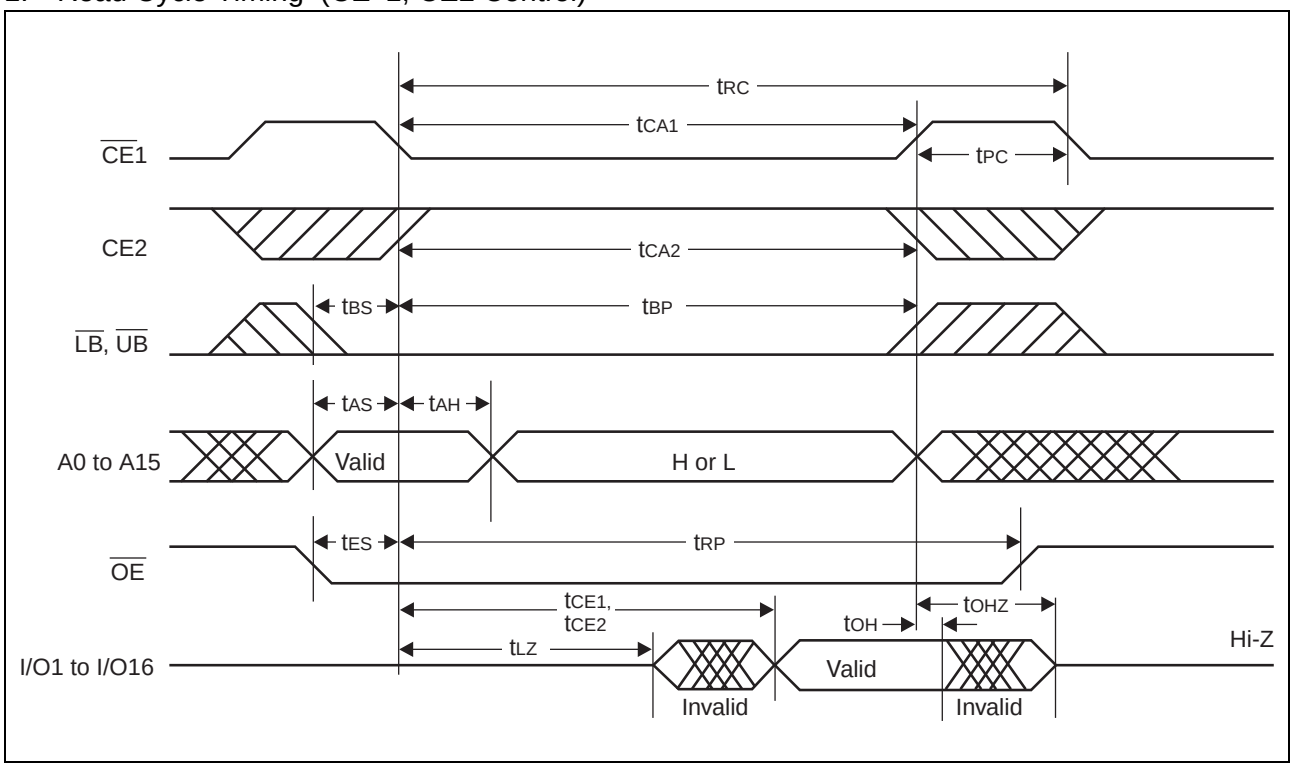
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	150	—	ns
$\overline{CE}$1 Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Precharge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Write Pulse Width	t_{WP}	120	—	ns
Data Setup Time	t_{DS}	0	—	ns
Data Hold Time	t_{DH}	50	—	ns
Write Setup Time	t_{WS}	0	—	ns

3. Pin Capacitance

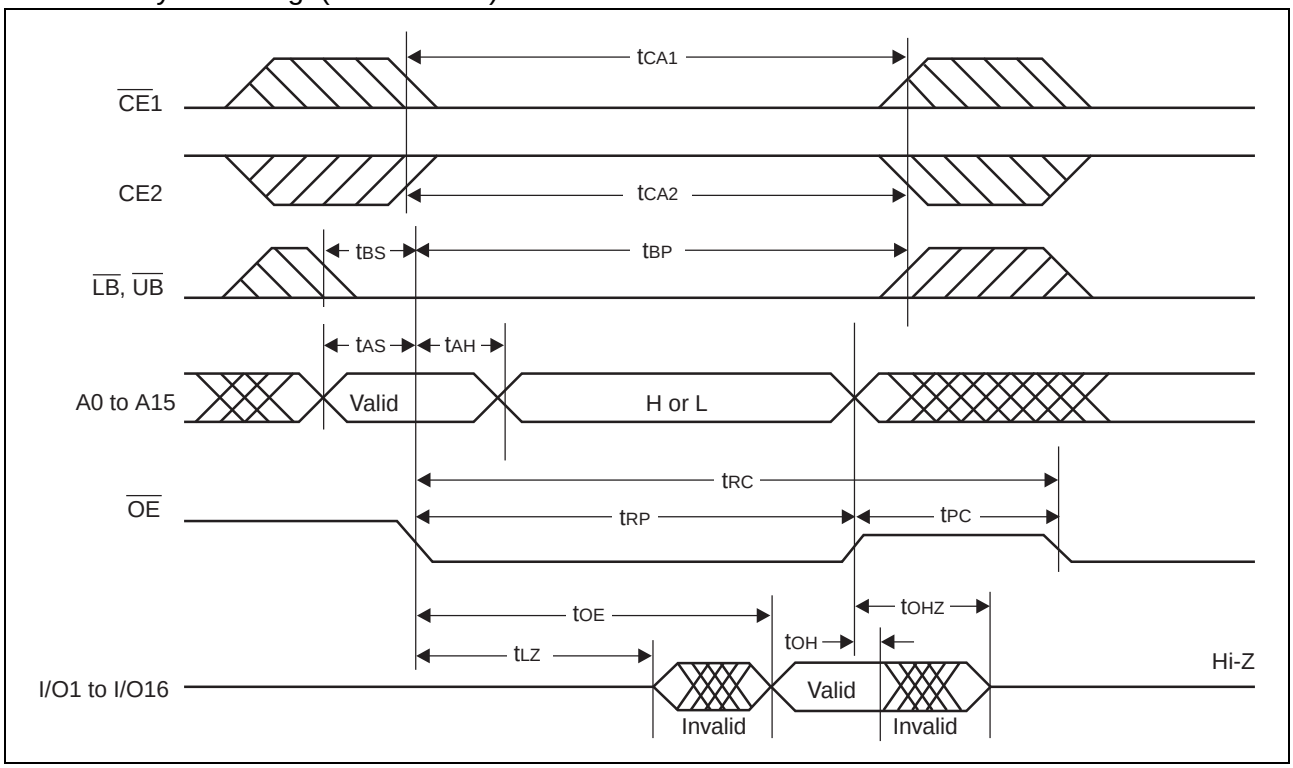
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	—	10	pF
Output Capacitance	C_{OUT}		—	—	10	pF

■ TIMING DIAGRAMS

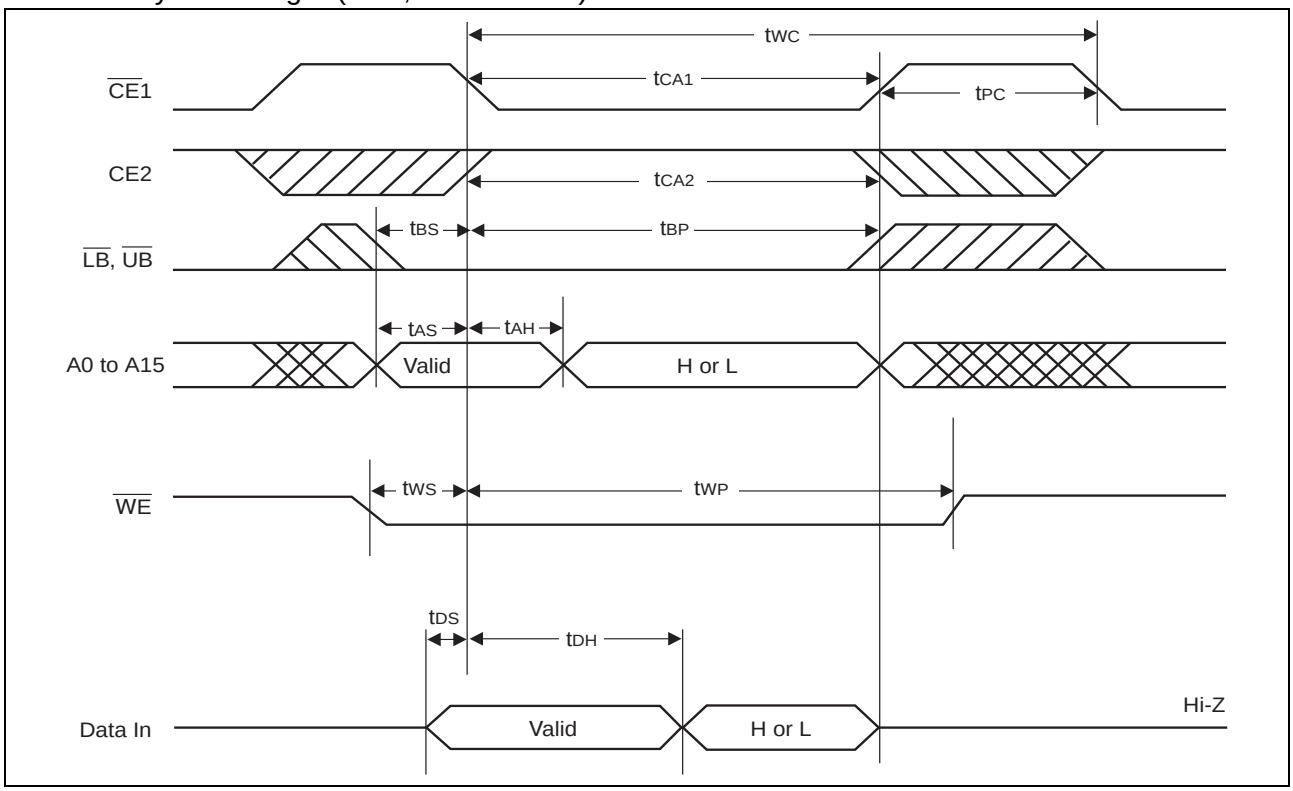
1. Read Cycle Timing ($\overline{CE}$ 1, CE2 Control)



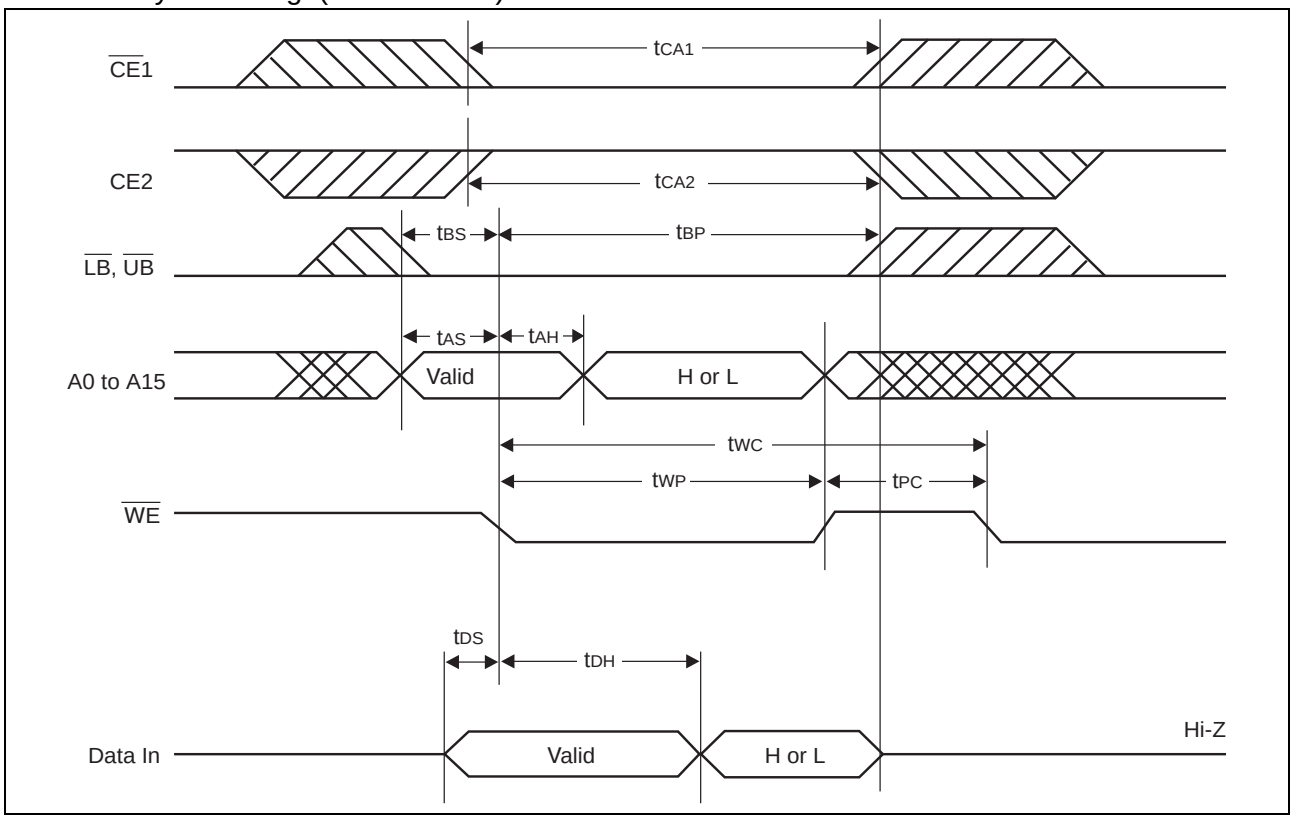
2. Read Cycle Timing ($\overline{OE}$ Control)



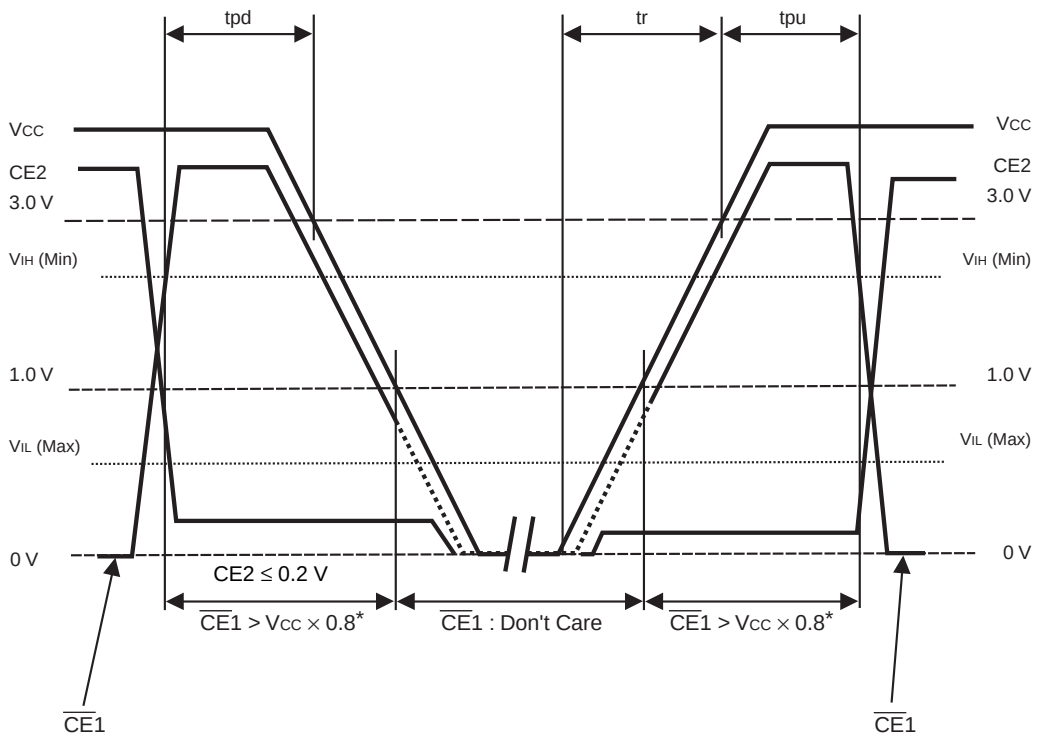
3. Write Cycle Timing ($\overline{CE}$1, CE2 Control)



4. Write Cycle Timing ($\overline{WE}$ Control)



■ POWER ON/OFF SEQUENCE



* : $\overline{CE1}$ (Max) < V_{CC} + 0.5 V

Notes:
- Use either of $\overline{CE1}$ or CE2, or both for disable control of the device.
- Because turning the power on from an intermediate level may cause malfunctions, when the power is turned on, V_{CC} is required to be started from 0 V.
- If the device does not operate within the specified conditions of read cycle, write cycle, power on/off sequence, memory data can not be guaranteed.
- When turning the power on or off, it is recommended that CE2 is connected to ground to prevent unexpected writing.

(within recommended operating conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE1}$ LEVEL hold time for Power OFF	t_{pd}	85	—	—	ns
$\overline{CE1}$ LEVEL hold time for Power ON	t_{pu}	85	—	—	ns
Power supply rising time	t_r	0.05	—	200	ms

■ NOTES ON USE

After the IR reflow completed, it is not guaranteed to save the data written prior to the IR reflow.

MEMO

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