NEC

MICROWAVE TRANSISTOR SERIES

NE463

Dual Gate GaAs MESFET

FEATURES

- VERY HIGH f_{max}
  45GHz
- TWO INDEPENDENT GATES FOR DESIGN FLEXIBILITY
- HIGH ASSOCIATED GAIN
  19dB at 4GHz
  14dB at 8GHz
  13dB at 12GHz
- LOW NOISE FIGURE
  1.5dB at 4GHz
- HIGH GAIN
  20dB at 4GHz
- AVAILABLE IN CASCODE CONFIGURATION FOR USE AS A GAIN BLOCK
- "85" STYLE PACKAGED VERSION AVAILABLE WITH 70 pF CAPACITOR INTERNAL
- SEVERAL UNIQUE OPERATIONAL MODES

DESCRIPTION AND APPLICATIONS

The NE463 is a dual-gate GaAs FET designed for low noise circuits, wide band amplifiers, and a variety of unique signal processing applications to 12 GHz and above.

The NE463 chip employs two independent 1.0μm gates. In the "83" style package, the device is connected in a cascode configuration suitable for use as a gain block. The "85" style package comes in two configurations. The standard "85" style has a 70 pF capacitor connected internally between the source and the second gate (G2). This option is designed for amplifier and AGC applications. The "85M" version does not have the 70 pF capacitor and is well suited for mixer and modulator applications.

PERFORMANCE SPECIFICATIONS (T_a=25°C)

NE PART NUMBER / PACKAGE CODE			NE46300 CHIP			NE46383 83			NE46385 85		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
f_{max}	Maximum Frequency of Oscillation at V_{DS} = 4V, V_{G2S} = 0V, I_{DS} = 20mA	GHz		45			45			45	
MAG	Maximum Available Gain[1] at V_{DS} = 4V, I_{DS} = 30mA,										
	f = 4GHz	dB		20						18	
	f = 8GHz	dB		15						14	
	f = 12GHz	dB		13.5						10	
NF_{opt}	Optimum Noise Figure[2,3] at V_{DS} = 4V, I_{DS} = 10mA, V_{G2S} = 0V,										
	f = 4GHz	dB		1.5						1.7	
	f = 8GHz	dB		2.7						3.0	4.0
	f = 12GHz	dB		3.7						4.1	
G_a	Associated Gain at Optimum Noise Figure[2,3] at V_{DS} = 4V, I_{DS} = 10mA, V_{G2S} = 0V,										
	f = 4GHz	dB		19						17	
	f = 8GHz	dB		14						12	
	f = 12GHz	dB		13						9	

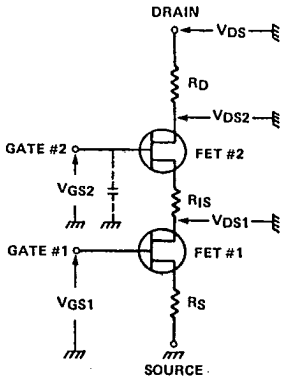
ELECTRICAL CHARACTERISTICS (T_a=25°C)

NE PART NUMBER / PACKAGE CODE			NE46300 CHIP			NE46383 83			NE46385 85		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
I_{DSS}	Drain Current at V_{DS} = 4V, V_{GS} = 0V	mA	30	60	100	30	60	100	30	60	100
V_P	Pinch-off Voltage at V_{DS} = 4V, V_{G2S} = 0V, I_{DS} = 0.1mA	V	−1.5	−3.0		−1.5	−3.0		−1.5	−3.0	
g_m	Transconductance at V_{DS} = 4V, V_{G2S} = 0V, I_{DS} = 20mA	m℧	15	20		15	20		15	20	
R_{th}	Thermal Resistance (ch–a)	°C/W		180[4]						355	

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

SYMBOL	PARAMETERS	UNITS	RATINGS
V_{DS}	Drain to Source Voltage	V	8
V_{G1S}, V_{G2S}	Gate to Source Voltage	V	−8
I_D	Drain Current	mA	100
P_T	Total Power Dissipation	mW	500
T_{ch}	Channel Temperature	°C	175
T_{stg}	Storage Temperature	°C	−65~+175

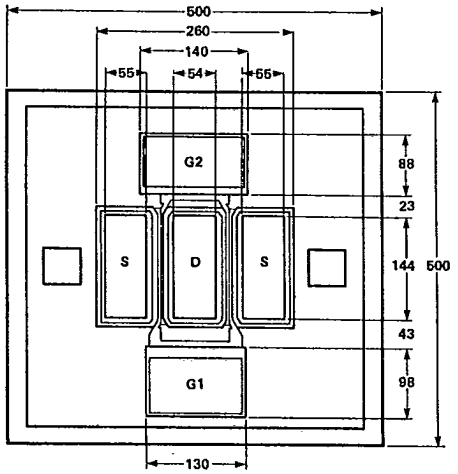
DEVICE CONFIGURATION



NE46385 has a 70 pF capacitor between G2 and Source. NE46385M has no 70 pF capacitor and is meant for mixer, modulator applications.

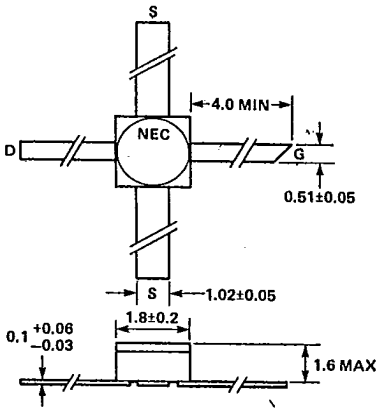
PHYSICAL DIMENSIONS (Units in mm)

NE46300 (Chip) (Units in μm)

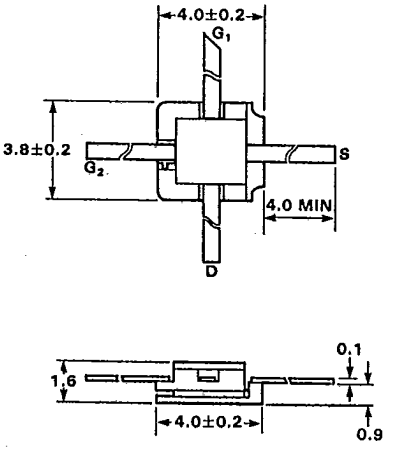


Chip Thickness: 140±10μm

PACKAGE CODE - 83

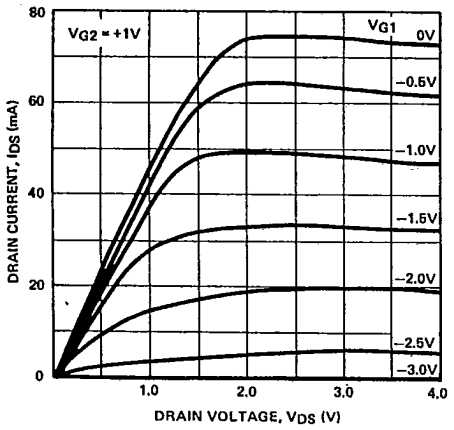


PACKAGE CODE - 85

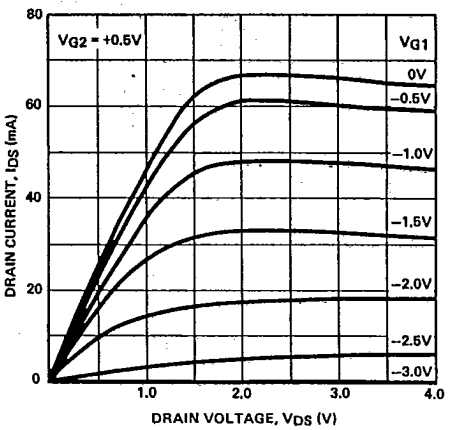


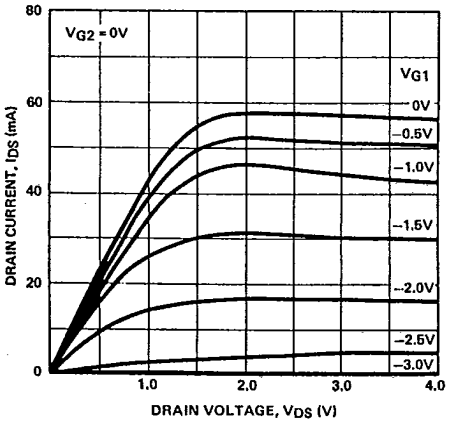
DEVICE CHARACTERISTICS (T_a=25°C)

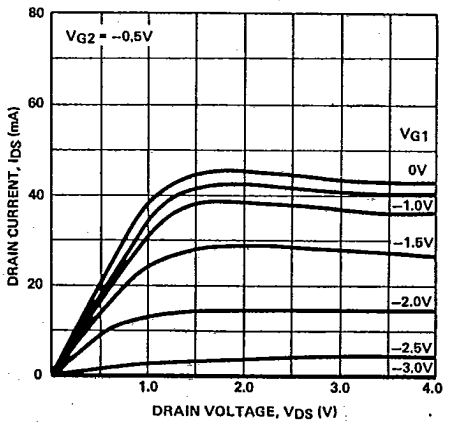
DC PERFORMANCE

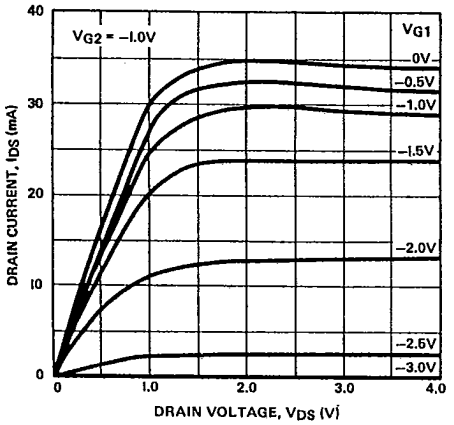


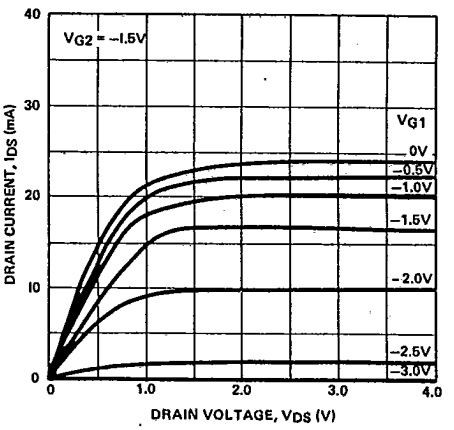
DC PERFORMANCE





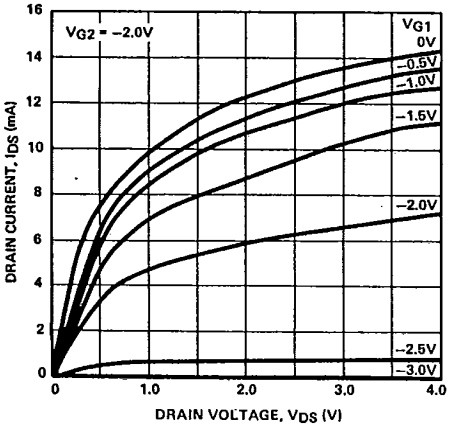




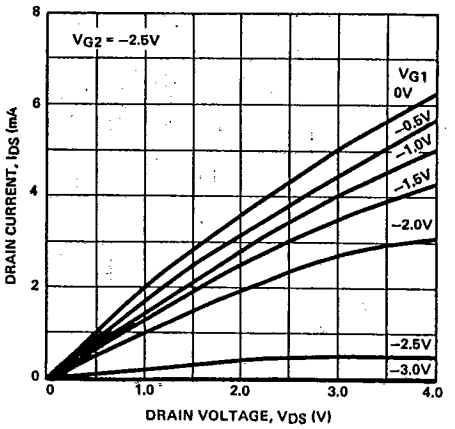


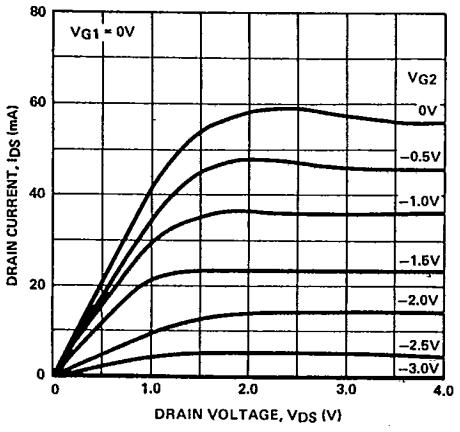
DEVICE CHARACTERISTICS (T_a=25°C) (Cont'd)

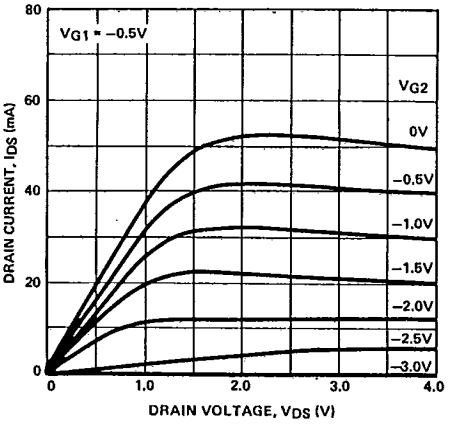
DC PERFORMANCE

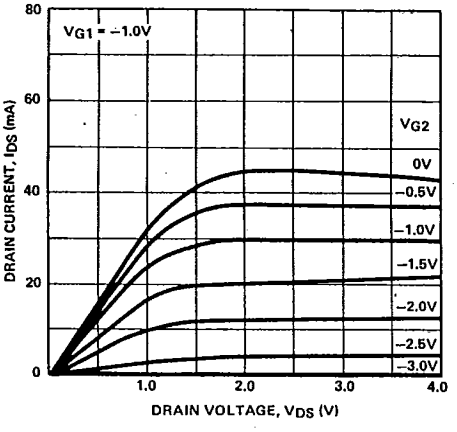


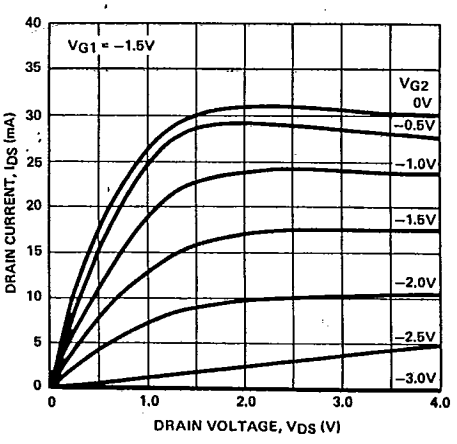
DC PERFORMANCE





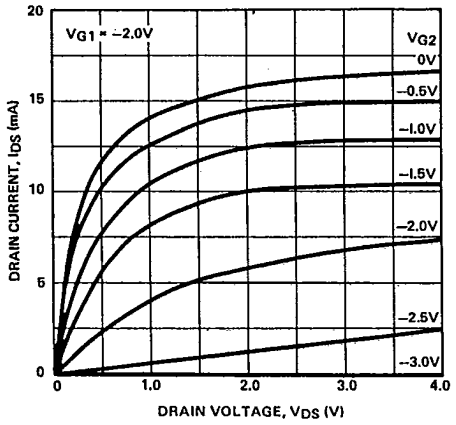




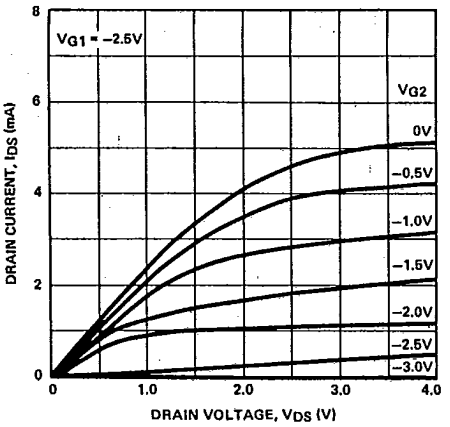


DEVICE CHARACTERISTICS (T_a=25°C) (Cont'd)

DC PERFORMANCE

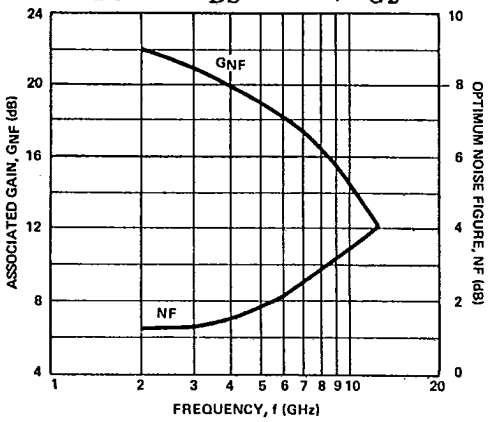


DC PERFORMANCE

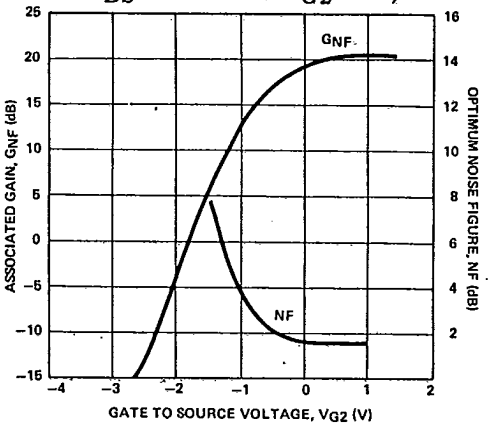


PERFORMANCE CHARACTERISTICS (T_a=25°C)

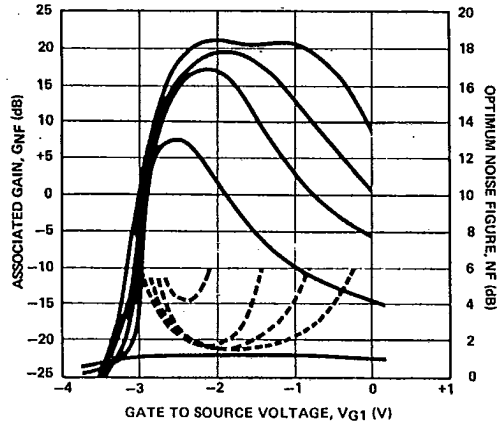
TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. FREQUENCY AT V_{DS} = 4V, I_{DS} = 10mA, V_{G2} = 0V



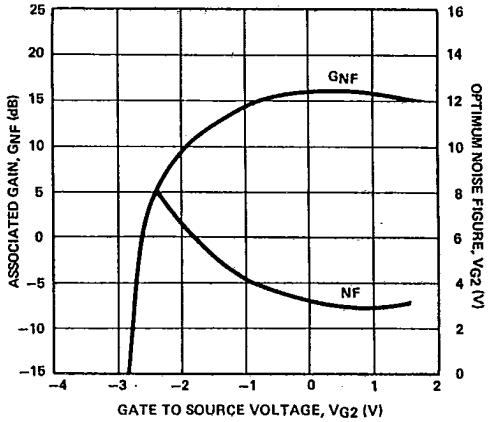
TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. V_{G1} AND V_{G2} AT f = 4GHz, V_{DS} = 4V (Matching point for minimum NF is at I_{DS} = 10mA and V_{G2} = 0V)



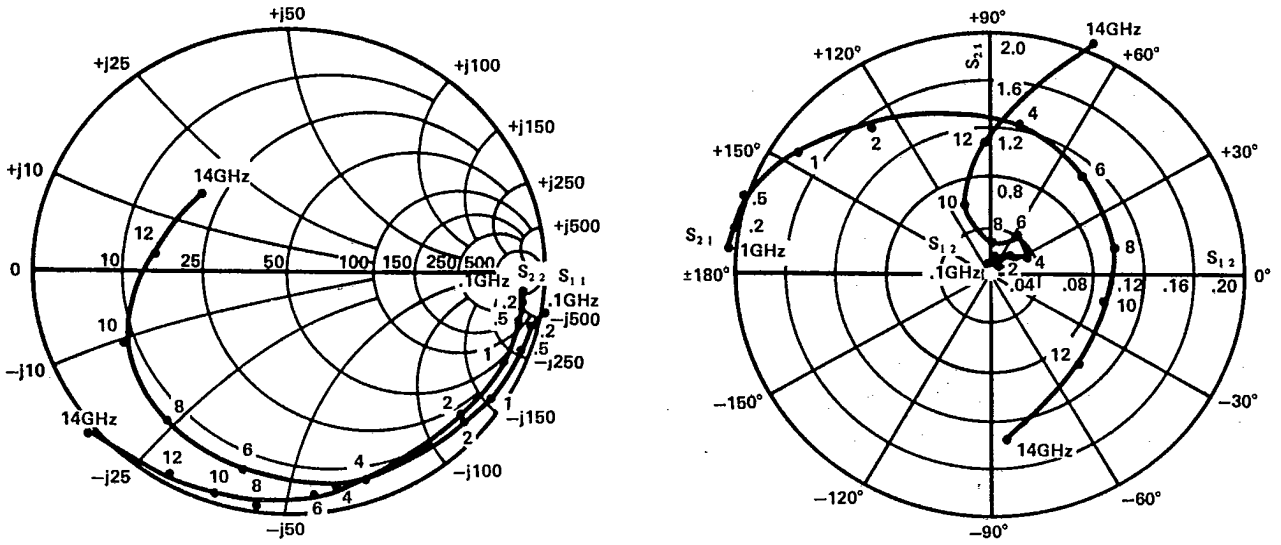
TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. V_{G2} AT f = 4GHz, V_{G1} = −1.6V, V_{DS} = 4V (Matching point for minimum NF is at I_{DS} = 10mA and V_{G2} = 0V)



TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. V_{G2} AT f = 8GHz, V_{G1} = −2.2V, V_{DS} = 4V (Matching point for minimum NF is at I_{DS} = 10mA and V_{G2} = 0V)



NE46385 COMMON SOURCE SCATTERING PARAMETERS



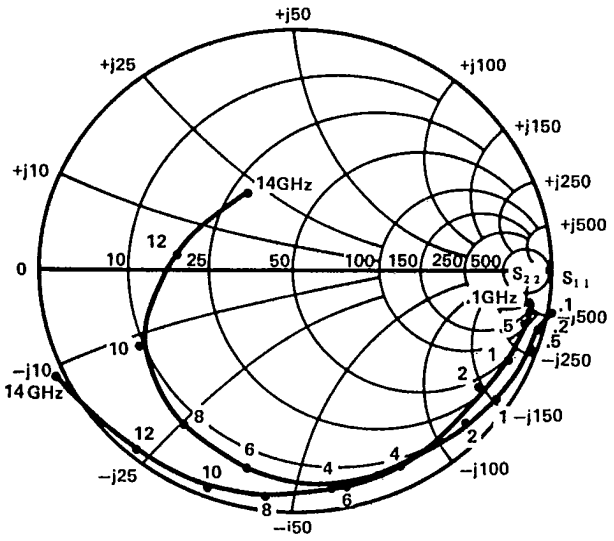
Coordinates in Ohms
Frequency in GHz
(V_{DS} = 4V, I_{DS} = 10mA)
(V_{G1} = −1.46V, V_{G2} = 0V)

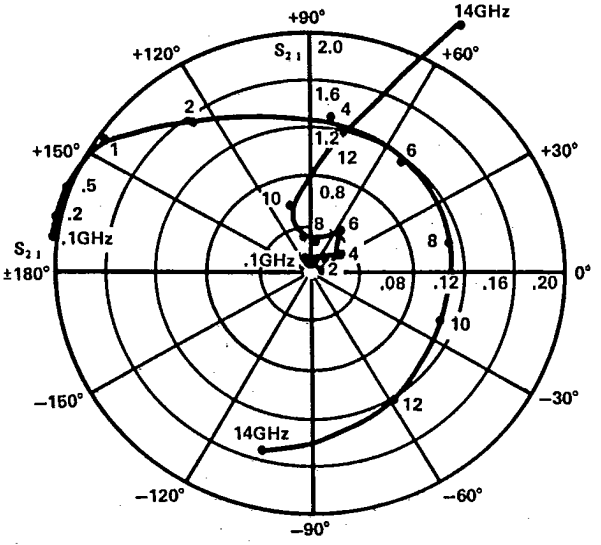
S–MAGN AND ANGLES:

V_{DS} = 4V, I_{DS} = 10mA

FREQUENCY (MHz)	S11		S21		S12		S22	
100	1.01	−8	2.04	174	.01	87	.92	−5
200	.99	−11	2.01	169	.01	67	.93	−7
500	.99	−18	2.01	161	.01	83	.93	−13
1000	.97	−32	1.88	146	.01	63	.93	−24
4000	.92	−77	1.26	79	.04	26	.92	−73
6000	.86	−101	1.09	47	.05	57	.93	−84
8000	.79	−126	1.01	11	.03	86	.99	−98
10000	.72	−154	.93	−14	.06	110	.98	−108
12000	.55	174	1.06	−47	.11	92	.97	−119
14000	.48	139	1.37	−85	.26	67	1.01	−140

NE46385 COMMON SOURCE SCATTERING PARAMETERS





Coordinates in Ohms
Frequency in GHz
(V_{DS} = 4V, I_{DS} = 30mA)
(V_{G1} = –2.25V, V_{G2} = 0V)

S–MAGN AND ANGLES:

V_{DS} = 4V, I_{DS} = 30mA

FREQUENCY (MHz)	S11		S21		S12		S22	
100	1.02	–9	2.09	172	.01	100	.94	–7
200	1.00	–13	2.03	167	.01	11	.94	–9
500	.99	–19	2.03	160	.01	80	.91	–13
1000	.96	–33	1.91	146	.01	60	.92	–23
2000	.94	–43	1.55	127	.03	50	.89	–33
4000	.94	–80	1.31	82	.04	30	.93	–62
6000	.86	–103	1.20	50	.04	58	.91	–77
8000	.79	–125	1.14	11	.03	82	.96	–96
10000	.69	–153	1.11	–19	.06	106	.98	–111
12000	.46	173	1.25	–57	.11	80	.96	–129
14000	.35	119	1.52	–104	.25	61	1.07	–155

NOTES:

1. Gain Calculations: MAG = $\frac{|S_{21}|}{|S_{12}|}(k \pm \sqrt{k^2-1})$, $k = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}||S_{21}|}$, $\Delta = S_{11}S_{22} - S_{21}S_{12}$

2. Typical values of noise figures are those obtained when 50% of the devices from a large number of lots were individually measured in a circuit with the input individually tuned to obtain the minimum value. Maximum values are criteria established on the production line as a "go-no-go" screening tuned for the "generic" type but not for each specimen.

3. RF performance is determined by packaging and testing 10 samples per wafer; wafer rejection criteria for standard devices is 2 rejects for 10 samples.

4. R_{th} (channel to case) for chips mounted on a copper heatsink.