

16 M-BIT DYNAMIC RAM

1 M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μ PD42S16160, 4216160, 42S18160, 4218160 are 1,048, 576 words by 16 bits CMOS dynamic RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the μ PD42S16160, 42S18160 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

Features

- 1,048,576 words by 16 bits organization
- Single +5.0 V ± 10 % power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S16160-50, 4216160-50	605 mW	50 ns	90 ns	35 ns
μ PD42S18160-50, 4218160-50	935 mW			
μ PD42S16160-60, 4216160-60	550 mW	60 ns	110 ns	40 ns
μ PD42S18160-60, 4218160-60	880 mW			
μ PD42S16160-70, 4216160-70	495 mW	70 ns	130 ns	45 ns
μ PD42S18160-70, 4218160-70	825 mW			
μ PD42S16160-80, 4216160-80	440 mW	80 ns	150 ns	50 ns
μ PD42S18160-80, 4218160-80	770 mW			

- The μ PD42S16160, 42S18160 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S16160	4,096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μ PD42S18160	1,024 cycles/128 ms		
μ PD4216160	4,096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μ PD4218160	1,024 cycles/16 ms		

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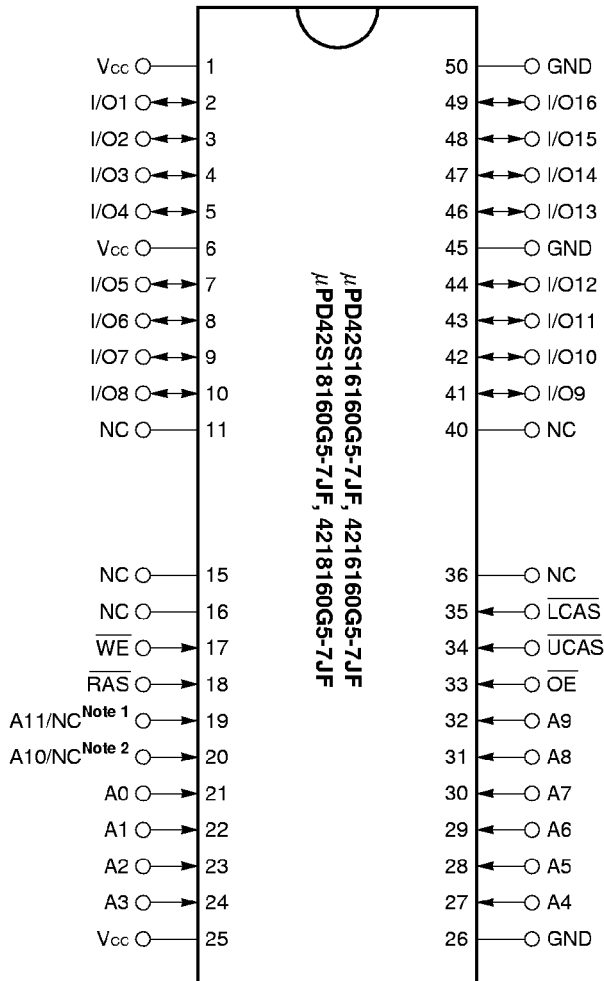
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Ordering Information

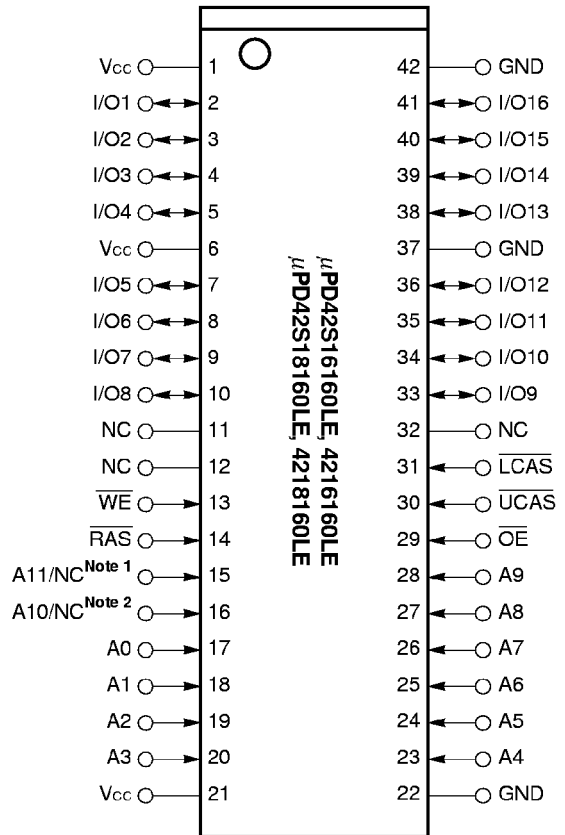
Part number	Access time (MAX.)	Package	Refresh
μPD42S16160G5-50-7JF	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S18160G5-50-7JF			
μPD42S16160G5-60-7JF	60 ns		
μPD42S18160G5-60-7JF			
μPD42S16160G5-70-7JF	70 ns		
μPD42S18160G5-70-7JF			
μPD42S16160G5-80-7JF	80 ns		
μPD42S18160G5-80-7JF			
μPD42S16160LE-50	50 ns	42-pin plastic SOJ (400 mil)	
μPD42S18160LE-50			
μPD42S16160LE-60	60 ns		
μPD42S18160LE-60			
μPD42S16160LE-70	70 ns		
μPD42S18160LE-70			
μPD42S16160LE-80	80 ns		
μPD42S18160LE-80			
μPD4216160G5-50-7JF	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD4218160G5-50-7JF			
μPD4216160G5-60-7JF	60 ns		
μPD4218160G5-60-7JF			
μPD4216160G5-70-7JF	70 ns		
μPD4218160G5-70-7JF			
μPD4216160G5-80-7JF	80 ns		
μPD4218160G5-80-7JF			
μPD4216160LE-50	50 ns	42-pin plastic SOJ (400 mil)	
μPD4218160LE-50			
μPD4216160LE-60	60 ns		
μPD4218160LE-60			
μPD4216160LE-70	70 ns		
μPD4218160LE-70			
μPD4216160LE-80	80 ns		
μPD4218160LE-80			

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II)(400 mil)



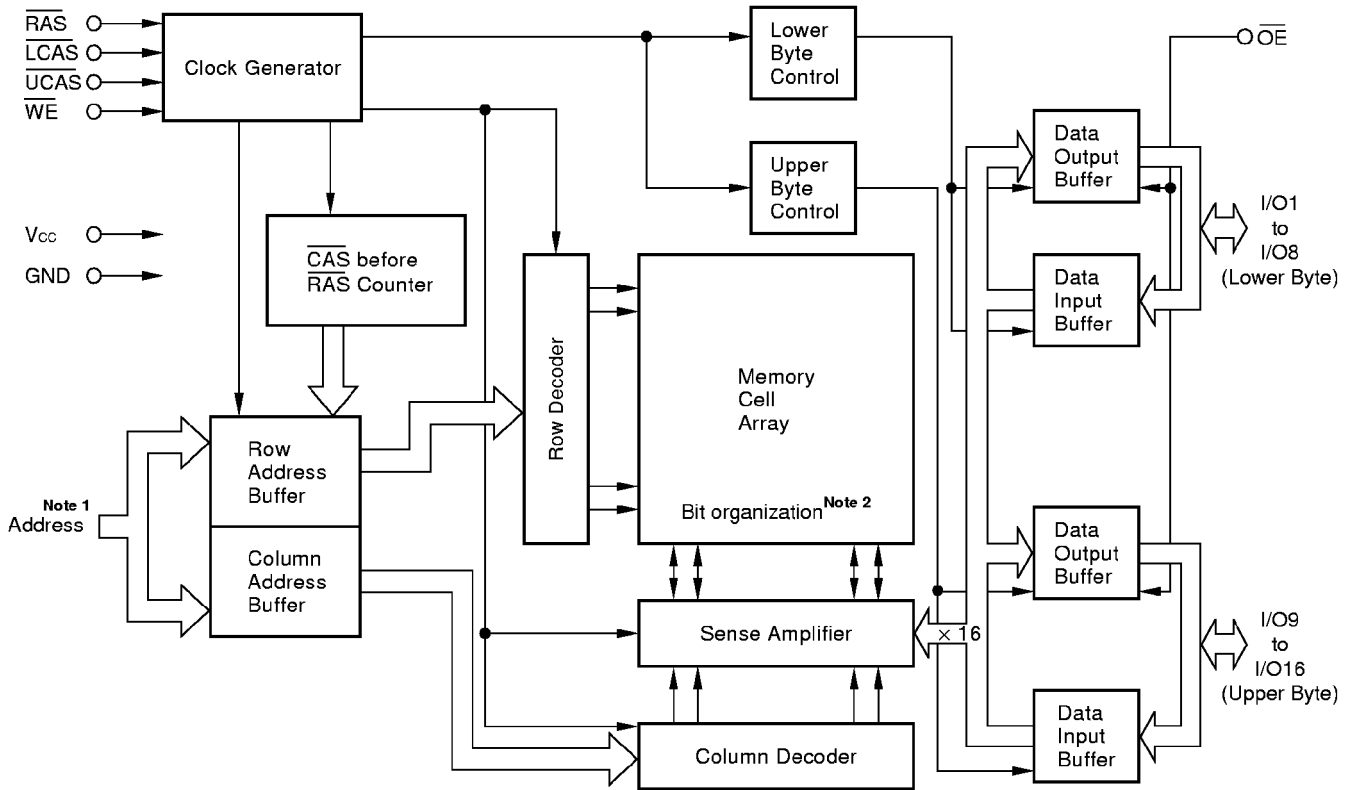
42-pin Plastic SOJ (400 mil)



- Notes** 1. A11 ... μPD42S16160, 4216160 NC ... μPD42S18160, 4218160
 2. A10 ... μPD42S16160, 4216160 NC ... μPD42S18160, 4218160

- A0 to A11 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{UCAS}}$: Column Address Strobe (upper)
- $\overline{\text{LCAS}}$: Column Address Strobe (lower)
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μ PD42S16160, 4216160	A0 - A11	A0 - A7
μ PD42S18160, 4218160	A0 - A9	A0 - A9

2. μ PD42S16160, 4216160 ... $4,096 \times 256 \times 16$ μ PD42S18160, 4218160 ... $1,024 \times 1,024 \times 16$

Input/Output Pin Functions

The μPD42S16160, 4216160, 42S18160, 4218160 have input pins \overline{RAS} , \overline{CAS} ^{Note 1}, \overline{WE} , \overline{OE} , Address^{Note 2} and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
\overline{RAS} (Row address strobe)	Input	\overline{RAS} activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • \overline{CAS} before \overline{RAS} refresh
\overline{CAS} (Column address strobe)	Input	\overline{CAS} activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A _x ^{Note 2} (Address input)	Input	Address bus. Input total 20-bit of address signal, upper bits and lower bits ^{Note 2} in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating \overline{RAS} . Then, switch the address bus to column address and activate \overline{CAS} . Each address is taken into the device when \overline{RAS} and \overline{CAS} are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of \overline{RAS} and \overline{CAS} .
\overline{WE} (Write enable)	Input	Write control signal. Write operation is executed by activating \overline{RAS} , \overline{CAS} and \overline{WE} .
\overline{OE} (Output enable)	Input	Read control signal. Read operation can be executed by activating \overline{RAS} , \overline{CAS} and \overline{OE} . If \overline{WE} is activated during read operation, \overline{OE} is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data input/output)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Notes 1. \overline{CAS} means \overline{UCAS} and \overline{LCAS} .

2.

Part number	Address inputs	Upper bits	Lower bits
μPD42S16160, 4216160	A0 - A11	12 bits	8 bits
μPD42S18160, 4218160	A0 - A9	10 bits	10 bits

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ inactive) and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[μ PD42S16160, 4216160]

Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes			
Operating current		I _{CC1}	\overline{RAS} , \overline{CAS} cycling $t_{RC} = t_{RC(MIN)}$ $I_o = 0$ mA	$t_{RAC} = 50$ ns	110	mA	1, 2, 3			
				$t_{RAC} = 60$ ns	100					
				$t_{RAC} = 70$ ns	90					
				$t_{RAC} = 80$ ns	80					
Standby current	μ PD42S16160	I _{CC2}	\overline{RAS} , $\overline{CAS} \geq V_{IH(MIN)}$, $I_o = 0$ mA \overline{RAS} , $\overline{CAS} \geq V_{CC} - 0.2$ V, $I_o = 0$ mA		2.0	mA				
	μ PD4216160			\overline{RAS} , $\overline{CAS} \geq V_{IH(MIN)}$, $I_o = 0$ mA \overline{RAS} , $\overline{CAS} \geq V_{CC} - 0.2$ V, $I_o = 0$ mA				2.0 1.0		
	\overline{RAS} only refresh current		I _{CC3}	\overline{RAS} cycling, $\overline{CAS} \geq V_{IH(MIN)}$ $t_{RC} = t_{RC(MIN)}$, $I_o = 0$ mA	$t_{RAC} = 50$ ns			110	mA	1, 2, 3, 4
					$t_{RAC} = 60$ ns			100		
$t_{RAC} = 70$ ns					90					
$t_{RAC} = 80$ ns					80					
Operating current (Fast page mode)		I _{CC4}	$\overline{RAS} \leq V_{IL(MAX)}$, \overline{CAS} cycling $t_{PC} = t_{PC(MIN)}$, $I_o = 0$ mA	$t_{RAC} = 50$ ns	100	mA	1, 2, 5			
				$t_{RAC} = 60$ ns	90					
				$t_{RAC} = 70$ ns	80					
				$t_{RAC} = 80$ ns	70					
\overline{CAS} before \overline{RAS} refresh current		I _{CC5}	\overline{RAS} cycling $t_{RC} = t_{RC(MIN)}$ $I_o = 0$ mA	$t_{RAC} = 50$ ns	110	mA	1, 2			
				$t_{RAC} = 60$ ns	100					
				$t_{RAC} = 70$ ns	90					
				$t_{RAC} = 80$ ns	80					
\overline{CAS} before \overline{RAS} long refresh current (4,096 cycles / 128 ms, only for the μ PD42S16160)		I _{CC6}	\overline{CAS} before \overline{RAS} refresh: $t_{RC} = 31.3$ μ s \overline{RAS} , \overline{CAS} : $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX)}$ 0 V $\leq V_{IL} \leq 0.2$ V Standby: \overline{RAS} , $\overline{CAS} \geq V_{CC} - 0.2$ V Address: V_{IH} or V_{IL} \overline{WE} , \overline{OE} : V_{IH} $I_o = 0$ mA	$t_{RAS} \leq 300$ ns	450	μ A	1, 2			
				$t_{RAS} \leq 1$ μ s	600					
Self refresh current (\overline{CAS} before \overline{RAS} self refresh, only for the μ PD42S16160)		I _{CC7}	\overline{RAS} , \overline{CAS} : $t_{RASS} = 5$ ms $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX)}$ 0 V $\leq V_{IL} \leq 0.2$ V $I_o = 0$ mA		250	μ A	2			
Input leakage current		I _{I(L)}	$V_I = 0$ to 5.5 V All other pins not under test = 0 V	-10	+10	μ A				
Output leakage current		I _{O(L)}	$V_O = 0$ to 5.5 V Output is disabled (Hi-Z)	-10	+10	μ A				
High level output voltage		V _{OH}	$I_o = -2.5$ mA	2.4		V				
Low level output voltage		V _{OL}	$I_o = +2.1$ mA		0.4	V				

[μPD42S18160, 4218160]

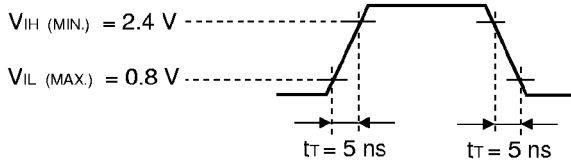
Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{RAS}, \overline{CAS}$ cycling $t_{RC} = t_{RC(MIN)}$ $I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$	170	mA	1, 2, 3
				$t_{RAC} = 60 \text{ ns}$	160		
				$t_{RAC} = 70 \text{ ns}$	150		
				$t_{RAC} = 80 \text{ ns}$	140		
Standby current	μPD42S18160	I _{CC2}	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN)}$, $I_o = 0 \text{ mA}$ $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$, $I_o = 0 \text{ mA}$ $\overline{RAS}, \overline{CAS} \geq V_{IH(MIN)}$, $I_o = 0 \text{ mA}$ $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$, $I_o = 0 \text{ mA}$		2.0	mA	
				0.25			
	μPD4218160			2.0			
				1.0			
RAS only refresh current		I _{CC3}	\overline{RAS} cycling, $\overline{CAS} \geq V_{IH(MIN)}$ $t_{RC} = t_{RC(MIN)}$, $I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$	170	mA	1, 2, 3, 4
				$t_{RAC} = 60 \text{ ns}$	160		
				$t_{RAC} = 70 \text{ ns}$	150		
				$t_{RAC} = 80 \text{ ns}$	140		
Operating current (Fast page mode)		I _{CC4}	$\overline{RAS} \leq V_{IL(MAX)}$, \overline{CAS} cycling $t_{PC} = t_{PC(MIN)}$, $I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$	100	mA	1, 2, 5
				$t_{RAC} = 60 \text{ ns}$	90		
				$t_{RAC} = 70 \text{ ns}$	80		
				$t_{RAC} = 80 \text{ ns}$	70		
CAS before RAS refresh current		I _{CC5}	\overline{RAS} cycling $t_{RC} = t_{RC(MIN)}$ $I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$	170	mA	1, 2
				$t_{RAC} = 60 \text{ ns}$	160		
				$t_{RAC} = 70 \text{ ns}$	150		
				$t_{RAC} = 80 \text{ ns}$	140		
CAS before RAS long refresh current (1,024 cycles / 128 ms, only for the μPD42S18160)		I _{CC6}	\overline{CAS} before \overline{RAS} refresh: $t_{RC} = 125.0 \mu\text{s}$ $\overline{RAS}, \overline{CAS}$: $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ Standby: $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Address: V_{IH} or V_{IL} $\overline{WE}, \overline{OE}$: V_{IH} $I_o = 0 \text{ mA}$	$t_{RAS} \leq 300 \text{ ns}$	350	μA	1, 2
				$t_{RAS} \leq 1 \mu\text{s}$	400	μA	1, 2
Self refresh current (CAS before RAS self refresh, only for the μPD42S18160)		I _{CC7}	$\overline{RAS}, \overline{CAS}$: $t_{RASS} = 5 \text{ ms}$ $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$		250	μA	2
Input leakage current		I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current		I _{O(L)}	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage		V _{OH}	$I_o = -2.5 \text{ mA}$	2.4		V	
Low level output voltage		V _{OL}	$I_o = +2.1 \text{ mA}$		0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX)}$ and $\overline{CAS} \geq V_{IH(MIN)}$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

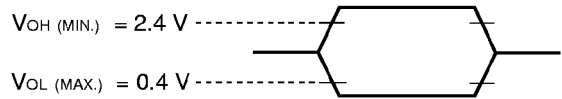
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

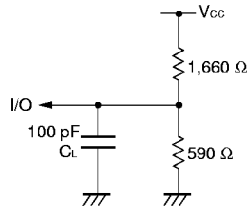
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	$t_{RAC} = 50 ns$		$t_{RAC} = 60 ns$		$t_{RAC} = 70 ns$		$t_{RAC} = 80 ns$		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read / Write cycle time	t_{RC}	90	—	110	—	130	—	150	—	ns		
\overline{RAS} precharge time	t_{RP}	30	—	40	—	50	—	60	—	ns		
\overline{CAS} precharge time	t_{CPN}	8	—	10	—	10	—	10	—	ns		
\overline{RAS} pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	1	
\overline{CAS} pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns		
\overline{RAS} hold time	t_{RSH}	13	—	15	—	18	—	20	—	ns		
\overline{CAS} hold time	t_{CSH}	50	—	60	—	70	—	80	—	ns		
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	18	35	20	45	20	50	25	60	ns	2	
\overline{RAS} to column address delay time	t_{RAD}	13	25	15	30	15	35	17	40	ns	2	
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5	—	5	—	5	—	5	—	ns	3	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns		
Row address hold time	t_{RAH}	8	—	10	—	10	—	12	—	ns		
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns		
Column address hold time	t_{CAH}	13	—	15	—	15	—	15	—	ns		
\overline{OE} lead time referenced to \overline{RAS}	t_{OES}	0	—	0	—	0	—	0	—	ns		
\overline{CAS} to data setup time	t_{CLZ}	0	—	0	—	0	—	0	—	ns		
\overline{OE} to data setup time	t_{OLZ}	0	—	0	—	0	—	0	—	ns		
\overline{OE} to data delay time	t_{OED}	10	—	13	—	15	—	15	—	ns		
Masked byte write hold time referenced to \overline{RAS}	t_{MRH}	0	—	0	—	0	—	0	—	ns		
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns		
Refresh time	μPD42S16160, 42S18160	t_{REF}	—	128	—	128	—	128	—	128	ms	4
	μPD4216160		—	64	—	64	—	64	—	64	ms	
	μPD4218160		—	16	—	16	—	16	—	16	ms	

- ★ **Notes 1.** In $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, $t_{\text{RAS(MAX.)}}$ is 100 μs.
If $10 \mu\text{s} < t_{\text{RAS}} < 100 \mu\text{s}$, $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied.
- 2.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{RAC (MAX.)}}$	$t_{\text{RAC (MAX.)}}$
$t_{\text{RAD}} > t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{AA (MAX.)}}$	$t_{\text{RAD}} + t_{\text{AA (MAX.)}}$
$t_{\text{RCD}} > t_{\text{RCD (MAX.)}}$	$t_{\text{CAC (MAX.)}}$	$t_{\text{RCD}} + t_{\text{CAC (MAX.)}}$

$t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD (MAX.)}}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \geq t_{\text{RCD (MAX.)}}$ will not cause any operation problems.

- 3.** $t_{\text{CRP (MIN.)}}$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
- 4.** This specification is applied only to the μPD42S16160, 42S18160.

Read Cycle

Parameter	Symbol	$t_{\text{RAC}} = 50 \text{ ns}$		$t_{\text{RAC}} = 60 \text{ ns}$		$t_{\text{RAC}} = 70 \text{ ns}$		$t_{\text{RAC}} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	t_{RAC}	–	50	–	60	–	70	–	80	ns	1
Access time from $\overline{\text{CAS}}$	t_{CAC}	–	15	–	15	–	20	–	20	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	–	40	ns	1
Access time from $\overline{\text{OE}}$	t_{OEA}	–	15	–	15	–	20	–	20	ns	
Column address lead time referenced to $\overline{\text{RAS}}$	t_{RAL}	25	–	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{\text{OE}}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	3
Output buffer turn-off delay time from $\overline{\text{CAS}}$	t_{OFF}	0	10	0	13	0	15	0	15	ns	3

- Notes 1.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{RAC (MAX.)}}$	$t_{\text{RAC (MAX.)}}$
$t_{\text{RAD}} > t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \leq t_{\text{RCD (MAX.)}}$	$t_{\text{AA (MAX.)}}$	$t_{\text{RAD}} + t_{\text{AA (MAX.)}}$
$t_{\text{RCD}} > t_{\text{RCD (MAX.)}}$	$t_{\text{CAC (MAX.)}}$	$t_{\text{RCD}} + t_{\text{CAC (MAX.)}}$

$t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD (MAX.)}}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD (MAX.)}}$ and $t_{\text{RCD}} \geq t_{\text{RCD (MAX.)}}$ will not cause any operation problems.

- 2.** Either $t_{\text{RCH (MIN.)}}$ or $t_{\text{RRH (MIN.)}}$ should be met in read cycles.
- 3.** $t_{\text{OFF (MAX.)}}$ and $t_{\text{OEZ (MAX.)}}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
\overline{WE} hold time referenced to \overline{CAS}	t _{WCH}	8	–	10	–	10	–	15	–	ns	1
\overline{WE} pulse width	t _{WP}	8	–	10	–	10	–	15	–	ns	1
\overline{WE} lead time referenced to \overline{RAS}	t _{RWL}	18	–	20	–	20	–	20	–	ns	
\overline{WE} lead time referenced to \overline{CAS}	t _{CWL}	13	–	15	–	15	–	15	–	ns	
\overline{WE} setup time	t _{WCS}	0	–	0	–	0	–	0	–	ns	2
\overline{OE} hold time	t _{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in setup time	t _{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	t _{DH}	10	–	10	–	15	–	15	–	ns	3

- Notes**
1. t_{WP (MIN.)} is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH (MIN.)} should be met.
 2. If t_{WCS} ≥ t_{WCS (MIN.)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS (MIN.)} and t_{DH (MIN.)} are referenced to the \overline{CAS} falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the \overline{WE} falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t _{RWC}	133	–	158	–	180	–	200	–	ns	
\overline{RAS} to \overline{WE} delay time	t _{RWD}	70	–	83	–	95	–	105	–	ns	1
\overline{CAS} to \overline{WE} delay time	t _{CWD}	33	–	38	–	40	–	45	–	ns	1
Column address to \overline{WE} delay time	t _{AWD}	45	–	53	–	60	–	65	–	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS (MIN.)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD (MIN.)}, t_{CWD} ≥ t_{CWD (MIN.)}, t_{AWD} ≥ t_{AWD (MIN.)} and t_{CPWD} ≥ t_{CPWD (MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.



Fast Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t _{PC}	35	–	40	–	45	–	50	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{\text{RAS}}$ pulse width	t _{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	30	–	35	–	40	–	45	–	ns	
Read modify write cycle time	t _{PRWC}	73	–	83	–	90	–	95	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t _{CPWD}	50	–	58	–	65	–	70	–	ns	1

★
★

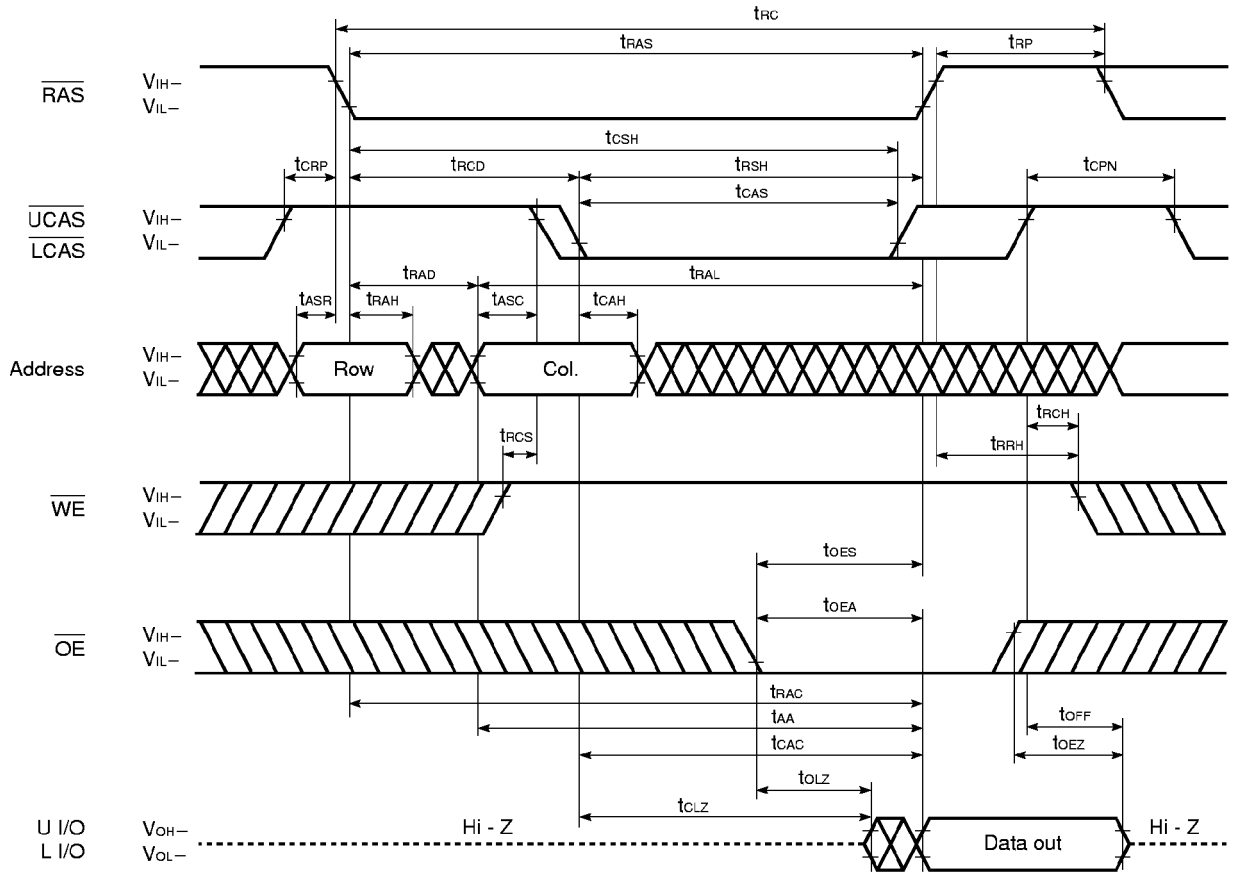
Note 1. If $t_{\text{WCS}} \geq t_{\text{WCS (MIN.)}}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD (MIN.)}}$, $t_{\text{CWD}} \geq t_{\text{CWD (MIN.)}}$, $t_{\text{AWD}} \geq t_{\text{AWD (MIN.)}}$ and $t_{\text{CPWD}} \geq t_{\text{CPWD (MIN.)}}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

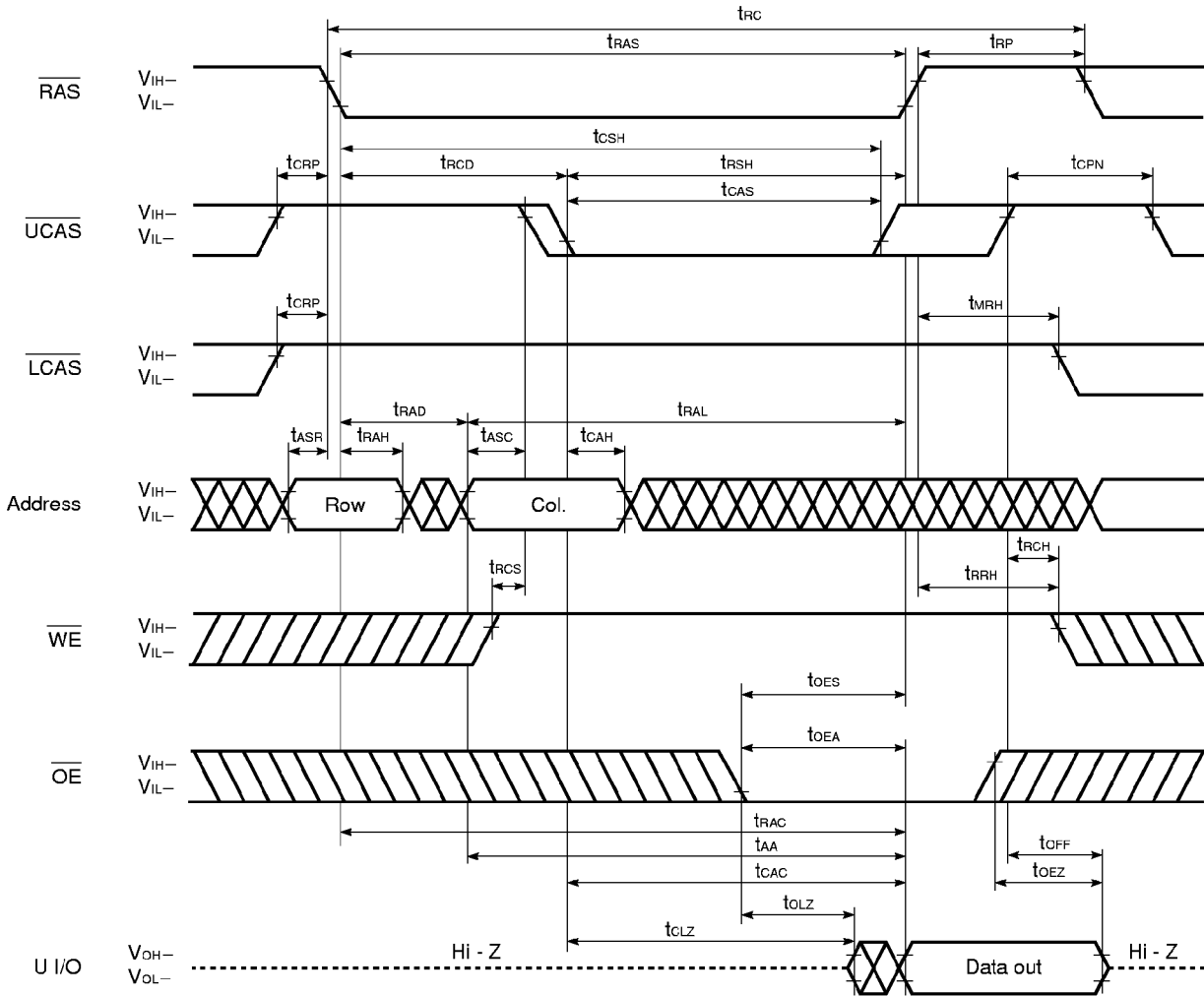
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	t _{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t _{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t _{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RASS}	100	–	100	–	100	–	100	–	μs	1
$\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RPS}	90	–	110	–	130	–	150	–	ns	1
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{CHS}	–50	–	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ hold time	t _{WHR}	15	–	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16160, 42S18160.

Read Cycle

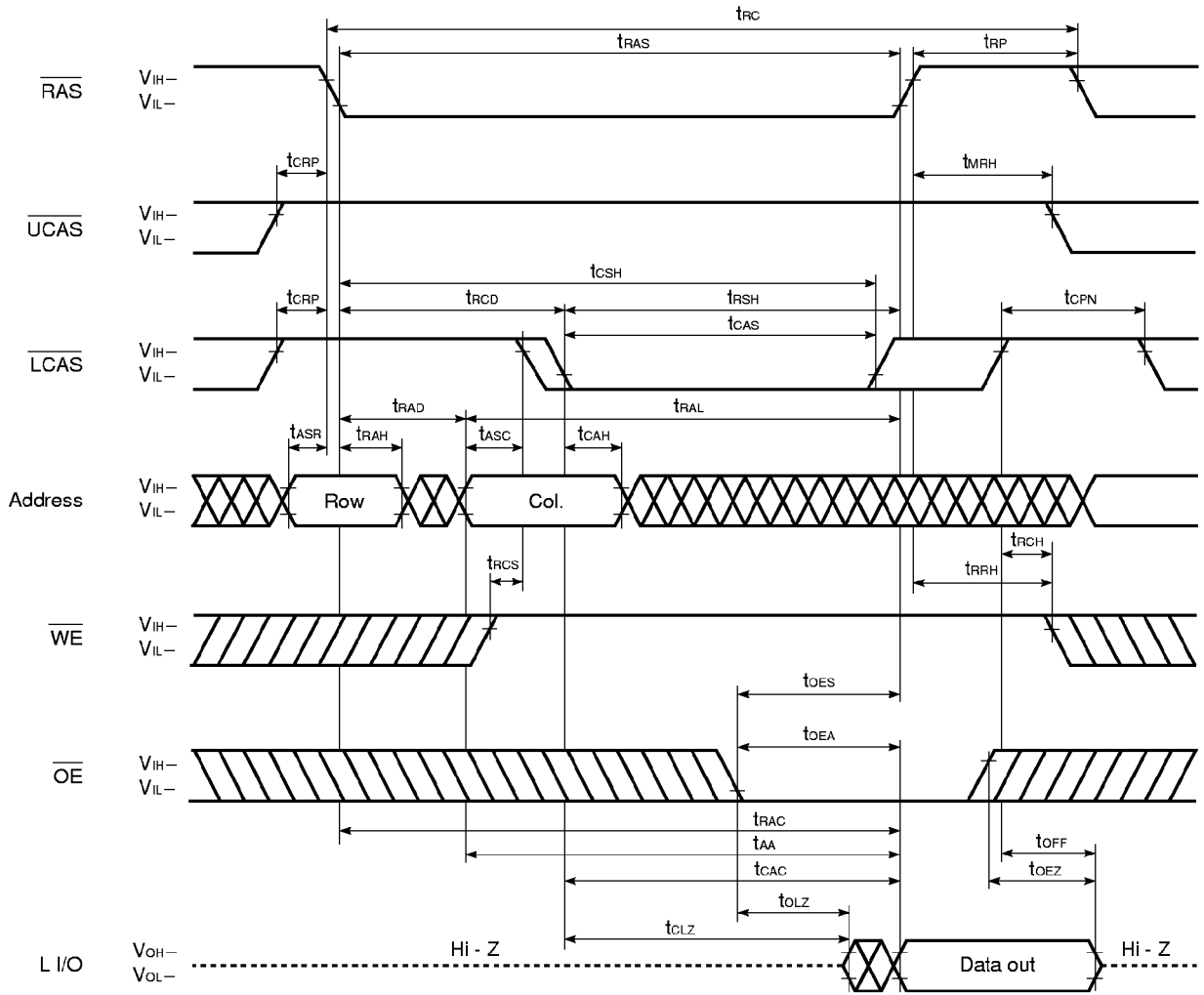


Upper Byte Read Cycle



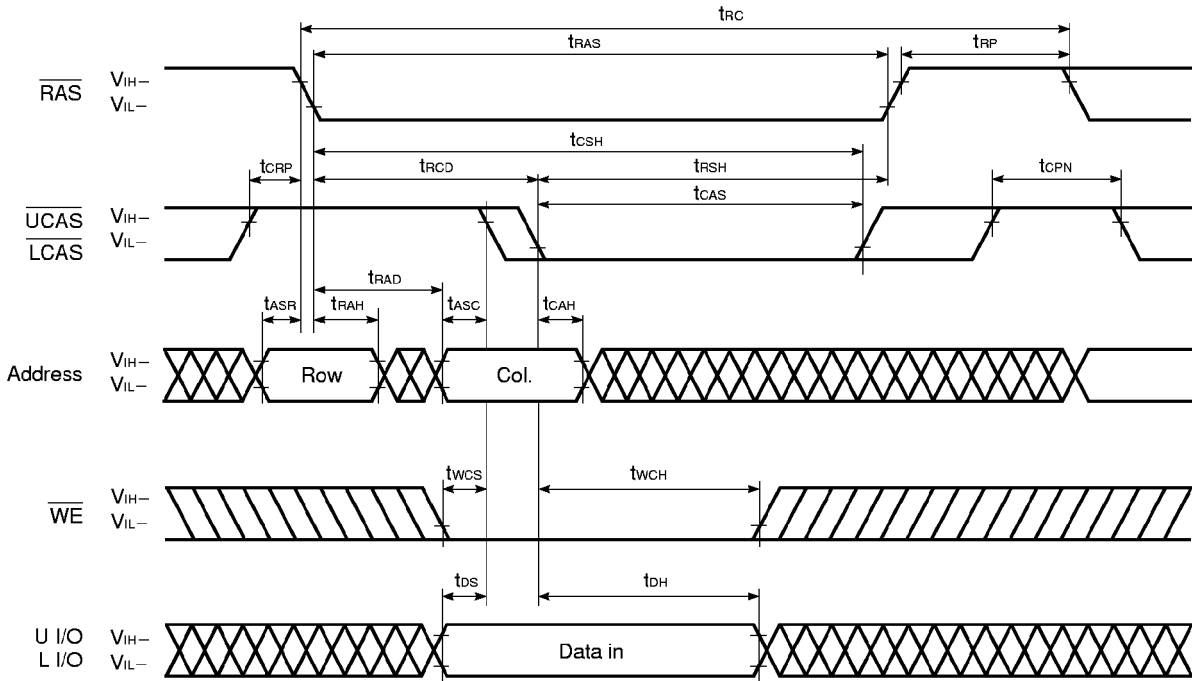
Remark L I/O: Hi-Z

Lower Byte Read Cycle



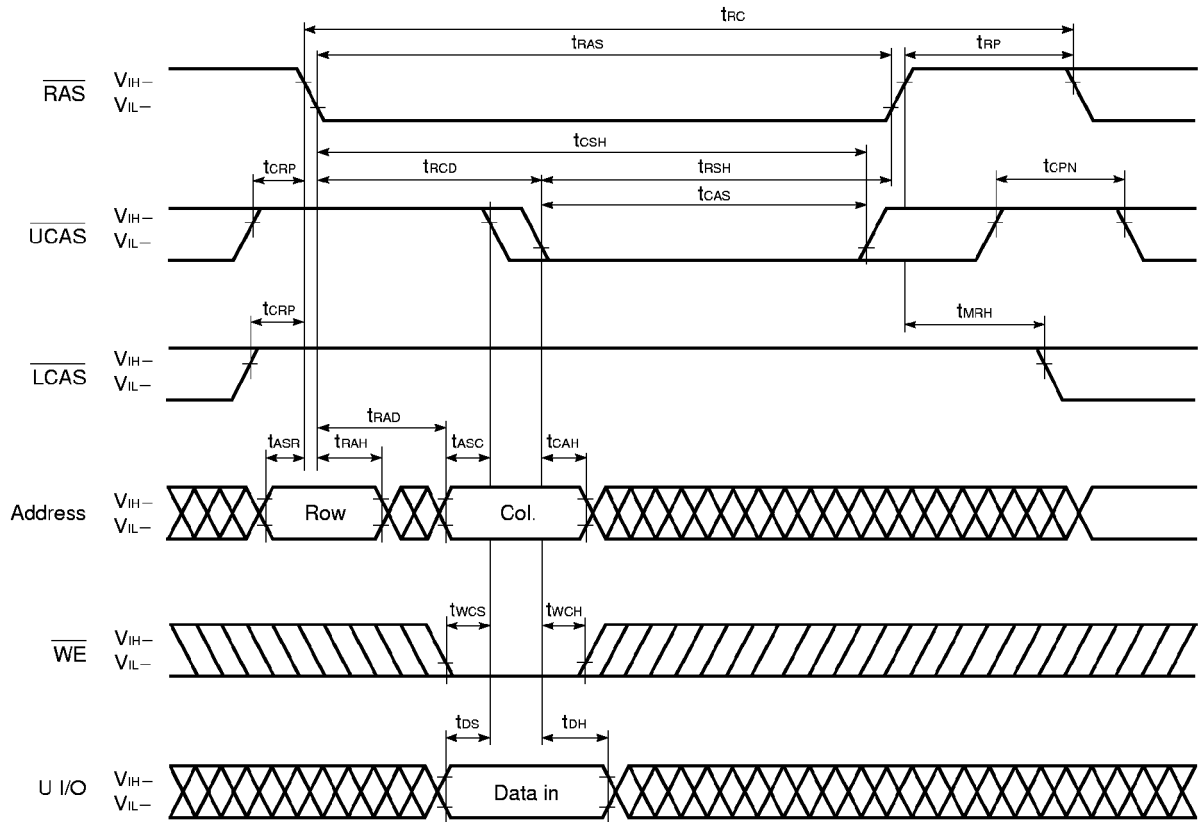
Remark U I/O: Hi-Z

Early Write Cycle



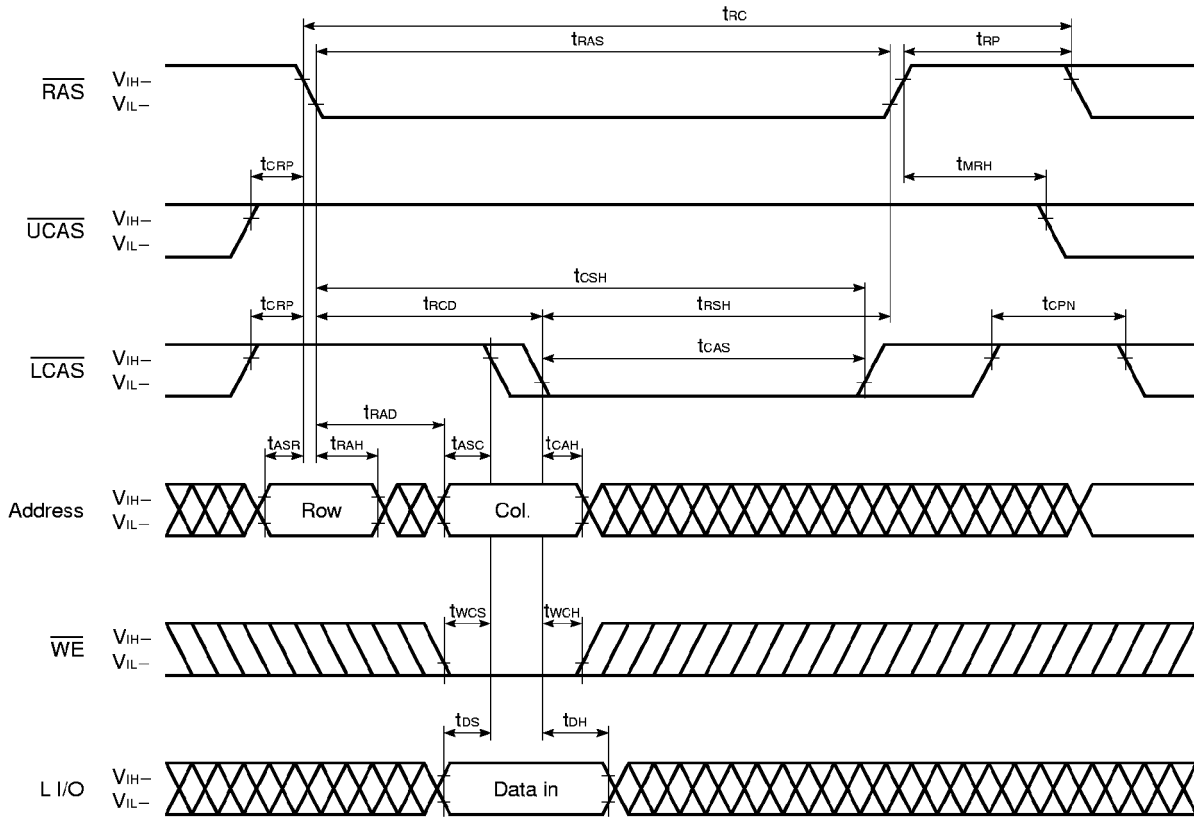
Remark \overline{OE} : Don't care

Upper Byte Early Write Cycle



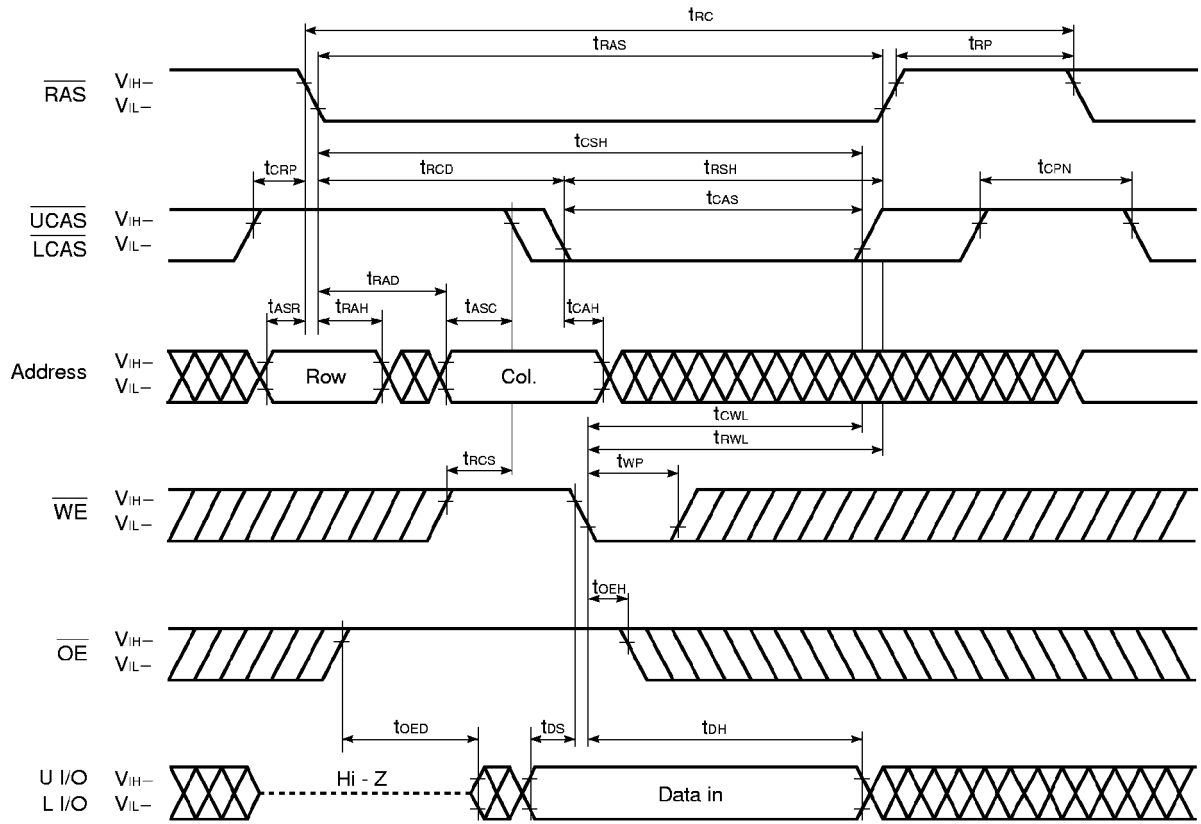
Remark \overline{OE} , L I/O: Don't care

Lower Byte Early Write Cycle

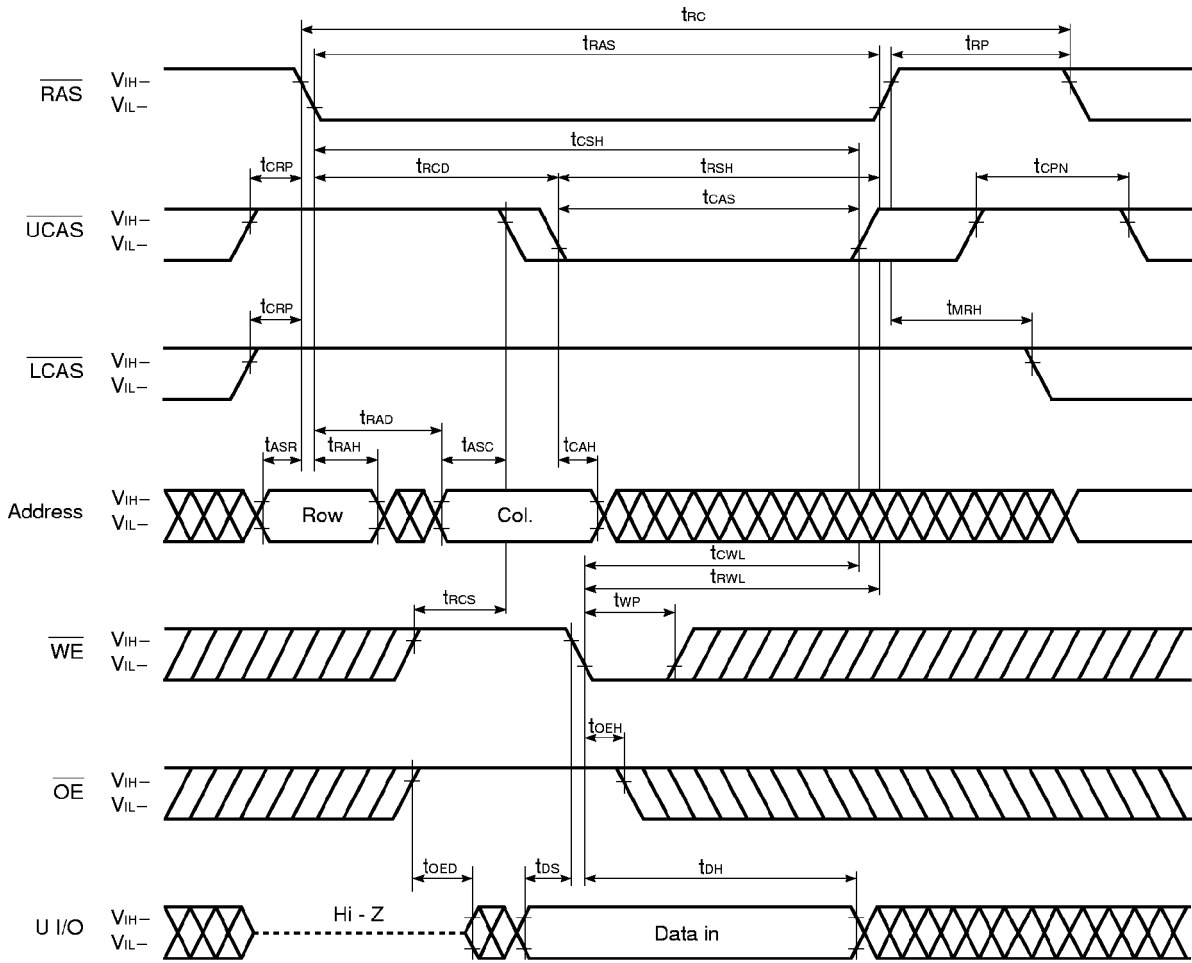


Remark \overline{OE} , U I/O: Don't care

Late Write Cycle

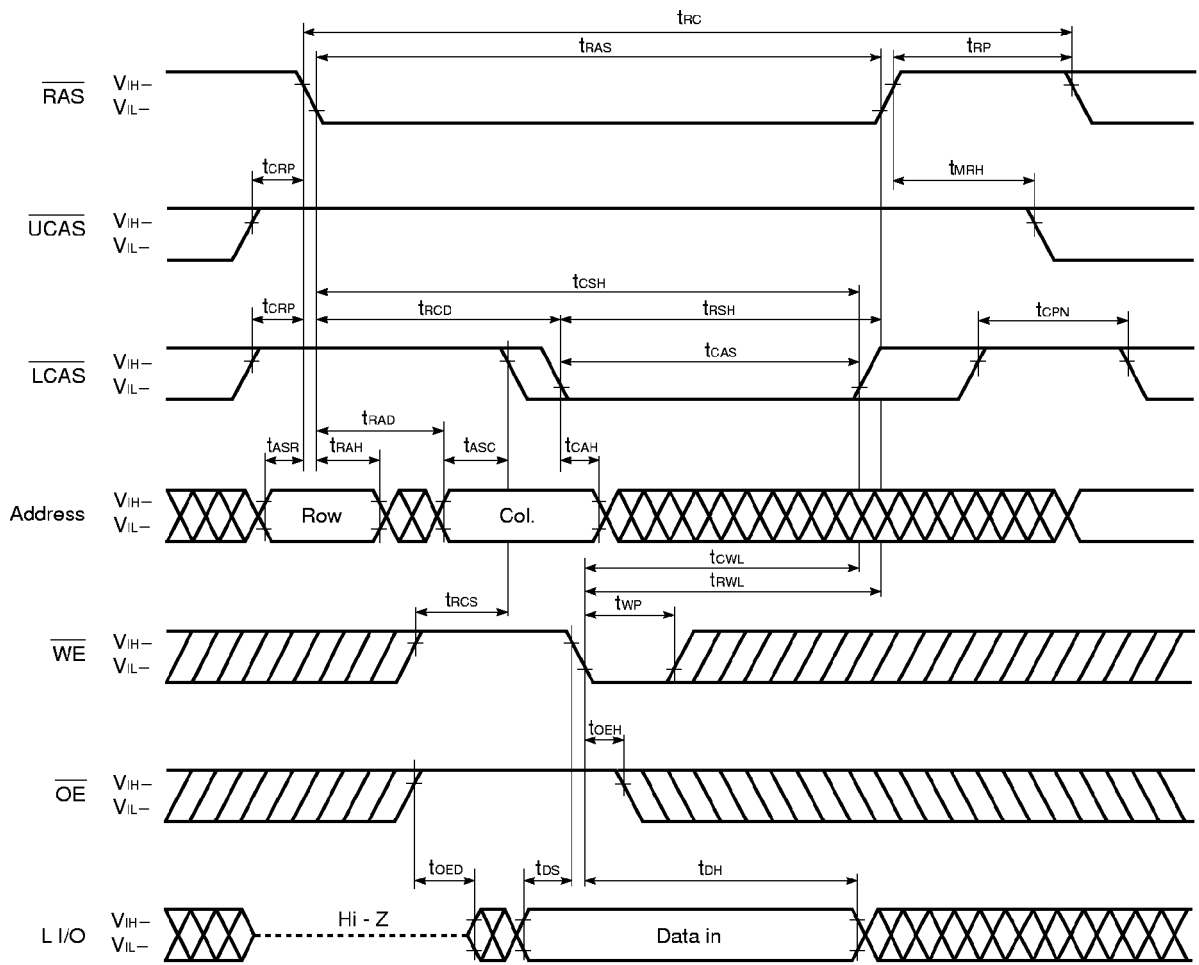


Upper Byte Late Write Cycle



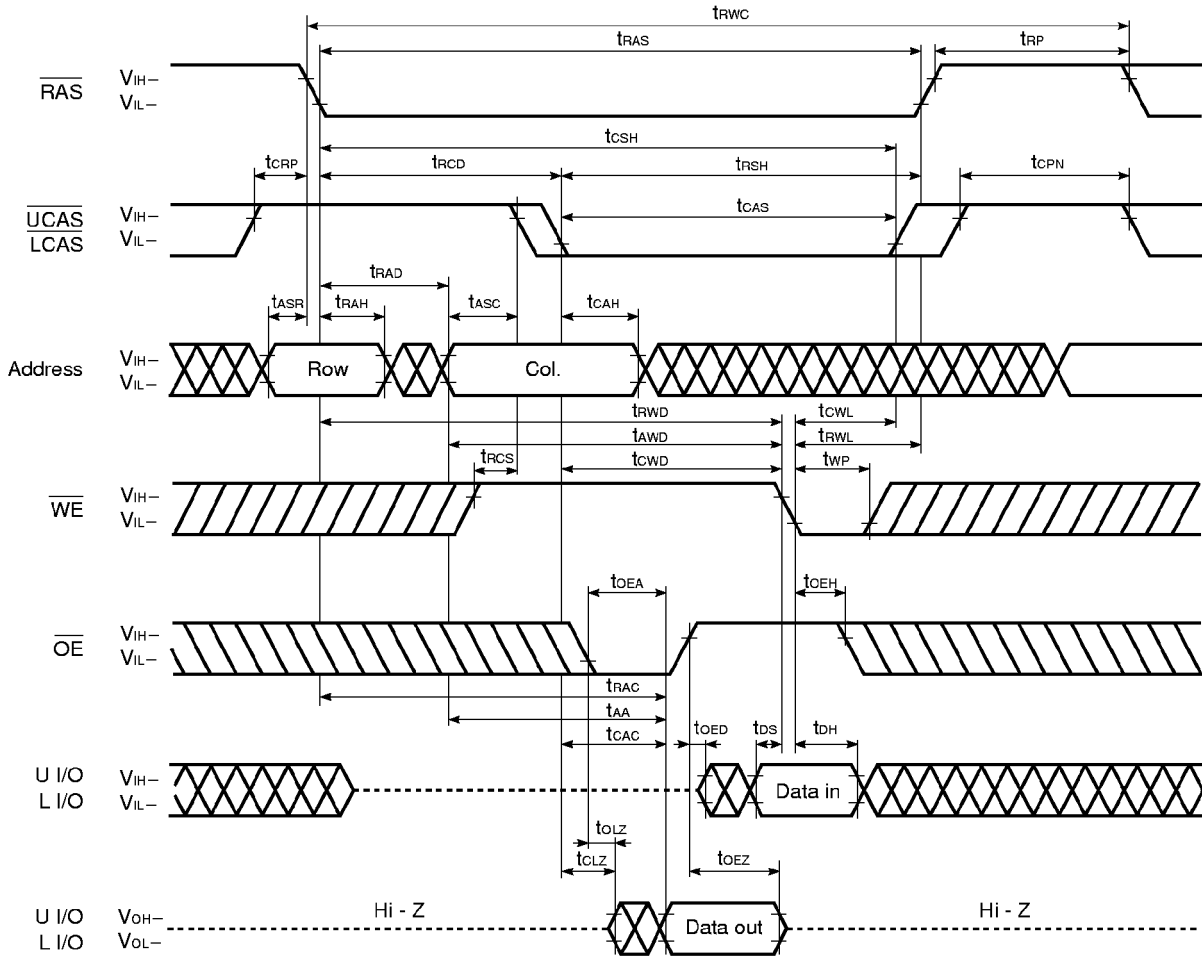
Remark L I/O: Don't care

Lower Byte Late Write Cycle

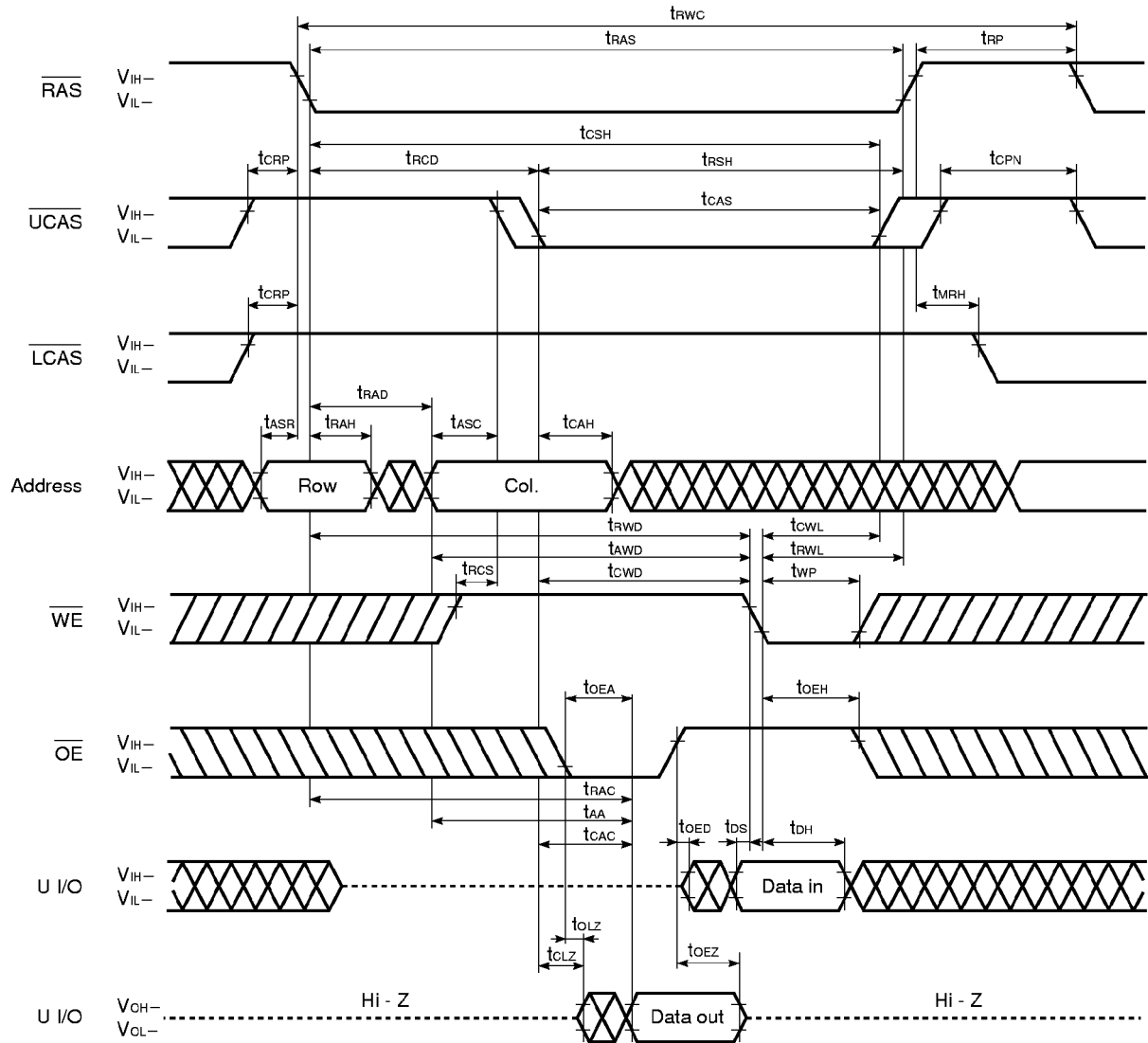


Remark U I/O: Don't care

Read Modify Write Cycle

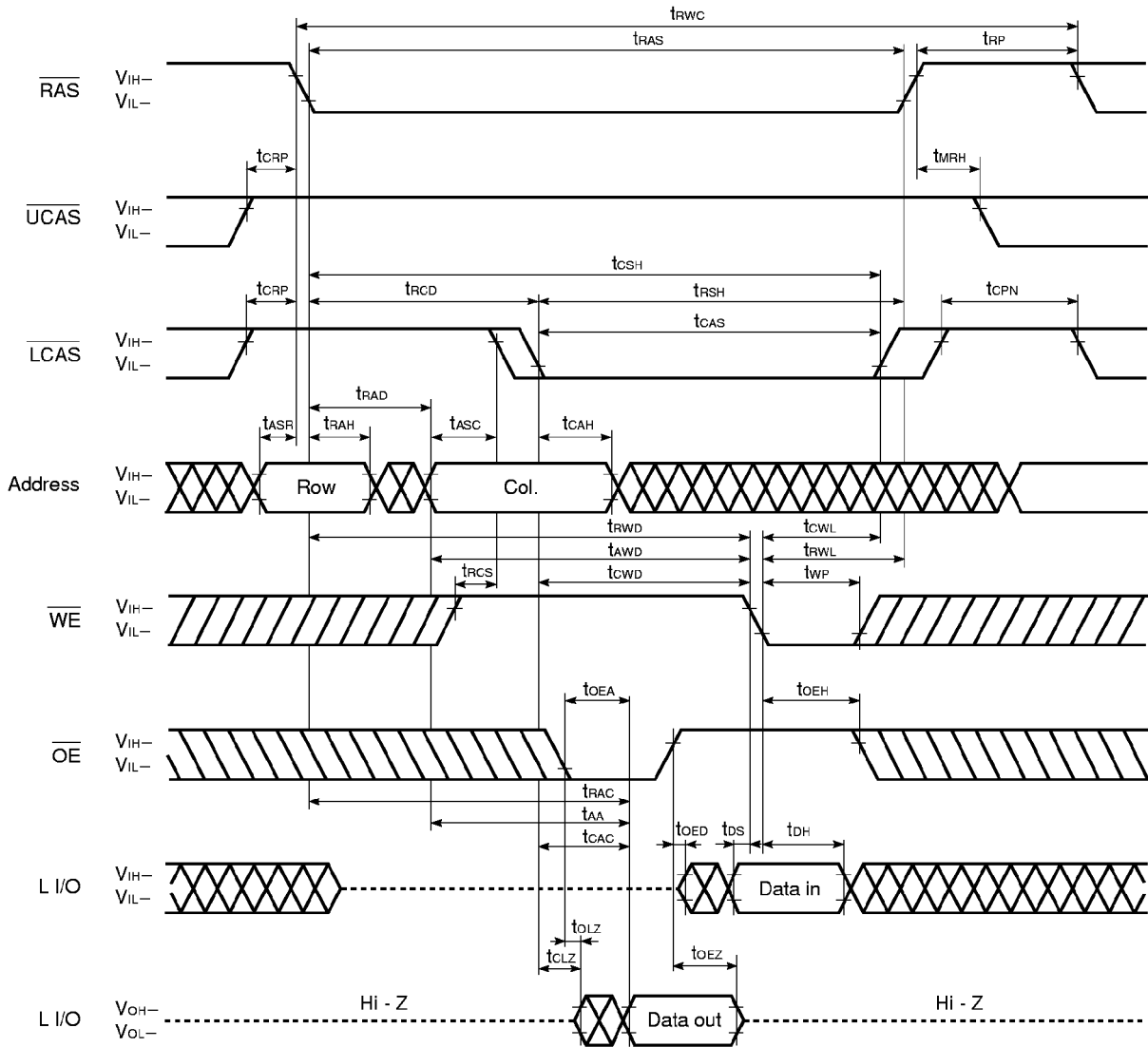


Upper Byte Read Modify Write Cycle



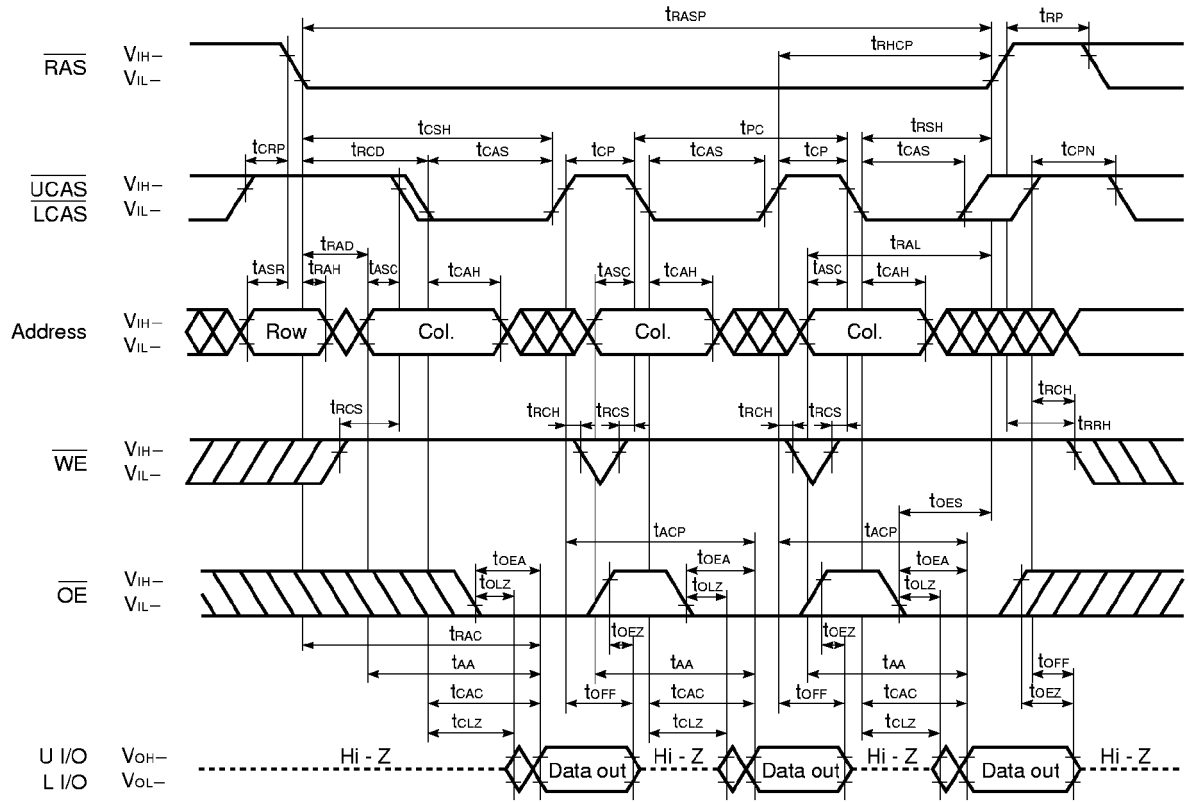
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



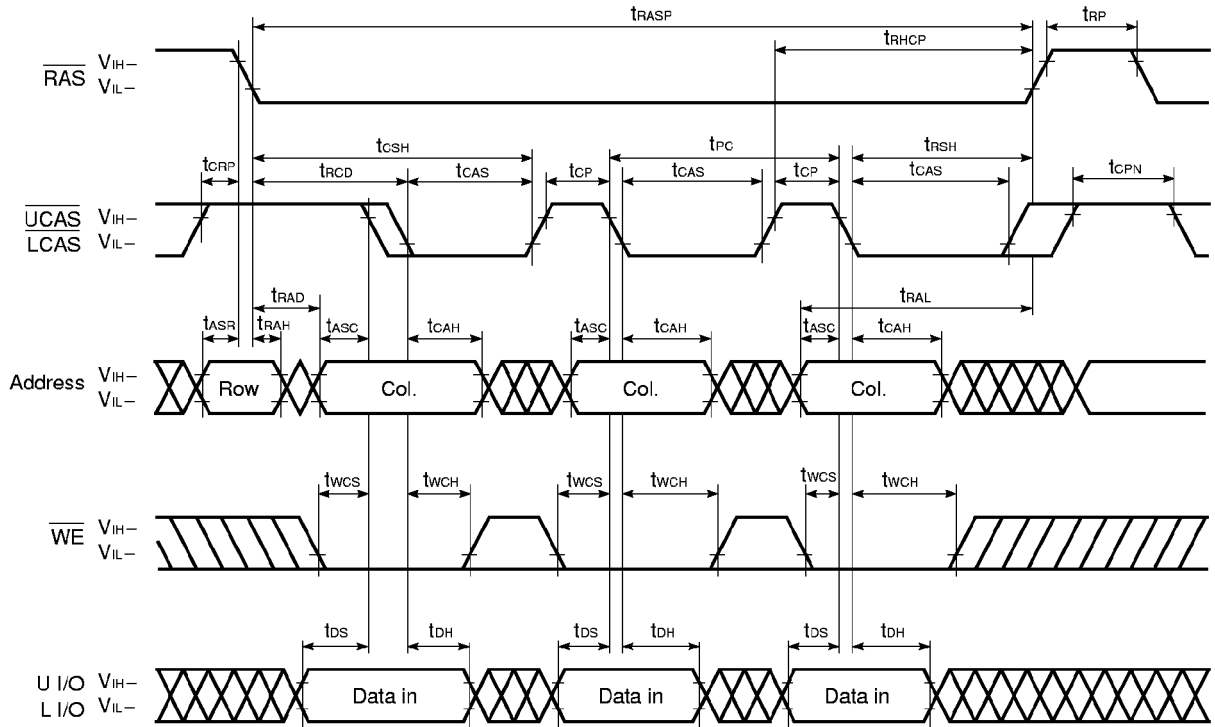
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Fast Page Mode Read Cycle



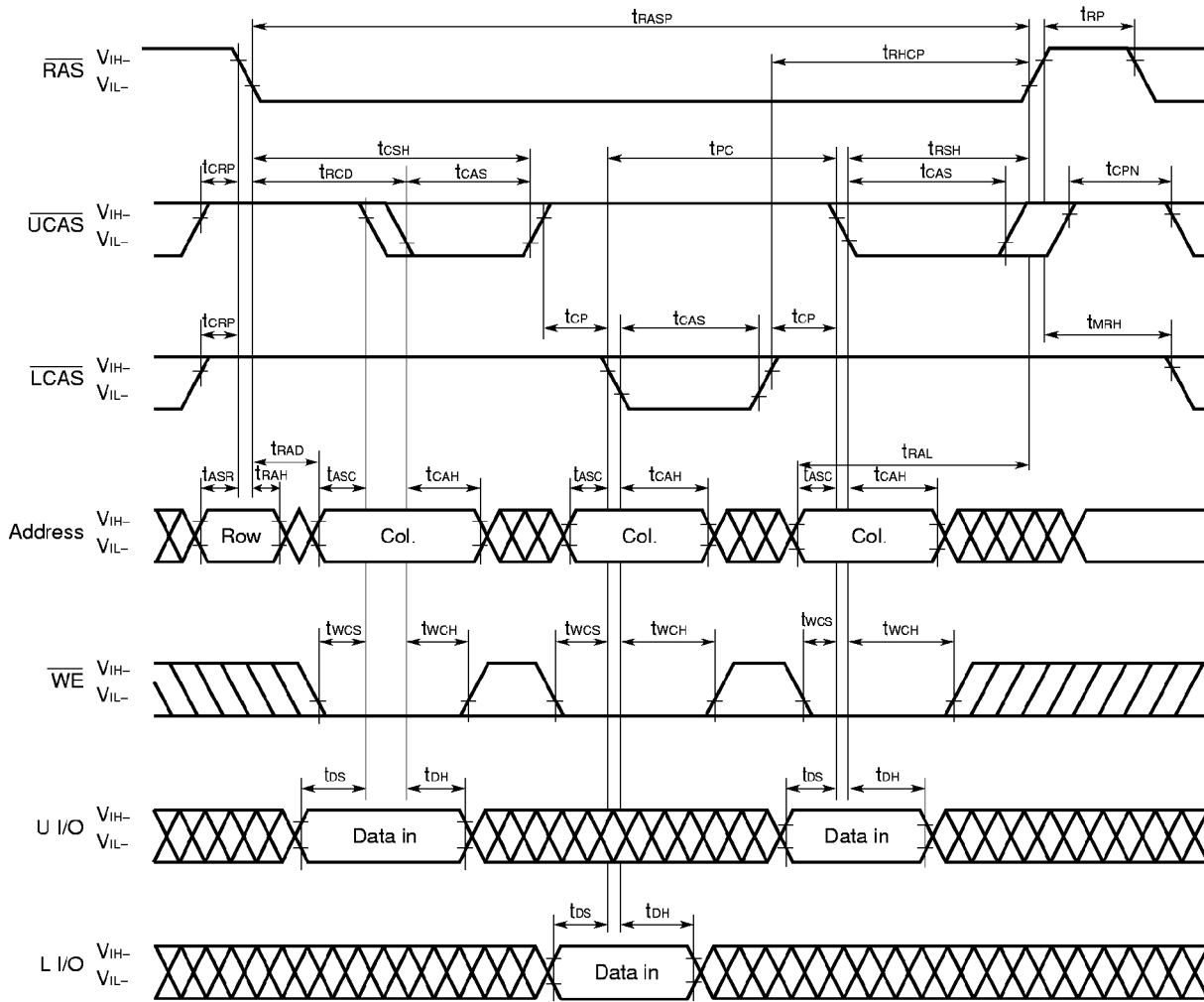
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



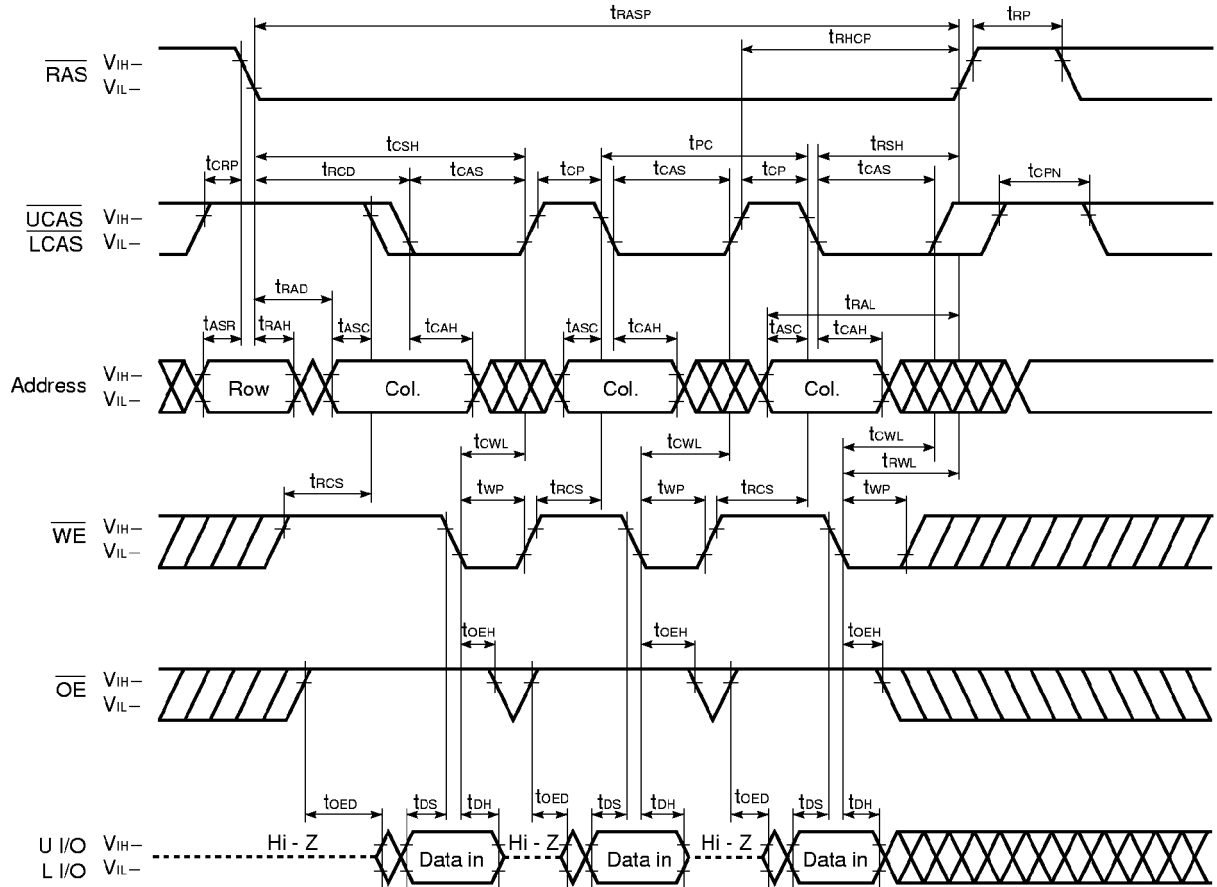
- Remarks**
1. \overline{OE} : Don't care
 2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive \overline{CAS} cycles within the same \overline{RAS} cycle.

Fast Page Mode Byte Early Write Cycle



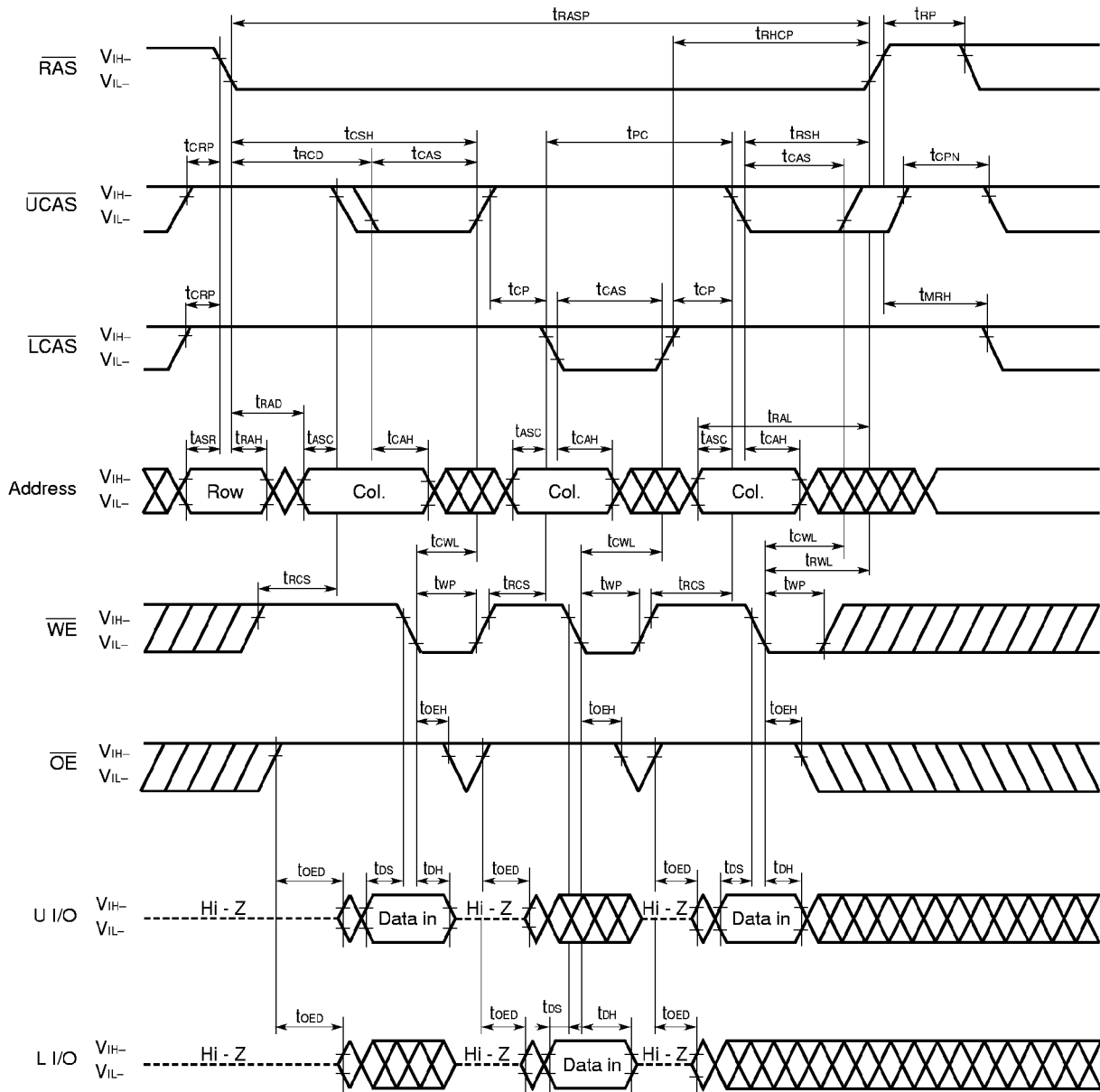
- Remarks**
1. $\overline{\text{OE}}$: Don't care
 2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
 3. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

Fast Page Mode Late Write Cycle



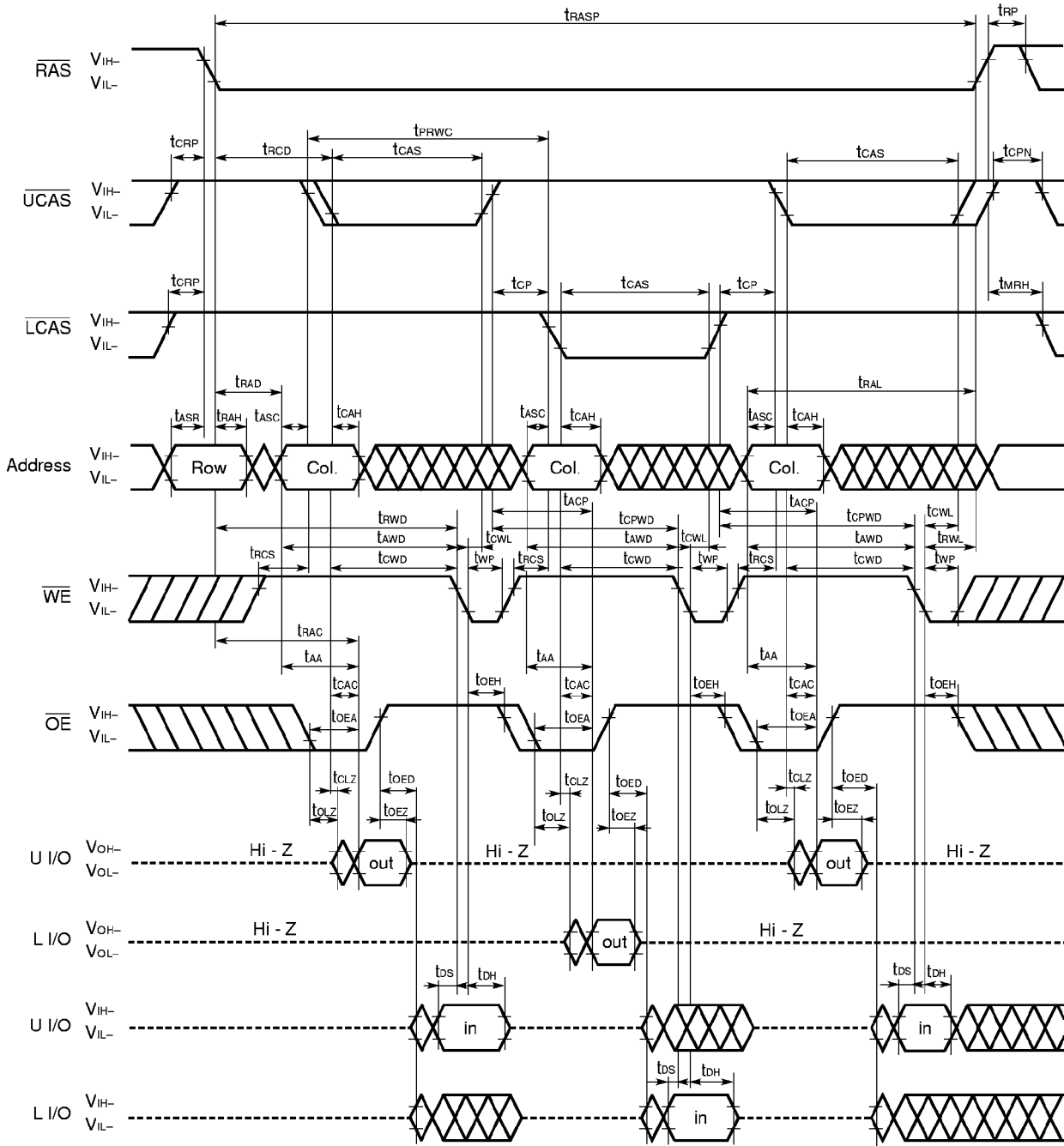
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Byte Late Write Cycle



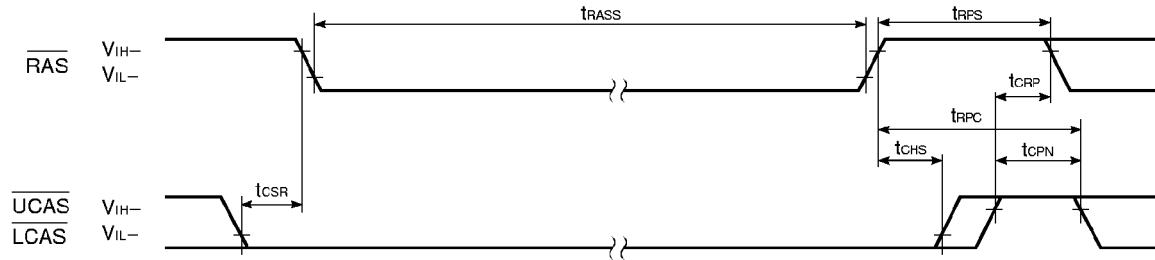
- Remarks**
1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
 2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

Fast Page Mode Byte Read Modify Write Cycle



- Remarks**
1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive \overline{CAS} cycles within the same \overline{RAS} cycle.
 2. This cycle can be used to control either \overline{UCAS} or \overline{LCAS} only. Or, it can be used to control \overline{UCAS} or \overline{LCAS} simultaneously, or at random.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh Cycle (Only for the μ PD42S16160, 42S18160)



Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with long $\overline{\text{RAS}}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Long Refresh

When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh are used in combination, please perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh as follows just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

μ PD42S16160: 4,096 times within a 64 ms interval
 μ PD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Long $\overline{\text{RAS}}$ Only Refresh

When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and $\overline{\text{RAS}}$ only refresh are used in combination, please perform $\overline{\text{RAS}}$ only refresh as follows just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

μ PD42S16160: 4,096 times within a 64 ms interval
 μ PD42S18160: 1,024 times within a 16 ms interval

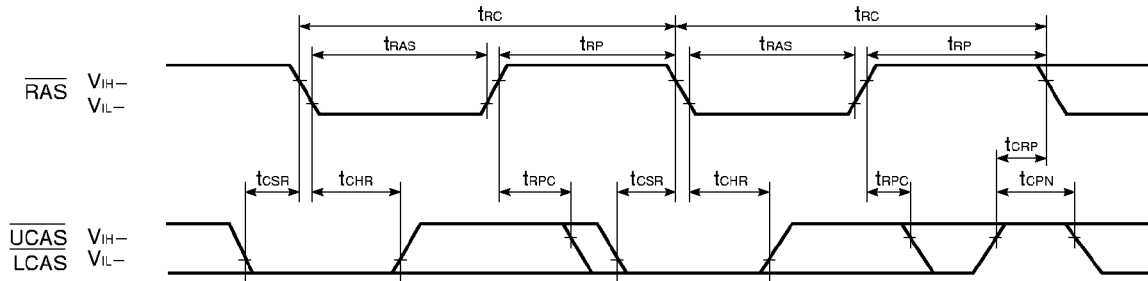
(3) If $t_{RASS(MIN)}$ is not satisfied at the beginning of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh cycles ($t_{RAS} < 100 \mu\text{s}$), $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles will be executed one time. ★

If $10 \mu\text{s} < t_{RAS} < 100 \mu\text{s}$, $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied. And refresh cycles as follows should be met.

μ PD42S16160: 4,096 times within a 128 ms interval
 μ PD42S18160: 1,024 times within a 128 ms interval

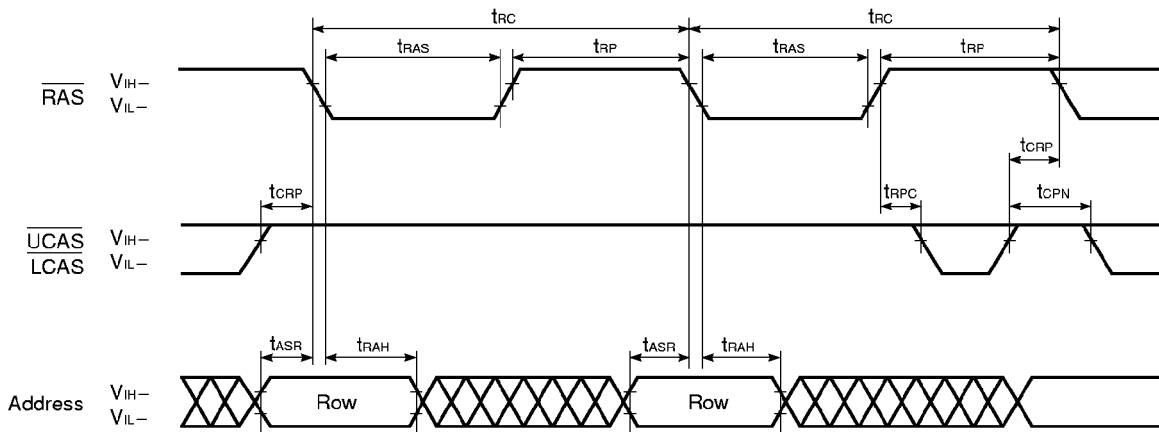
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



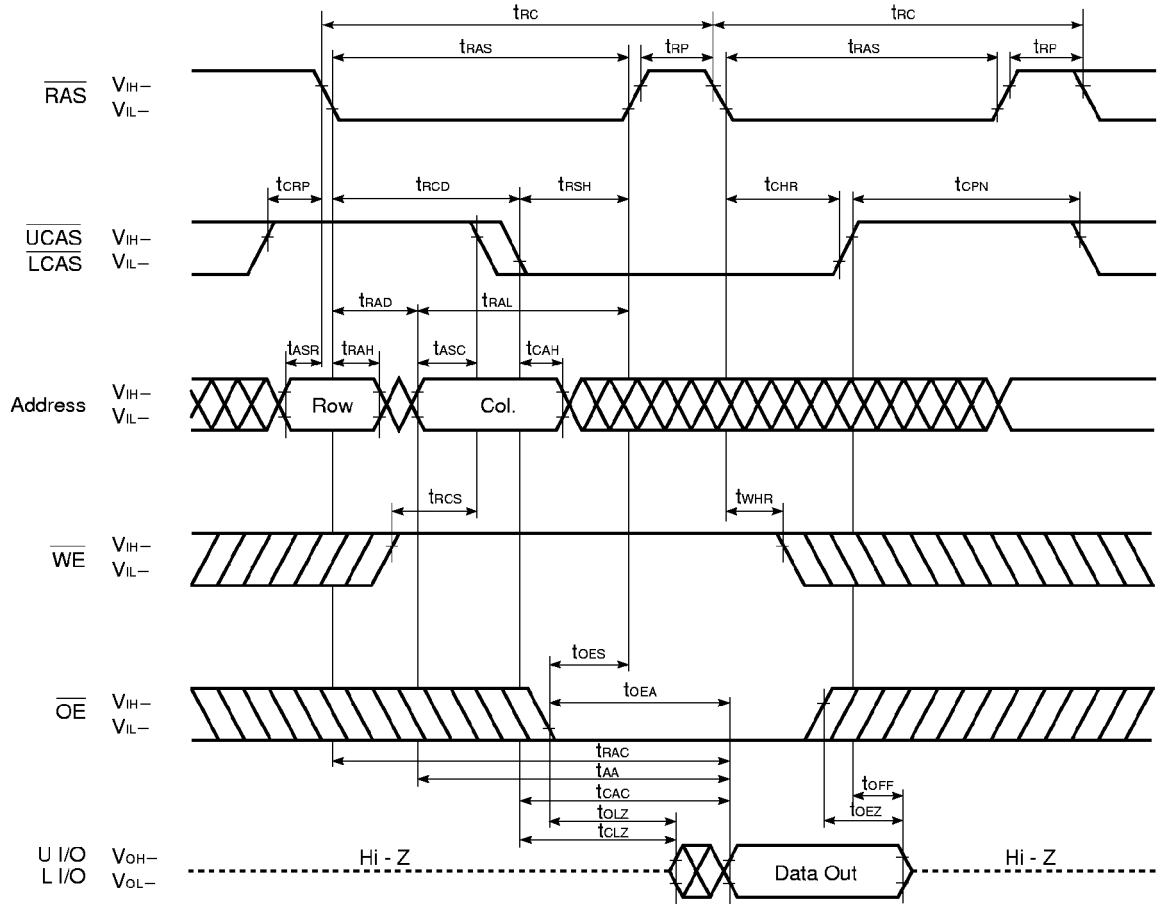
Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle

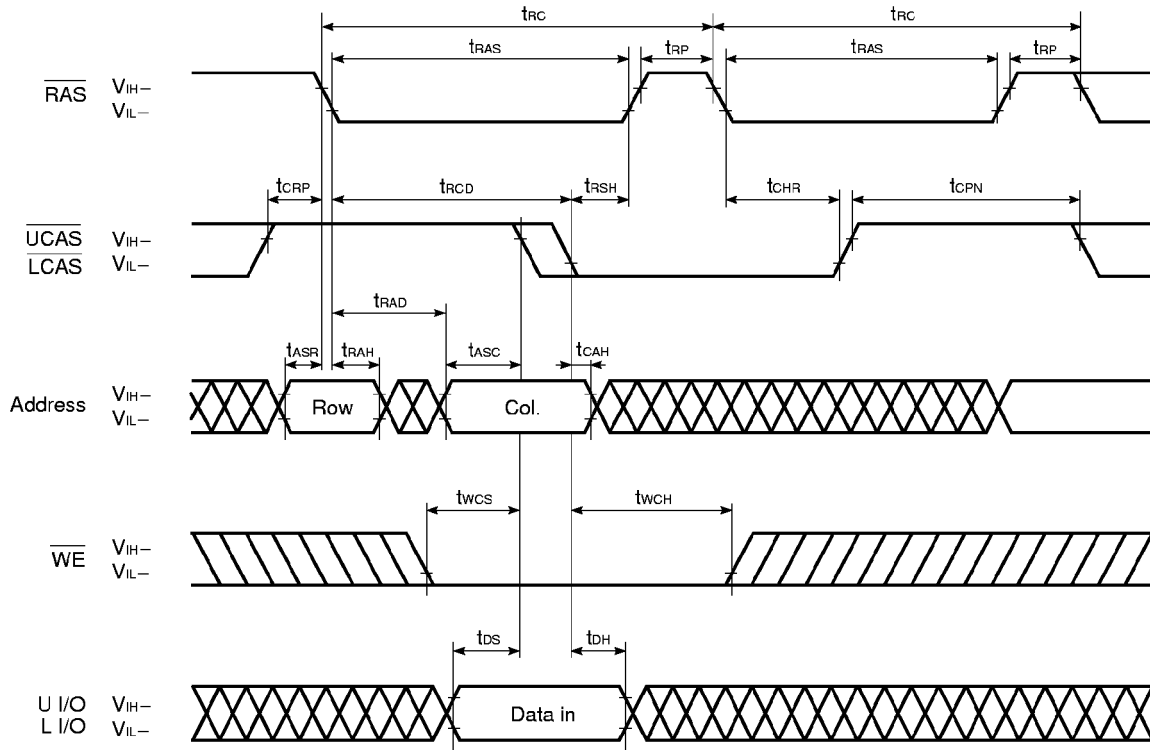


Remark \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



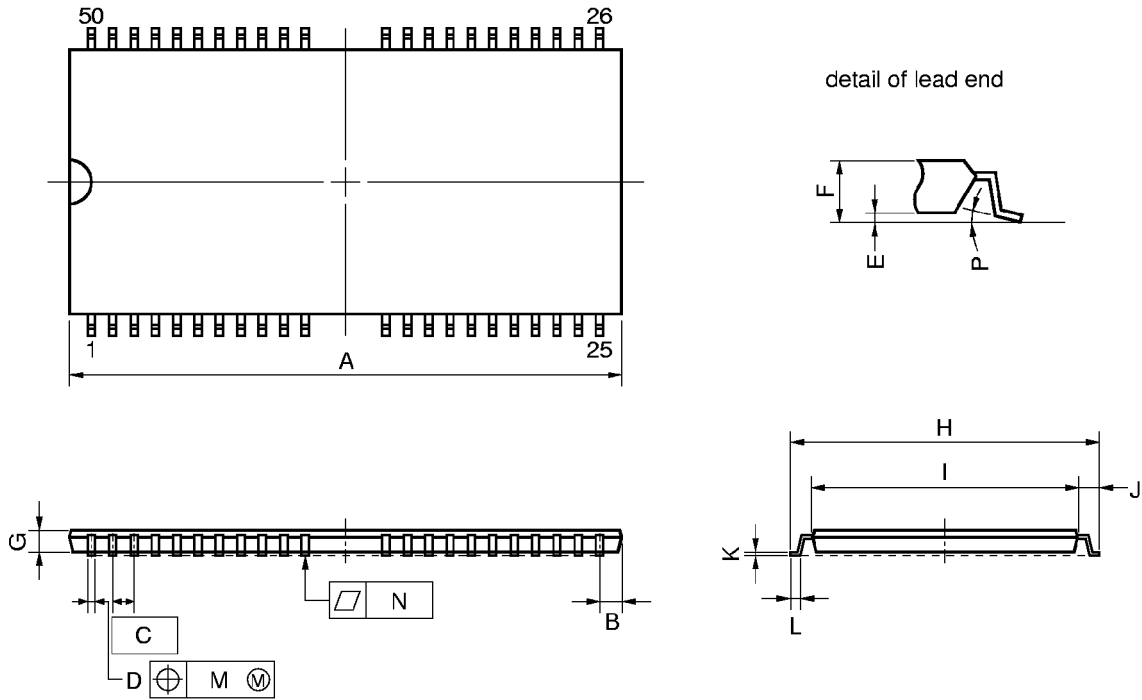
Hidden Refresh Cycle (Write)



Remark \overline{OE} : Don't care

Package Drawings

50PIN PLASTIC TSOP(II) (400 mil)



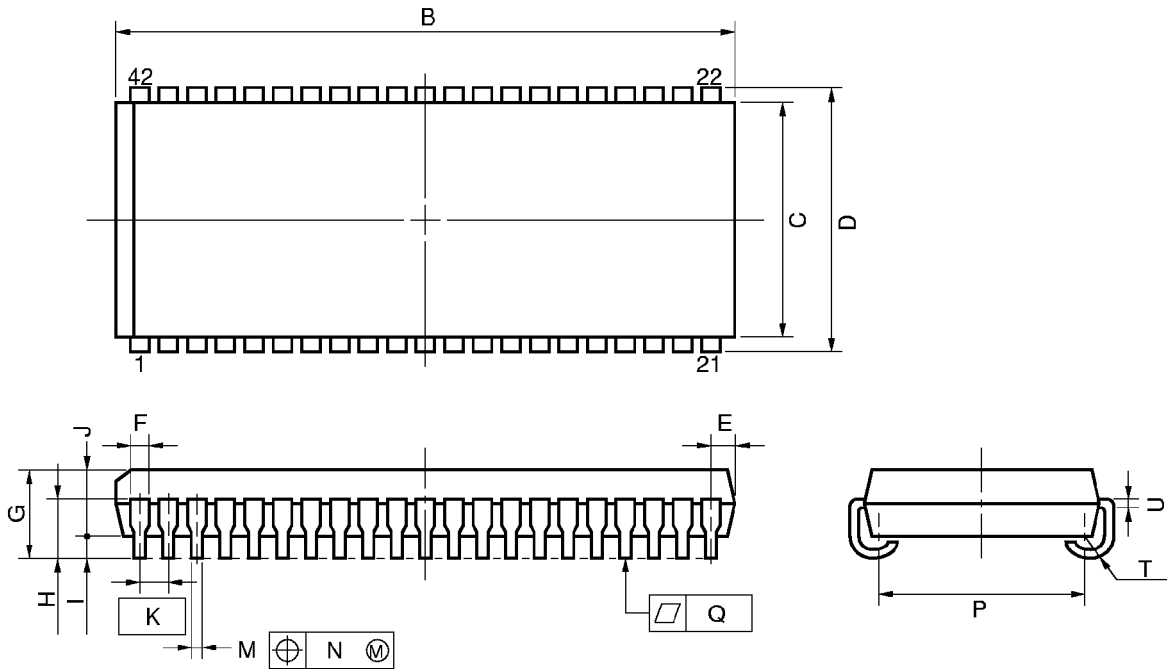
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P42LE-400A

ITEM	MILLIMETERS	INCHES
B	27.56 ^{+0.2} _{-0.35}	1.085 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S16160, 4216160, 42S18160, 4218160.

For more details, refer to our document “SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16160G5-7JF, 4216160G5-7JF, 42S18160G5-7JF, 4218160G5-7JF: 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards) Cautions 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.

μPD42S16160LE, 4216160LE, 42S18160LE, 4218160LE: 42-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	<p>Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^{Note} (20 hours pre-baking is required at 125 °C afterwards)</p> <p>Cautions</p> <ol style="list-style-type: none"> 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process). 	IR35-207-2
VPS	<p>Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days^{Note} (20 hours pre-baking is required at 125 °C afterwards)</p> <p>Cautions</p> <ol style="list-style-type: none"> 1. After the first reflow process, cool the package down to room temperature, then start the second reflow process. 2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process). 	VP15-207-2
Partial heating method	<p>Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).</p>	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.