18-Mbit (512K x 36/1M x 18) Pipelined SRAM

Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250, 200, and 167 MHz
- Registered inputs and outputs for pipelined operation
- 2.5V core power supply
- Fast clock-to-output times, 2.6 ns (for 250-MHz device)
- Provides high-performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed writes
- Asynchronous output enable
- Single Cycle Chip Deselect
- CY7C1380DV25/CY7C1382DV25 available in JEDEC-standard Pb-free 100-pin TQFP, Pb-free and non Pb-free 165-ball FBGA package. CY7C1380FV25/CY7C1382FV25 available in Pb-free and non Pb-free 119-ball BGA package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- ZZ sleep mode option

Functional Description [1]

The CY7C1380DV25/CY7C1382DV25/CY7C1380FV25/CY7C1382FV25 SRAM integrates 512K x 36 and 1M x 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive edge triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE_1}$), depth expansion chip enables (CE_2 and $\overline{CE_3}$ [2]), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW_X}$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self timed write cycle.This part supports byte write operations (see Pin Definitions on page 6 and Truth Table [4, 5, 6, 7, 8] on page 9 for further details). Write cycles can be one to two or four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ when active LOW causes all bytes to be written.

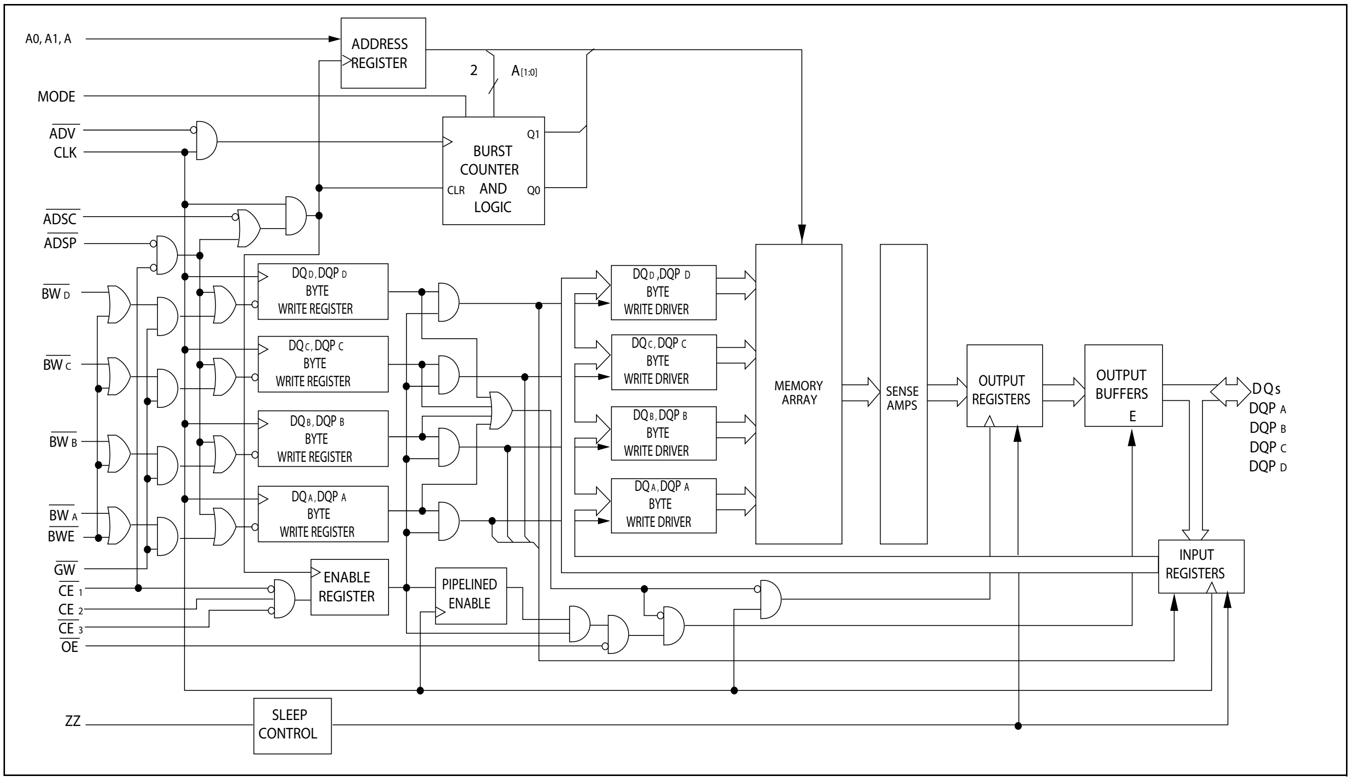
The CY7C1380DV25/CY7C1382DV25/CY7C1380FV25/CY7C1382FV25 operates from a +2.5V core power supply while all outputs may operate with a +2.5 supply. All inputs and outputs are JEDEC-standard and JESD8-5-compatible.

Selection Guide

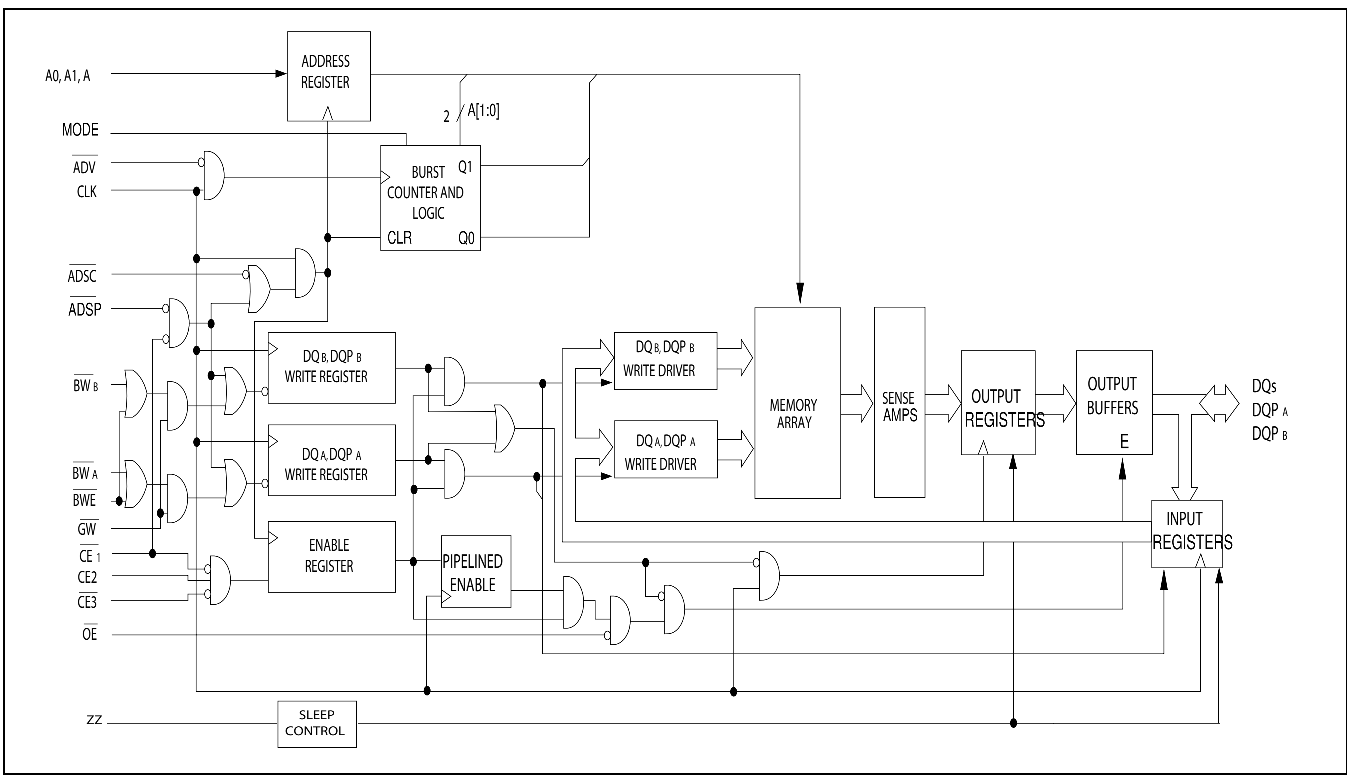
	250 MHz	200 MHz	167 MHz	Unit
Maximum Access Time	2.6	3.0	3.4	ns
Maximum Operating Current	350	300	275	mA
Maximum CMOS Standby Current	70	70	70	mA

Notes:
1. For best practices or recommendations, please refer to the Cypress application note AN1064, *SRAM System Design Guidelines* on www.cypress.com.
2. $\overline{CE_3}$, CE_2 are for TQFP and 165 FBGA packages only. 119 BGA is offered only in 1 chip enable

Logic Block Diagram – CY7C1380DV25/CY7C1380FV25 [3] (512K x 36)



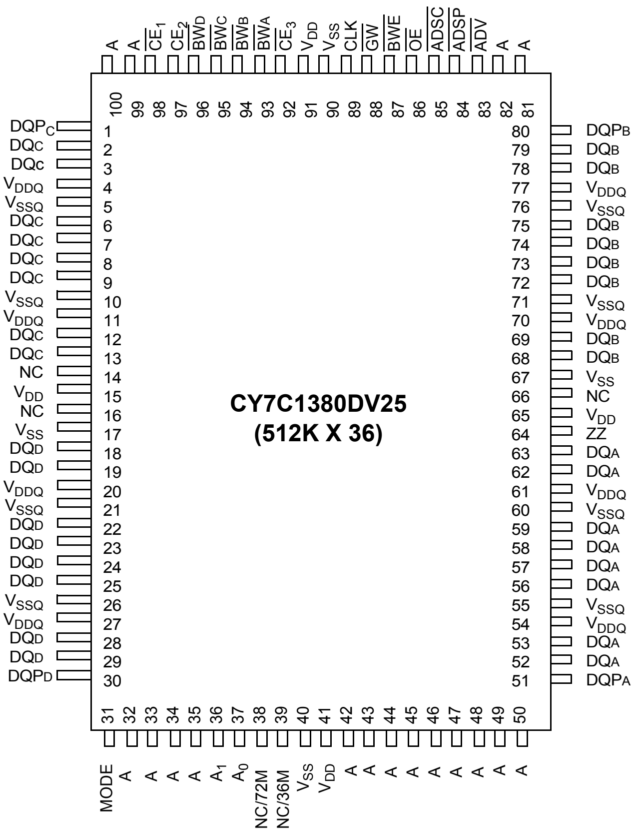
Logic Block Diagram – CY7C1382DV25/CY7C1382FV25 [3] (1M x 18)

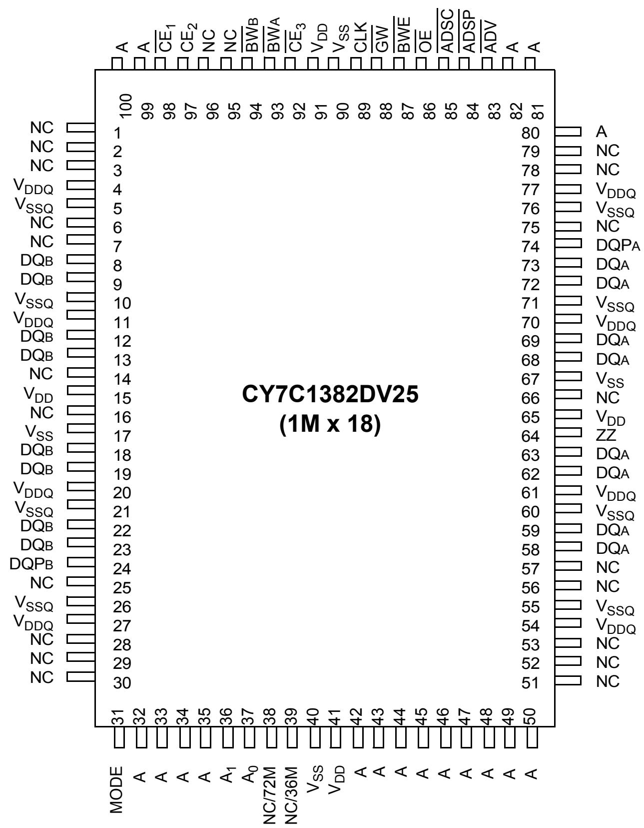


Note:
3. CY7C1380F and CY7C1382F have only 1 Chip Enable ($\overline{CE}_1$).

Pin Configurations

100-pin TQFP Pinout (3 Chip Enable)





Pin Configurations (continued)

119-Ball BGA Pinout

CY7C1380FV25 (512K x 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC/288M	A	A	$\overline{ADSC}$	A	A	NC/576M
C	NC/144M	A	A	V_{DD}	A	A	NC/1G
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW}_C$	$\overline{ADV}$	$\overline{BW}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW}_D$	NC	$\overline{BW}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BWE}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1382FV25 (1M x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC/288M	A	A	$\overline{ADSC}$	A	A	NC/576M
C	NC/144M	A	A	V_{DD}	A	A	NC/1G
D	DQ_B	NC	V_{SS}	NC	V_{SS}	DQP_A	NC
E	NC	DQ_B	V_{SS}	$\overline{CE}_1$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{BW}_B$	$\overline{ADV}$	NC	NC	DQ_A
H	DQ_B	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CLK	V_{SS}	NC	DQ_A
L	DQ_B	NC	NC	NC	$\overline{BW}_A$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	DQ_B	NC	V_{SS}	A1	V_{SS}	DQ_A	NC
P	NC	DQP_B	V_{SS}	A0	V_{SS}	NC	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC/72M	A	A	NC/36M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-Ball FBGA Pinout (3 Chip Enable)

CY7C1380DV25 (512K x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1382DV25 (1M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC/144M	A	CE2	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_A
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	IO	Description
A_0, A_1, A	Input-Synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$[2]are sampled active. A1: A0 are fed to the two-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$ $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2 [2]	Input-Synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$ [2]	Input-Synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the IO pins. When LOW, the IO pins behave as outputs. When deasserted HIGH, IO pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ sleep input**. This active HIGH input places the device in a non-time critical sleep condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQs, DQP_X	IO-Synchronous	**Bidirectional data IO lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.

Pin Definitions (continued)

Name	IO	Description
V_{SSQ}	IO Ground	**Ground for the IO circuitry**.
V_{DDQ}	IO Power Supply	**Power supply for the IO circuitry**.
MODE	Input-Static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull up.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be disconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not used, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No Connects**. Not internally connected to the die
NC/(36M,72M, 144M, 288M, 576M, 1G)	–	**These pins are not connected**. They will be used for expansion to the 36M, 72M, 144M, 288M, 576M and 1G densities.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.6 ns (250-MHz device).

The CY7C1380DV25/CY7C1382DV25/CY7C1380FV25/CY7C1382FV25 supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium® and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ($\overline{\mathrm{ADSP}}$) or the controller address strobe ($\overline{\mathrm{ADSC}}$). Address advancement through the burst sequence is controlled by the $\overline{\mathrm{ADV}}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ($\overline{\mathrm{BWE}}$) and byte write select ($\overline{\mathrm{BW}}_X$) inputs. A global write enable ($\overline{\mathrm{GW}}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip selects ($\overline{\mathrm{CE}}_1$, CE_2, $\overline{\mathrm{CE}}_3$) and an asynchronous output enable ($\overline{\mathrm{OE}}$) provide for easy bank selection and output tri-state control. $\overline{\mathrm{ADSP}}$ is ignored if $\overline{\mathrm{CE}}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{\mathrm{ADSP}}$ or $\overline{\mathrm{ADSC}}$ is asserted LOW, (2) $\overline{\mathrm{CE}}_1$, CE_2, $\overline{\mathrm{CE}}_3$ are all asserted active, and (3) the write signals ($\overline{\mathrm{GW}}$, $\overline{\mathrm{BWE}}$) are all deasserted HIGH. $\overline{\mathrm{ADSP}}$ is ignored if $\overline{\mathrm{CE}}_1$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the address register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 2.6 ns (250-MHz device) if $\overline{\mathrm{OE}}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{\mathrm{OE}}$ signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{\mathrm{ADSP}}$ or $\overline{\mathrm{ADSC}}$ signals, its output will tri-state immediately.

Single Write Accesses Initiated by $\overline{\mathrm{ADSP}}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{\mathrm{ADSP}}$ is asserted LOW, and (2) $\overline{\mathrm{CE}}_1$, CE_2, $\overline{\mathrm{CE}}_3$ are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The write signals ($\overline{\mathrm{GW}}$, $\overline{\mathrm{BWE}}$, and $\overline{\mathrm{BW}}_X$) and $\overline{\mathrm{ADV}}$ inputs are ignored during this first cycle.

ADSP triggered write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the write operation is controlled by BWE and BW_X signals.

The CY7C1380DV25/CY7C1382DV25/CY7C1380FV25/ CY7C1382FV25 provides byte write capability that is described in the write cycle descriptions table. Asserting the byte write enable input (BWE) with the selected byte write (BW_X) input, will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations.

The CY7C1380DV25/CY7C1382DV25/CY7C1380FV25/ CY7C1382FV25 is a common IO device, the output enable (OE) must be deserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) CE_1, CE_2, CE_3 are all asserted active, and (4) the appropriate combination of the write inputs (GW, BWE, and BW_X) are asserted active to conduct a write to the desired byte(s). ADSC triggered write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations.

The CY7C1380DV25/CY7C1382DV25/CY7C1380FV25/ CY7C1382FV25 is a common IO device, the output enable (OE) must be deserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1380DV25/CY7C1382DV25/CY7C1380FV25/ CY7C1382FV25 provides a two-bit wraparound counter, fed by A1: A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting ADV LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. CE_1, CE_2, CE_3, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		80	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ Active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table [4, 5, 6, 7, 8]

Operation	Add. Used	$\overline{CE}_1$	CE_2	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L-H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes:
4. X = Don't Care, H = Logic HIGH, L = Logic LOW.
5. $\overline{WRITE}$ = L when any one or more byte write enable signals, and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
6. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
7. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_X$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are Tri-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write [6, 9]

Function (CY7C1380DV25/CY7C1380FV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	H	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – (DQ_C and DQP_C)	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – (DQ_D and DQP_D)	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Truth Table for Read/Write [6, 9]

Function (CY7C1382DV25/CY7C1382FV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	L	H
Write Bytes B, A	H	L	L	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

Note:
9. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write will be done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

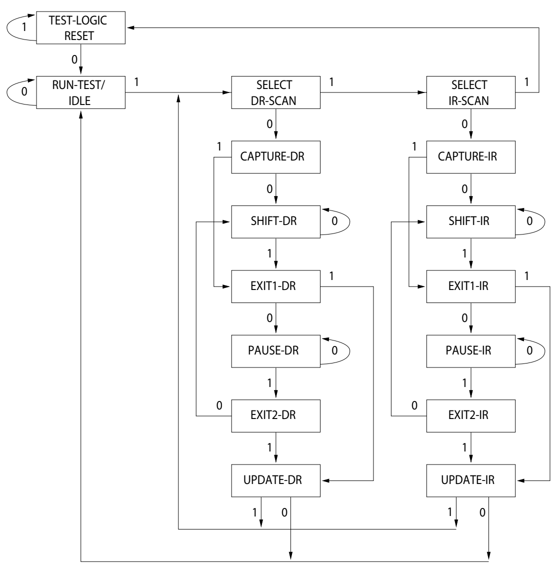
The CY7C1380DV25/CY7C1382DV25 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3V or 2.5V IO logic levels.

The CY7C1380DV25/CY7C1382DV25 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device will come up in a reset state which will not interfere with the operation of the device.

TAP Controller State Diagram



The 0 or 1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

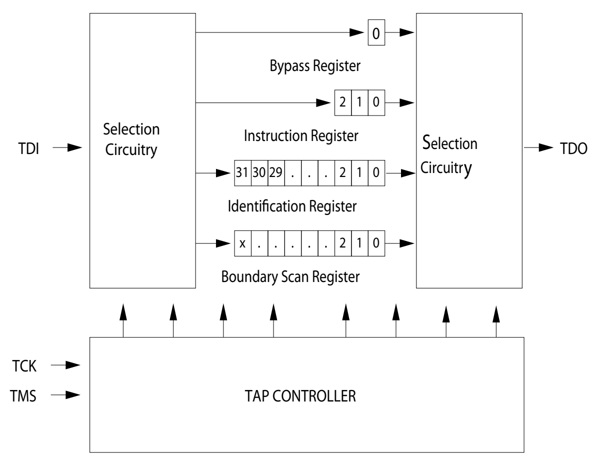
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See TAP Controller Block Diagram).

Test Data-Out (TDO)

The TDO output ball is used to serially clock data out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See TAP Controller State Diagram).

TAP Controller Block Diagram



Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary ‘01’ pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The boundary scan order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions on page 14.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in Identification Codes on page 15. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the Shift-DR controller state.

IDCODE

The IDCODE instruction causes a vendor specific 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. The SAMPLE Z command places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. As there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required; that is, while data captured is shifted out, the preloaded data is shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST Output Bus Tri-State

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

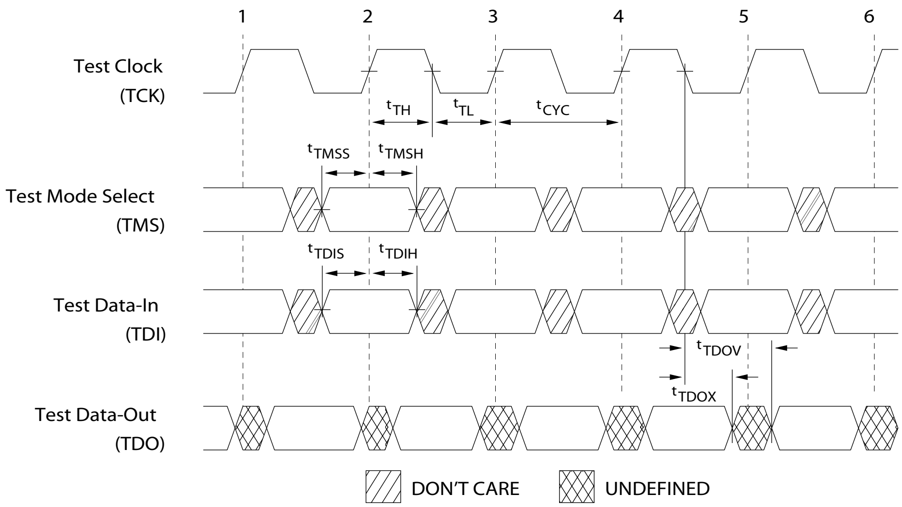
The boundary scan register has a special bit located at bit #85 (for 119-BGA package) or bit #89 (for 165-fBGA package). When this scan cell, called the “extest output bus tri-state,” is latched into the preload register during the Update-DR state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP AC Switching Characteristics

Over the Operating Range [10, 11]

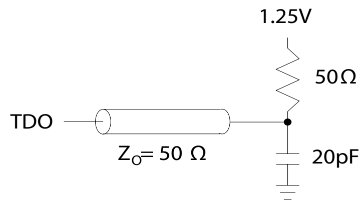
Parameter	Description	Min.	Max.	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	20		ns
t_{TL}	TCK Clock LOW time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes:
10. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1ns.

2.5V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 2.5V
Input rise and fall time .... 1 ns
Input timing reference levels 1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operating Conditions

(0°C < T_A < +70°C; V_{DD} = 2.5V ±0.125V unless otherwise noted) [12]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –1.0 mA, V_{DDQ} = 2.5V		2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA, V_{DDQ} = 2.5V		2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA, V_{DDQ} = 2.5V			0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Identification Register Definitions

Instruction Field	CY7C1380DV25/ CY7C1380FV25 (512K x 36)	CY7C1382DV25/ CY7C1382FV25 (1 Mbit x 18)	Description
Revision Number (31:29)	000	000	Describes the version number.
Device Depth (28:24)	01011	01011	Reserved for internal use.
Device Width (23:18) 119-BGA	101000	101000	Defines the memory type and architecture.
Device Width (23:18) 165-FBGA	000000	000000	Defines the memory type and architecture.
Cypress Device ID (17:12)	100101	010101	Defines the width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-ball BGA package)	85	85
Boundary Scan Order (165-ball FBGA package)	89	89

Note:
12. All voltages referenced to V_{SS} (GND).

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use. This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use. This instruction is reserved for future use.
RESERVED	110	Do Not Use. This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

119-Ball BGA Boundary Scan Order [13, 14]

Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID
1	H4	23	F6	45	G4	67	L1
2	T4	24	E7	46	A4	68	M2
3	T5	25	D7	47	G3	69	N1
4	T6	26	H7	48	C3	70	P1
5	R5	27	G6	49	B2	71	K1
6	L5	28	E6	50	B3	72	L2
7	R6	29	D6	51	A3	73	N2
8	U6	30	C7	52	C2	74	P2
9	R7	31	B7	53	A2	75	R3
10	T7	32	C6	54	B1	76	T1
11	P6	33	A6	55	C1	77	R1
12	N7	34	C5	56	D2	78	T2
13	M6	35	B5	57	E1	79	L3
14	L7	36	G5	58	F2	80	R2
15	K6	37	B6	59	G1	81	T3
16	P7	38	D4	60	H2	82	L4
17	N6	39	B4	61	D1	83	N4
18	L6	40	F4	62	E2	84	P4
19	K7	41	M4	63	G2	85	Internal
20	J5	42	A5	64	H1		
21	H6	43	K4	65	J3		
22	G7	44	E4	66	2K		

Notes:
13. Balls that are NC (No Connect) are preset LOW.
14. Bit #85 is preset HIGH.

165-Ball BGA Boundary Scan Order [13, 15]

Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID
1	N6	31	D10	61	G1
2	N7	32	C11	62	D2
3	N10	33	A11	63	E2
4	P11	34	B11	64	F2
5	P8	35	A10	65	G2
6	R8	36	B10	66	H1
7	R9	37	A9	67	H3
8	P9	38	B9	68	J1
9	P10	39	C10	69	K1
10	R10	40	A8	70	L1
11	R11	41	B8	71	M1
12	H11	42	A7	72	J2
13	N11	43	B7	73	K2
14	M11	44	B6	74	L2
15	L11	45	A6	75	M2
16	K11	46	B5	76	N1
17	J11	47	A5	77	N2
18	M10	48	A4	78	P1
19	L10	49	B4	79	R1
20	K10	50	B3	80	R2
21	J10	51	A3	81	P3
22	H9	52	A2	82	R3
23	H10	53	B2	83	P2
24	G11	54	C2	84	R4
25	F11	55	B1	85	P4
26	E11	56	A1	86	N5
27	D11	57	C1	87	P6
28	G10	58	D1	88	R6
29	F10	59	E1	89	Internal
30	E10	60	F1		

Note:
15. Bit #89 is preset HIGH.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. For user guidelines, not tested.

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied.. –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND .... –0.3V to +3.6V

Supply Voltage on V_{DDQ} Relative to GND ...... –0.3V to $+V_{DD}$

DC Voltage Applied to Outputs in Tri-State... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage .... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}/V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%
Industrial	–40°C to +85°C	

Electrical Characteristics

Over the Operating Range [16, 17]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	IO Supply Voltage	for 2.5V IO		2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	for 2.5V IO, $I_{OH} = -1.0$ mA		2.0		V
V_{OL}	Output LOW Voltage	for 2.5V IO, I_{OL}= 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage [16]	for 2.5V IO		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage [16]	for 2.5V IO		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	$GND \le V_I \le V_{DDQ}$		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{DD,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		350	mA
			5.0-ns cycle, 200 MHz		300	mA
			6.0-ns cycle, 167 MHz		275	mA
I_{SB1}	Automatic CE Power Down Current—TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		160	mA
			5.0-ns cycle, 200 MHz		150	mA
			6.0-ns cycle, 167 MHz		140	mA
I_{SB2}	Automatic CE Power Down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \le 0.3V$ or $V_{IN} \ge V_{DDQ} - 0.3V$, f = 0	All speeds		70	mA
I_{SB3}	Automatic CE Power Down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, or $V_{IN} \le 0.3V$ or $V_{IN} \ge V_{DDQ} - 0.3V$ f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		135	mA
			5.0-ns cycle, 200 MHz		130	mA
			6.0-ns cycle, 167 MHz		125	mA
I_{SB4}	Automatic CE Power Down Current—TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = 0	All speeds		80	mA

Notes:
16. Overshoot: $V_{IH}(AC) < V_{DD}$ +1.5V (pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (pulse width less than $t_{CYC}/2$).
17. $T_{power\ up}$: assumes a linear ramp from 0V to V_{DD}(min.) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.

Capacitance [18]

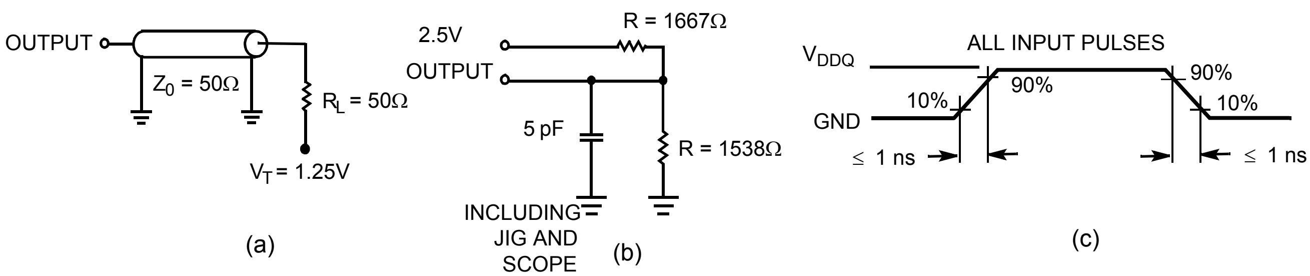
Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD}/V_{DDQ} = 2.5V	5	8	9	pF
C_{CLK}	Clock Input Capacitance		5	8	9	pF
C_{IO}	Input/Output Capacitance		5	8	9	pF

Thermal Resistance [18]

Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	28.66	23.8	20.7	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		4.08	6.2	4.0	°C/W

AC Test Loads and Waveforms

2.5V IO Test Load



Note:
18. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

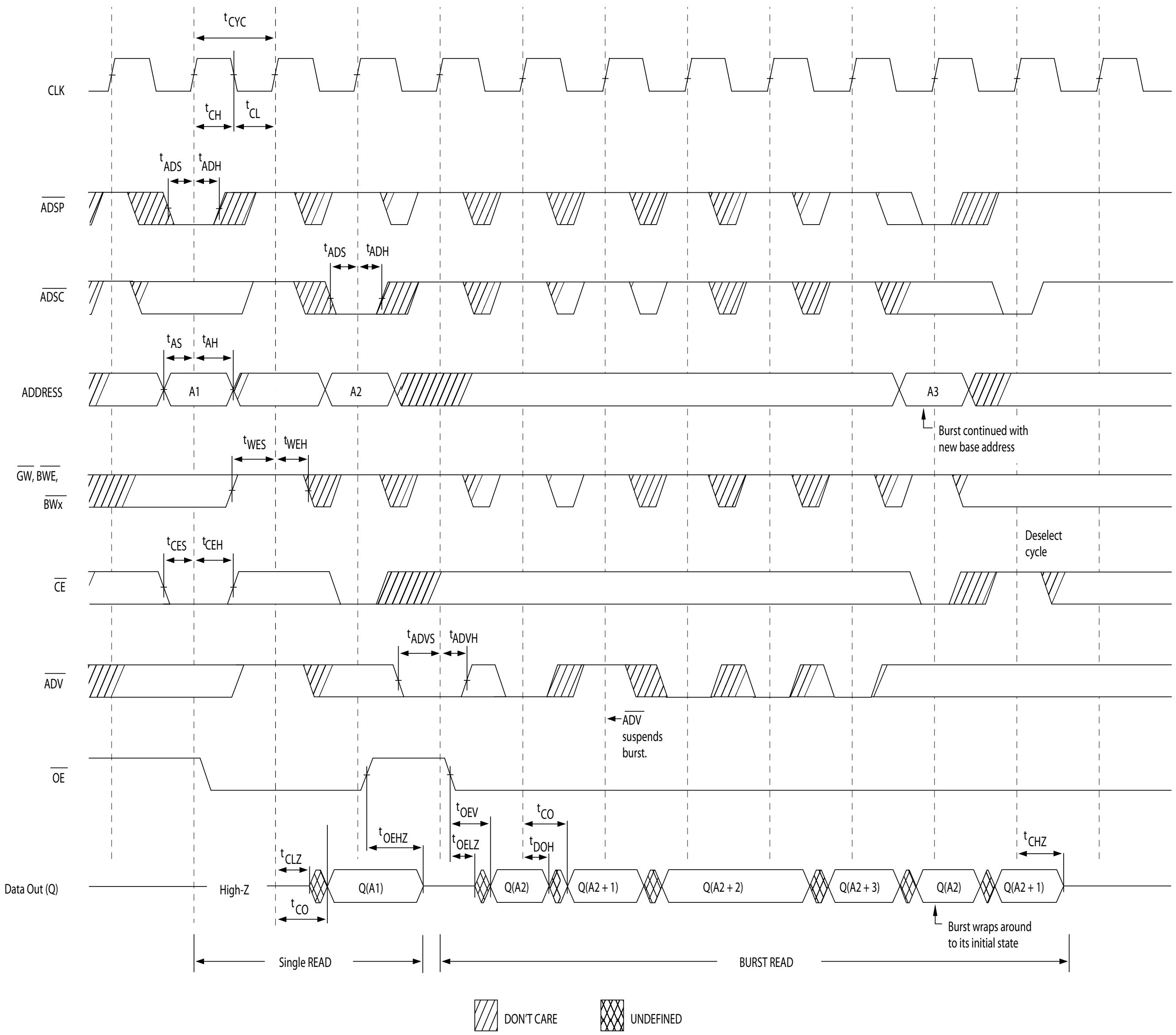
Over the Operating Range [19, 20]

Parameter	Description	250 MHz		200 MHz		167 MHz		Unit
		Min.	Max	Min.	Max.	Min.	Max	
t_{POWER}	V_{DD}(Typical) to the First Access [21]	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	4.0		5		6		ns
t_{CH}	Clock HIGH	1.7		2.0		2.2		ns
t_{CL}	Clock LOW	1.7		2.0		2.2		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise		2.6		3.0		3.4	ns
t_{DOH}	Data Output Hold After CLK Rise	1.0		1.3		1.3		ns
t_{CLZ}	Clock to Low-Z [22, 23, 24]	1.0		1.3		1.3		ns
t_{CHZ}	Clock to High-Z [22, 23, 24]		2.6		3.0		3.4	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		2.6		3.0		3.4	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z [22, 23, 24]	0		0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z [22, 23, 24]		2.6		3.0		3.4	ns
Setup Times								
t_{AS}	Address Setup Before CLK Rise	1.2		1.4		1.5		ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ Setup Before CLK Rise	1.2		1.4		1.5		ns
t_{ADVS}	$\overline{ADV}$ Setup Before CLK Rise	1.2		1.4		1.5		ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup Before CLK Rise	1.2		1.4		1.5		ns
t_{DS}	Data Input Setup Before CLK Rise	1.2		1.4		1.5		ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.2		1.4		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.3		0.4		0.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.3		0.4		0.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.3		0.4		0.5		ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Hold After CLK Rise	0.3		0.4		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.3		0.4		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.3		0.4		0.5		ns

Notes:
19. Timing reference level is 1.5V when V_{DDQ} = 1.25V when V_{DDQ} = 2.5V.
20. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
21. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above VDD(minimum) initially before a read or write operation can be initiated.
22. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
23. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
24. This parameter is sampled and not 100% tested.

Switching Waveforms

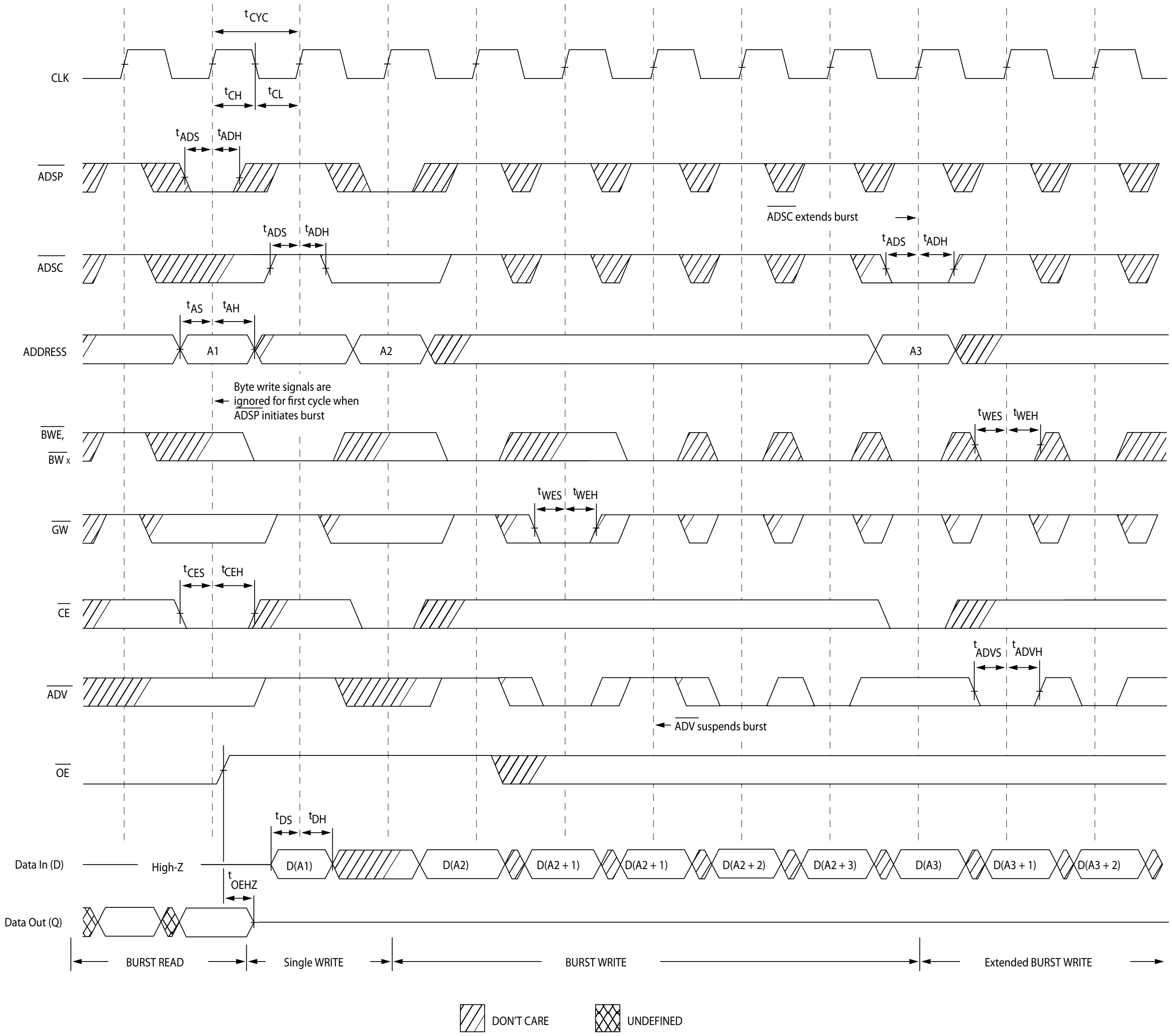
Read Cycle Timing [25]



Note:
25. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.

Switching Waveforms (continued)

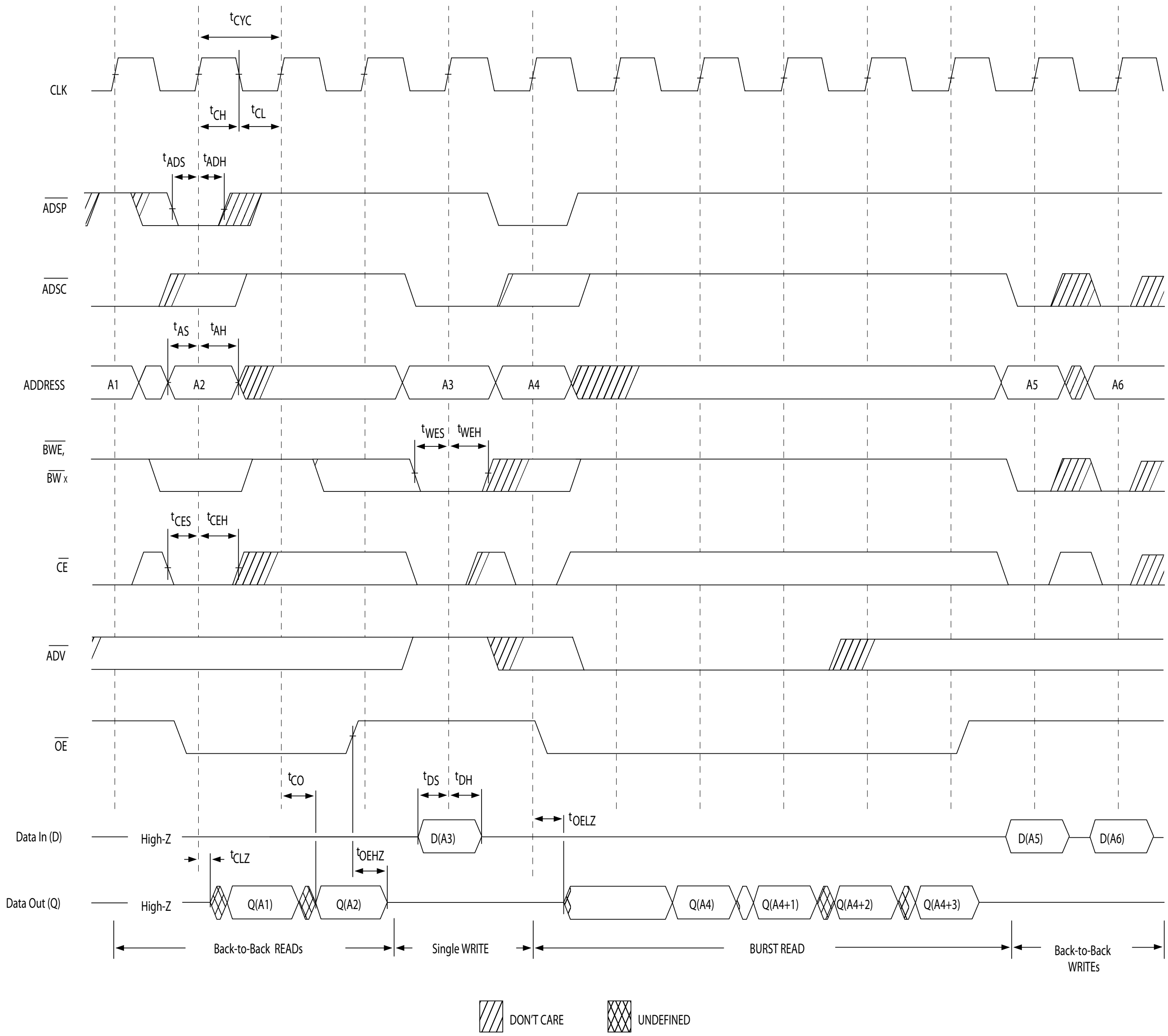
Write Cycle Timing [25, 26]



Note:
26. Full width write can be initiated by either $\overline{GW}$ LOW, or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW_X}$ LOW.

Switching Waveforms (continued)

Read/Write Cycle Timing [25, 27, 28]

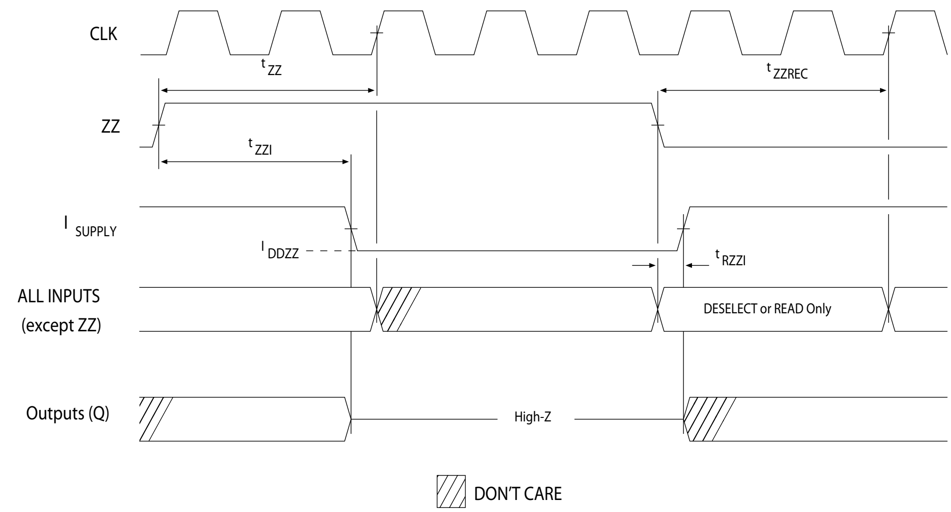


Notes:

27. The data bus (Q) remains in high-Z following a write cycle, unless a new read access is initiated by $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$.
28. $\overline{\text{GW}}$ is HIGH.

Switching Waveforms (continued)

ZZ Mode Timing [29, 30]



Notes:
29. Device must be deselected when entering ZZ sleep mode. See cycle descriptions table for all possible signal conditions to deselect the device.
30. DQs are in high-Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package, and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1380DV25-167AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1382DV25-167AXC			
	CY7C1380FV25-167BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1382FV25-167BGC			
	CY7C1380FV25-167BGXC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
	CY7C1382FV25-167BGXC			
	CY7C1380DV25-167BZC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1382DV25-167BZC			
	CY7C1380DV25-167BZXC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1382DV25-167BZXC			
	CY7C1380DV25-167AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1382DV25-167AXI			
	CY7C1380FV25-167BGI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1382FV25-167BGI			
	CY7C1380FV25-167BGXI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
	CY7C1382FV25-167BGXI			
	CY7C1380DV25-167BZI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1382DV25-167BZI			
	CY7C1380DV25-167BZXI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1382DV25-167BZXI			
200	CY7C1380DV25-200AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1382DV25-200AXC			
	CY7C1380FV25-200BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1382FV25-200BGC			
	CY7C1380FV25-200BGXC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
	CY7C1382FV25-200BGXC			
	CY7C1380DV25-200BZC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1382DV25-200BZC			
	CY7C1380DV25-200BZXC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1382DV25-200BZXC			
	CY7C1380DV25-200AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1382DV25-200AXI			
	CY7C1380FV25-200BGI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1382FV25-200BGI			
	CY7C1380FV25-200BGXI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
	CY7C1382FV25-200BGXI			
	CY7C1380DV25-200BZI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1382DV25-200BZI			
	CY7C1380DV25-200BZXI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1382DV25-200BZXI			

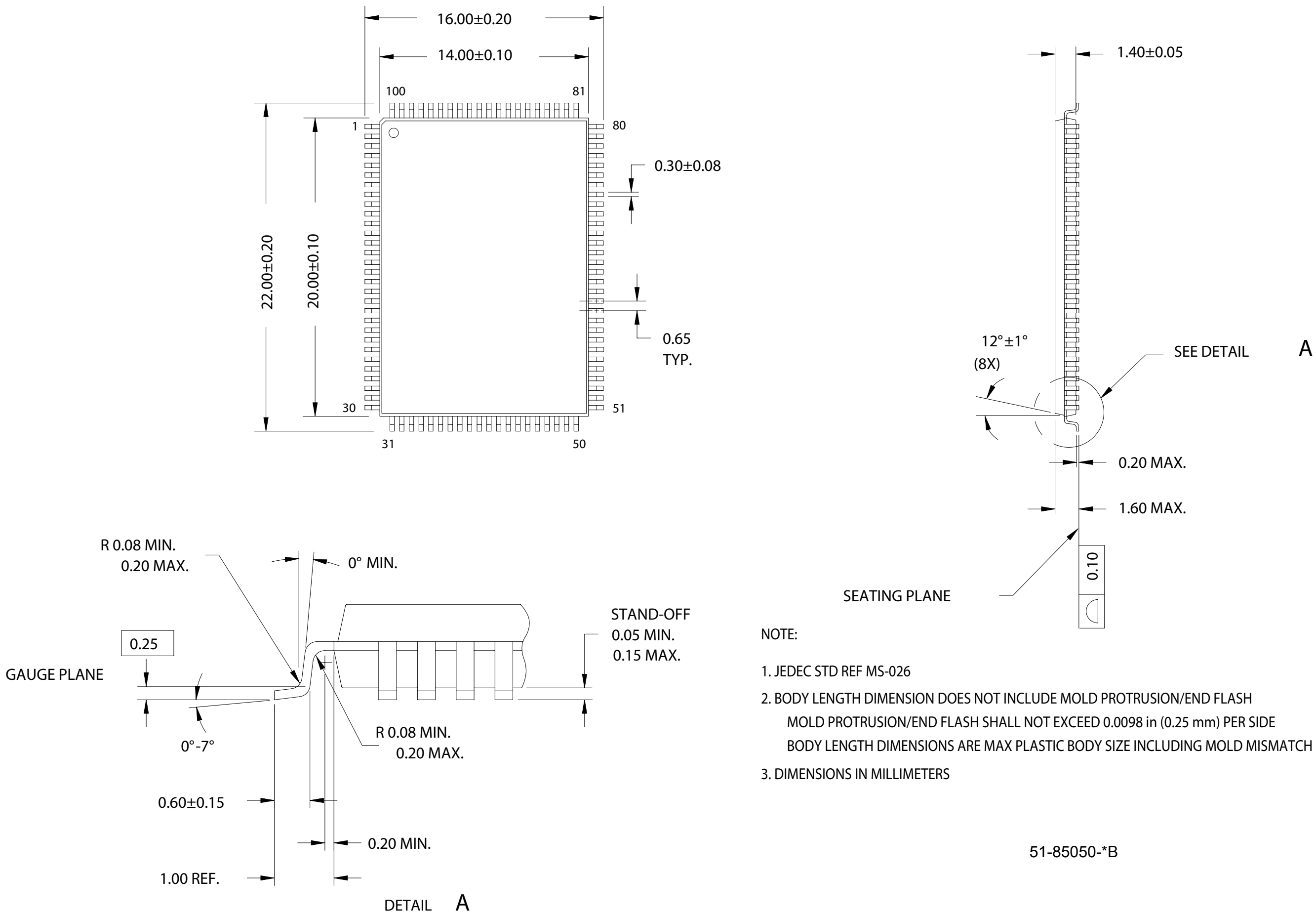
Ordering Information (continued)

Not all of the speed, package, and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

250	CY7C1380DV25-250AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1382DV25-250AXC			
	CY7C1380FV25-250BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1382FV25-250BGC			
	CY7C1380FV25-250BGXC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
	CY7C1382FV25-250BGXC			
	CY7C1380DV25-250BZC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1382DV25-250BZC			
	CY7C1380DV25-250BZXC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1382DV25-250BZXC			
	CY7C1380DV25-250AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1382DV25-250AXI			
	CY7C1380FV25-250BGI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1382FV25-250BGI			
	CY7C1380FV25-250BGXI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
	CY7C1382FV25-250BGXI			
	CY7C1380DV25-250BZI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1382DV25-250BZI			
	CY7C1380DV25-250BZXI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1382DV25-250BZXI			

Package Diagrams

Figure 1. 100-Pin Thin Plastic Quad Flat pack (14 x 20 x 1.4 mm) (51-085050)



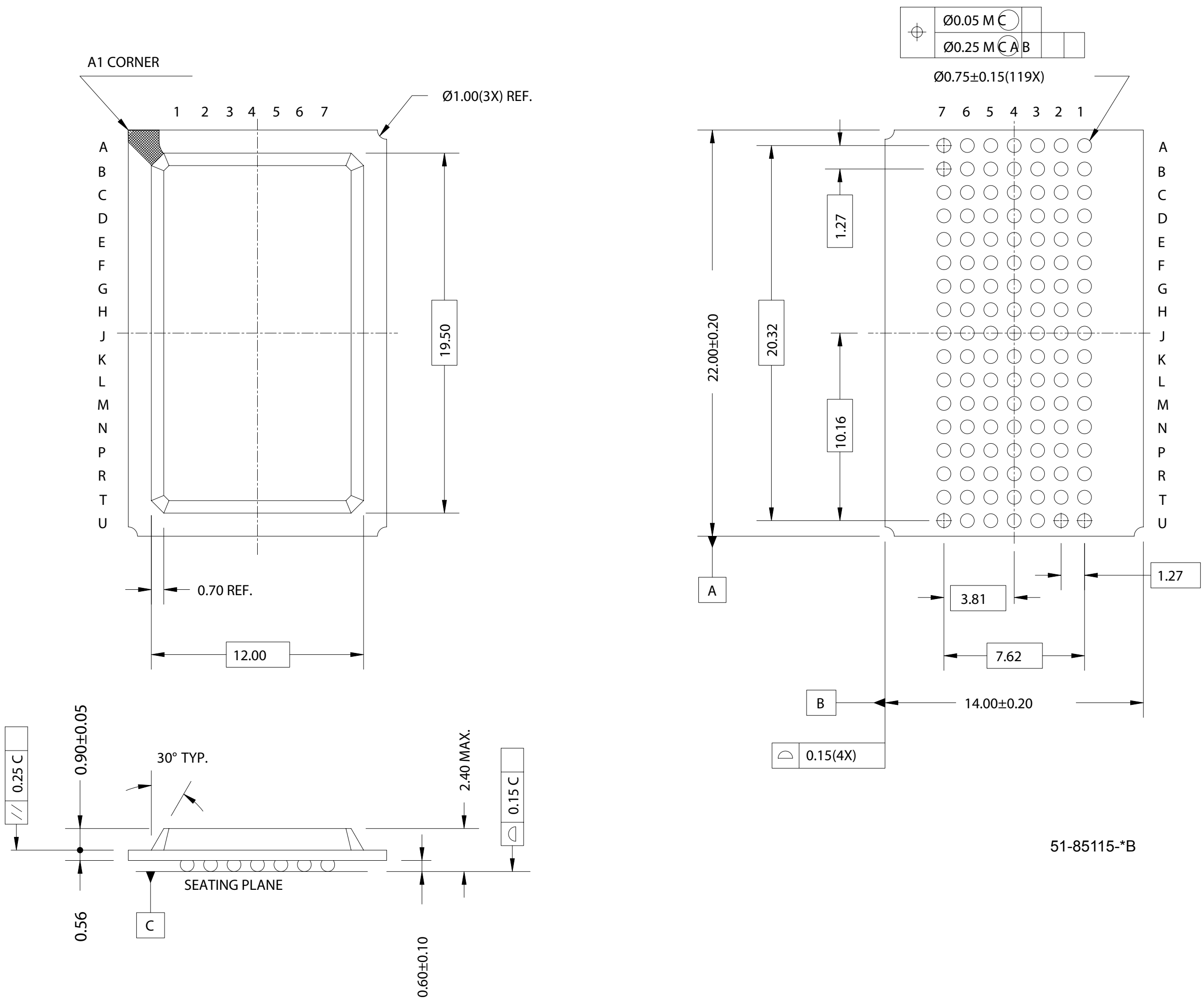
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

Package Diagrams (continued)

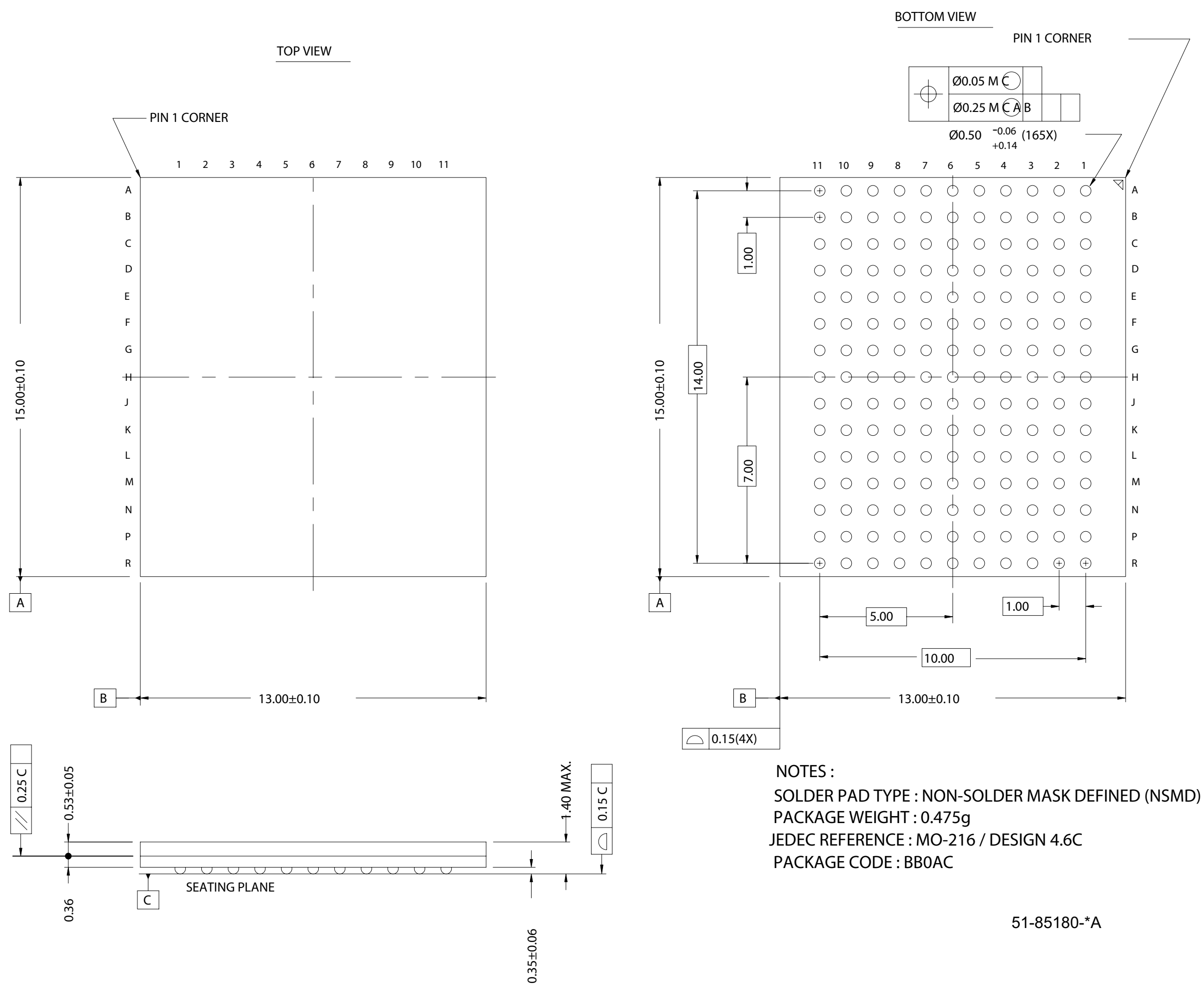
Figure 2. 119-Ball BGA (14 x 22 x 2.4 mm) (51-85115)



[+] Feedback

Package Diagrams (continued)

Figure 3. 165-Ball FBGA (13 x 15 x 1.4 mm) (51-085180)



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Document History Page

Document Title: CY7C1380DV25/CY7C1382DV25/CY7C1380FV25/CY7C1382FV25, 18-Mbit (512K x 36/1M x 18) Pipelined SRAM
Document Number: 38-05546

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	254515	See ECN	RKF	New data sheet
*A	288531	See ECN	SYT	Edited description under “IEEE 1149.1 Serial Boundary Scan (JTAG)” for non-compliance with 1149.1 Removed 225 and 133 Mhz Speed Bin Added Pb-free information for 100-Pin TQFP, 119 BGA and 165 FBGA Packages Added comment of ‘Pb-free BG packages availability’ below the Ordering Information
*B	326078	See ECN	PCI	Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard Added description on EXTEST Outut Bus Tri-State Changed description on the Tap Instruction Set Overview and Extest Changed Device Width (23:18) for 119-BGA from 000000 to 101000 Added seperate row for 165 -FBGA Device Width (23:18) Changed Θ_{JA} and Θ_{JC} for TQFP Package from 31 and 6 °C/W to 28.66 and 4.08 °C/W respectively Changed Θ_{JA} and Θ_{JC} for BGA Package from 45 and 7 °C/W to 23.8 and 6.2 °C/W respectively Changed Θ_{JA} and Θ_{JC} for FBGA Package from 46 and 3 °C/W to 20.7 and 4.0 °C/W respectively Modified $V_{OL,}$ V_{OH} test conditions Removed comment of ‘Pb-free BG packages availability’ below the Ordering Information Updated Ordering Information Table
*C	418125	See ECN	NXR	Converted from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Changed the description of I_X from Input Load Current to Input Leakage Current on page# 18 Changed the I_X current values of MODE on page # 18 from –5 µA and 30 µA to –30 µA and 5 µA Changed the I_X current values of ZZ on page # 18 from –30 µA and 5 µA to –5 µA and 30 µA Changed $V_{IH} \le V_{DD}$ to $V_{IH} < V_{DD}$on page # 18 Replaced Package Name column with Package Diagram in the Ordering Information table Updated Ordering Information Table
*D	475009	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND Changed t_{TH}, t_{TL} from 25 ns to 20 ns and t_{TDOV} from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*E	793579	See ECN	VKN	Added Part numbers CY7C1380FV25 and CY7C1382FV25 Added footnote# 3 regarding Chip Enable Updated Ordering Information table