

# HD153009, HD153013

## 2-7 Code Encoder/Decoder

### Description

The HD153009/HD153013 2-7 encoder/decoder IC for magnetic disks converts an NRZ signal to be written to a magnetic disk into a 2-7 code, and converts a 2-7 code read from the disk into an NRZ signal.

This IC incorporates phase comparator logic for the data separator. In combination with a data separator chip, this IC performs two functions: 2-7 modulation/demodulation and data separation.

### Features

- Encode/decode IBM 2-7 codes
- Can generate and detect address marks using soft sector approach.
- Can synchronize phases in 4T (1000) SYNC pattern.
- Built-in phase comparison logic for data separation
- Built-in sync field detection logic
- Maximum data transfer rate: 15 Mbps
- LSTTL-compatible inputs/outputs
- Small 44-pin MSP package suitable for surface mounting
- Single 5 V power supply

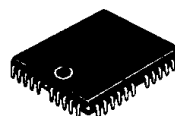
### Functions

- NRZ signal to 2-7 code conversion
- 2-7 code to NRZ signal conversion
- Write precompensation
- Phase synchronization in 4T(1000) SYNC pattern
- Address mark(DC erase) generation
- Address mark(DC erase) detection
- Phase comparison for data separator
- Sync field detection

### Ordering Information

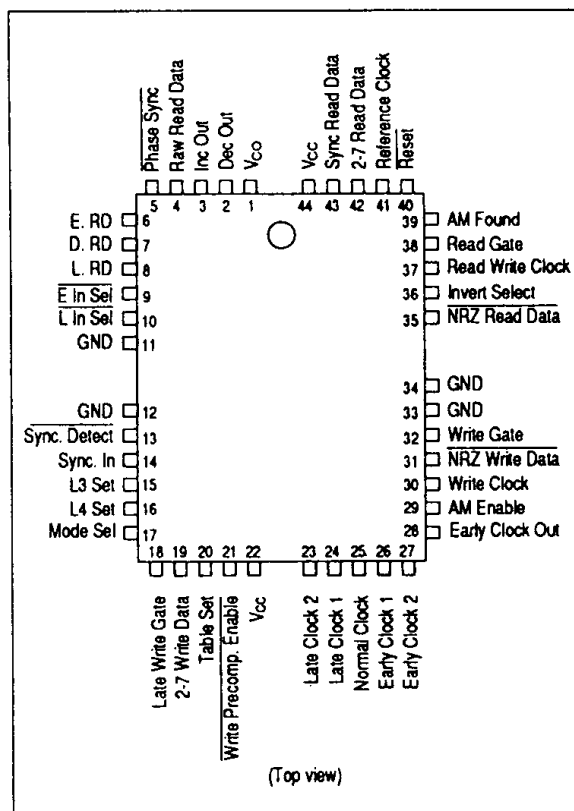
| Type No.              | Package |
|-----------------------|---------|
| HD153009,<br>HD153013 | MP-44   |

HD153009, HD153013

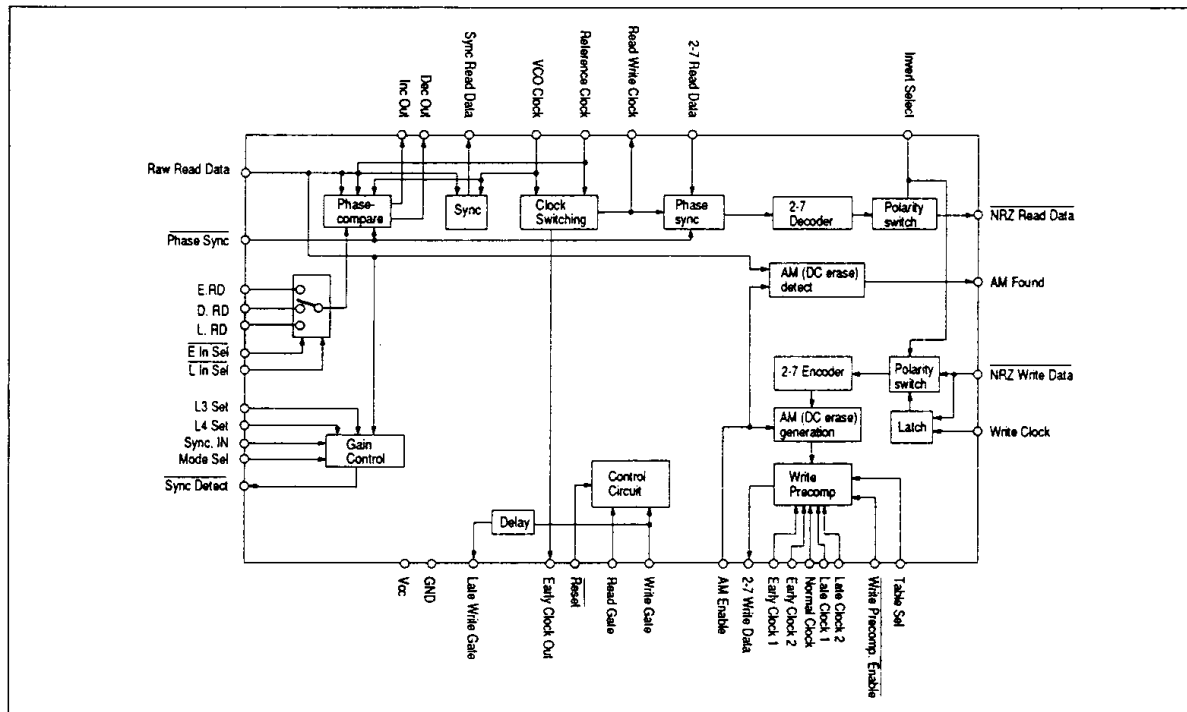


(MP-44)

### Pin Arrangement



## Block Diagram



**Table 1 Pin Description**

| Pin No.     | Pin name                        | Input/output |
|-------------|---------------------------------|--------------|
| 22,24       | Vcc                             | Power        |
| 11,12,33,34 | GND                             | Power        |
| 42          | 2-7 Read data                   | In           |
| 1           | VCO clock                       | In           |
| 38          | Read gate                       | In           |
| 41          | Reference clock                 | In           |
| 31          | NRZ write data                  | In           |
| 32          | Write gate                      | In           |
| 21          | Write precomp. enable           | In           |
| 27          | Early clock 2                   | In           |
| 26          | Early clock 1                   | In           |
| 25          | Normal clock                    | In           |
| 24          | Late clock 1                    | In           |
| 23          | Late clock 2                    | In           |
| 5           | Phase sync.                     | In           |
| 29          | AM enable (Address mark enable) | In           |
| 40          | Reset                           | In           |
| 20          | Table sel                       | In           |
| 36          | Invert select                   | In           |
| 4           | Raw read data                   | In           |

| Pin No. | Pin name                      | Input/output |
|---------|-------------------------------|--------------|
| 7       | D.RD (Delayed read data)      | In           |
| 14      | Sync. in                      | In           |
| 17      | Mode sel                      | In           |
| 9       | E in sel                      | In           |
| 6       | E.RD (E read data)            | In           |
| 10      | L in sel                      | In           |
| 8       | L. RD (L head data)           | In           |
| 15      | L3 set                        | In           |
| 16      | L4 set                        | In           |
| 30      | Write clock                   | In           |
| 35      | NRZ read data                 | Out          |
| 19      | 2-7 write data                | Out          |
| 39      | AM found (Address mark found) | Out          |
| 37      | Read write clock              | Out          |
| 28      | Early clock out               | Out          |
| 18      | Late write gate               | Out          |
| 3       | Inc out                       | Out          |
| 2       | Dec out                       | Out          |
| 43      | Sync. read data               | Out          |
| 13      | Sync. detect                  | Out          |

## Pin Function

### 2-7 Read Data

The 2-7 Read Data pin inputs the 2-7 code from the disk. The signal synchronized in the data separator is applied to this pin. It must also be synchronized to the VCO Clock from the data separator. When using the internal phase comparator, input the Sync Read Data signal to this pin.

### VCO Clock

The VCO Clock is input from a data separator, which has synchronized it with the 2-7 Read Data. The internal phase comparator compares this signal with the Delayed Read Data.

### Read Gate

Setting Read Gate input high permits the HD153009 to read data from the disk. It converts the 2-7 code read from the disk into NRZ data for output. Read Gate activates the gain control circuit, performs phase comparison, switches internal circuit clocks, and enables NRZ signal output.

### Reference Clock

Reference Clock is the reference clock for this IC. It is also the write data clock. Its frequency must be twice the data transfer rate.

### NRZ Write Data

NRZ Write Data inputs NRZ data to be written to the disk. It must be input synchronously with the Write Clock signal when E In Sel and L In Sel pins are set low. Otherwise it must be set synchronously with the Read Write Clock. The polarity of this signal can be switched by the Invert Select pin. Invert Select high selects inverted input and Invert Select low selects noninverted input for 2-7 conversion.

### Write Gate

Write Gate high allows data write; NRZ data to be written to the disk is converted to 2-7 code for output. Set Write Gate high for soft-sector address mark write and low for address detection.

### Write Precomp. Enable

Setting Write Precomp. Enable low enables write precompensation during writes. In this case, provide a write precompensation clock signal.

### Early Clock 2

The phase of the Early Clock 2 write precompensation clock input must lead the Normal Clock.

### Early Clock 1

The phase of the Early Clock 1 write precompensation clock input must lead the Normal Clock and follow Early Clock 2.

### Normal Clock

The Normal Clock input is used for write precompensation.

### Late Clock 1

Late Clock 1 input is used for write precompensation according to write precompensation table 2. Its phase must follow the Normal Clock signal.

### Late Clock 2

The Late Clock 1 write precompensation input must follow the Normal Clock and lead Late Clock 1.

### Phase Sync

Setting Phase Sync low at the beginning of a read allows 2-7 read data phase to be synchronized in 4T (1000) SYNC pattern (the phase comparator is placed in frequency/phase comparison mode). After synchronization, Phase Sync must be set high for normal decoding. Normally, input Sync Det. to this pin.

### AM Enable (Address Mark Enable)

Setting AM Enable input high allows soft-sector address mark write and detection. During address mark write, DC erase continues while AM Enable and Write Gate are held high. If an address mark is detected, the AM Found signal is output at the completion of DC erase, which continues for at least 30 Reference Clock periods. When the AM Found signal is output, the disk controller must clear Address Mark Enable.

**Reset**

A low-level  $\overline{\text{Reset}}$  input initializes the internal circuits at power on. Hold Reset high for normal operation.

**Table Sel**

Table Sel input high selects write precompensation table 1, and Table Sel input low selects write precompensation table 2.

**Invert Select**

Invert Select input switches the NRZ polarity for the interface with the controller. When Invert Select is high, the NRZ signal is inverted. When Invert Select is low, the NRZ signal input/output is noninverted.

**Raw Read Data**

Raw Read Data inputs the 2-7 code read from the disk before it is synchronized in the separator. It is input to the internal comparator for the PLL.

**D. RD (Delayed Read Data)**

D. RD input is delayed by a period of half the NRZ data transfer rate from the Raw Read Data. It is delivered to the internal comparator for the PLL.

**Sync. In**

Sync. In input goes to the sync field detect gain control circuit. When the gain control circuit is in normal mode, input the Read Gate signal to Sync. In. When it is in frequency verify mode, input the one-shot output activated by the Raw Read Data signal.

**Mode Sel**

Mode Sel input selects the mode of the sync field detect gain control circuit. Mode Sel low specifies normal mode, and Mode Sel high specifies frequency verify mode.

 **$\overline{\text{E In Sel}}$** 

$\overline{\text{E In Sel}}$  input low inputs the E. RD signal instead of the D. RD signal into the internal phase comparator for the PLL. When  $\overline{\text{E In Sel}}$  and  $\overline{\text{L In Sel}}$  are low, the  $\overline{\text{NRZ Write Data}}$  signal is synchronized with the Write Clock.

**E. RD (E Read Data)**

When E In Sel input is low, input the E. RD signal instead of the D. RD signal into the internal phase comparator for the PLL.

 **$\overline{\text{L In Sel}}$** 

Setting the  $\overline{\text{L In Sel}}$  input low inputs the L. RD signal instead of the D. RD signal into the internal phase comparator for the PLL. When  $\overline{\text{E In Sel}}$  and  $\overline{\text{L In Sel}}$  are low, the  $\overline{\text{NRZ Write Data}}$  signal is synchronized with the Write Clock.

**L. RD (L Read Data)**

When  $\overline{\text{L In Sel}}$  input is low, input the L. RD signal instead of the D. RD signal into the internal phase comparator for the PLL.

**L3 Set, L4 Set**

L3 Set and L4 Set input specify the  $\overline{\text{Sync. Detect}}$  output period for the sync field detection gain control circuit (table 1. ).

**Write Clock**

Write Clock input enables the  $\overline{\text{NRZ Write Data}}$  signal. It is valid while both  $\overline{\text{E In Sel}}$  and  $\overline{\text{L In Sel}}$  are kept low.

 **$\overline{\text{NRZ Read Data}}$** 

$\overline{\text{NRZ Read Data}}$  outputs the NRZ signal converted from a 2-7 code read from the disk. This signal is synchronous with the Read Write Clock. The polarity can be switched by the Invert Select pin. Invert Select high selects inverted output, and Invert Select low specifies noninverted output.

**2-7 Write Data**

2-7 Write Data outputs 2-7 codes converted from NRZ signals to write to disk.

**AM Found (Address Mark Found)**

AM Found goes high when the HD153009 detects an address mark in a soft sector. It is valid only when AM Enable is high.

**Table 2 Output Period**

| L3 Set | L4 Set | Period  |
|--------|--------|---------|
| High   | High   | 6 Bytes |
|        | Low    | 2 Bytes |
| Low    | High   | 4 Bytes |
|        | Low    | 4 Bytes |

**Table 3 NRZ Signal to from 2-7 Code Conversion**

| NRZ Code | NRZ Code | 2-7 Code        |
|----------|----------|-----------------|
| 0 1      | 1 0      | 0 1 0 0         |
| 1 0 1    | 0 1 0    | 1 0 0 1 0 0     |
| 1 1 0 1  | 0 0 1 0  | 0 0 1 0 0 1 0 0 |
| 0 0      | 1 1      | 1 0 0 0         |
| 1 0 0    | 0 1 1    | 0 0 1 0 0 0     |
| 1 1 0 0  | 0 0 1 1  | 0 0 0 0 1 0 0 0 |
| 1 1 1    | 0 0 0    | 0 0 0 1 0 0     |

**Read Write Clock**

For data read, Read Write Clock outputs a clock signal synchronous to the converted NRZ signal. For data write, it outputs a clock signal divided by the Reference Clock signal. The disk controller must enable NRZ Read Data (for reads) and NRZ Write Data (for writes) synchronously with Read Write Clock.

**Early Clock Out**

Connect the Early Clock Out write precompensation reference clock output directly to the Early Clock 2 pin.

**Late Write Gate**

The rising edge of the Late Write Gate signal is delayed about 32 Reference Clock periods from the start of writing. During Late Write Gate output, the 2-7 Write Data signal is output normally.

**Inc Out**

The Inc Out internal comparator signal is output when Read Data phase leads the VCO Clock phase. This signal is passed to the PLL charge pump.

**Dec Out**

The Dec Out internal comparator signal is output when Read Data phase follows the VCO Clock phase. This signal is passed to the PLL charge pump.

**Sync. Read Data**

Sync. Read Data outputs the 2-7 Read Data signal phase-synchronized with the PLL, which was synchronized to the VCO Clock signal. It is provided to the 2-7 Read Data pin for 2-7 reverse conversion.

**Sync. Detect**

The Sync. Detect sync field detect gain control circuit output is normally sent to the Phase Sync. pin. While Sync. Detect is output, the voltage can be quickly stabilized to the PLL voltage by increasing the PLL gain.

**Vcc, GND**

Vcc supplies the +5 V power. Both Vcc pins must be connected to the power line. All four GND ground pins must be directly grounded separately from each other.

## Functional Description

### NRZ Signal to 2-7 Code Conversion

The NRZ write signal is converted into a 2-7 code to be written to the disk. Either the  $\overline{\text{NRZ}}$  or NRZ signal is selected depending on the Invert Select pin input level; a high level Invert Select the  $\overline{\text{NRZ}}$  signal and a low level selects NRZ. The NRZ write signal is synchronized with the Read Reference Clock signal and then converted into a 2-7 code according to the conversion Table 2. The resulting 2-7 code is subject to write precompensation.

### 2-7 Code to NRZ Signal Conversion

The 2-7 code read from the disk is converted into an NRZ signal;  $\overline{\text{NRZ}}$  or NRZ signal is also selected by the Invert Select signal. The 2-7 code is synchronized with the VCO Clock signal and then converted into an NRZ signal based on the conversion table. The NRZ read signal is synchronized with the read clock signal.

### Write Precompensation

The converted 2-7 write code (Figure 1) is subject to write precompensation according to Table 3 or 4.

Table Sel pin chooses either write precompensation table 1 (high level) or write precompensation table 2 (low level).

The amount of write precompensation is determined by the phase of the externally supplied clock signal.

When the  $\overline{\text{Write Precomp. Enable}}$  is high level and the Table Sel is high level, the HD153013 activates write-precompensation in table 1 by the built-in delay, and in the other hand, the HD153009 does not activate write-precompensation. (Refer to Table 5)

When the  $\overline{\text{Write Precomp. Enable}}$  is high level and the Table Sel is low level, the HD153009 activates write-precompensation in table 2 by the built-in delay, and in the other hand, the HD153013 does not activate write-precompensation. (Refer to Table 5)

### Phase Synchronization in 4T (1000) SYNC Pattern

When data is being read from a magnetic disk, the clock phase can be synchronized in 4T (1000) SYNC pattern. In this case, for NRZ signal selection, "11 ... 111" data must be in the SYNC field and "00 ... 000" for  $\overline{\text{NRZ}}$  signal. During read, the synchronous signal is applied, during which the phase is synchronized.

### Address Mark (DC Erase) Generation

The 2-7 write signal change is halted by the address mark generation signal. The address mark continues to be written while the address mark generation signal is applied.

### Address Mark (DC Erase) Detection

The AM detection signal is output following the address mark when the 2-7 read signal remains unchanged for a period exceeding 16 bits of data.

### Phase Comparison for the Data Separator

This device incorporates a phase comparator for the data separator (HA16658). This comparator compares Raw Read Data and Delayed Read Data with VCO Clock phase to provide phase comparison signal Inc Out or Dec Out as follows:

- When Read Data phase leads the VCO Clock phase, Inc Out is output.
- When Read Data phase follows the VCO Clock phase, Dec Out is output.

When the  $\overline{\text{Phase Sync. pin}}$  is set low, frequency as well as phase are compared between the Read Data and VCO Clock signals. Accordingly, this comparator can be effectively used to stabilize the voltage to the PLL in sync field. The Read Data in sync field is assumed to be 4T (1000).

The  $\overline{\text{Phase Sync. pin}}$  input can be appropriately delivered from the  $\overline{\text{Sync. Detect}}$  signal output by the built-in gain control circuit.

### Gain Control Circuit

The gain control circuit outputs the  $\overline{\text{Sync. Detect}}$  signal during SYNC field. Using L3 Set and L4 set input pins, the  $\overline{\text{Sync. Detect}}$  signal output period can be selected from among 2-, 4-, and 6-byte lengths of the NRZ signal (see Table 6).

**Table 4 Write Precompensation Table 1**

| n\m | 2  | 3  | 4  | 5  | 6  | 7  |
|-----|----|----|----|----|----|----|
| 2   | N  | E2 | E2 | E2 | E2 | E2 |
| 3   | L2 | E1 | E1 | E1 | E1 | E1 |
| 4   | L2 | E1 | E1 | E1 | E1 | E1 |
| 5   | L2 | E1 | E1 | E1 | E1 | E1 |
| 6   | L2 | E1 | E1 | E1 | E1 | E1 |
| 7   | L2 | E1 | E1 | E1 | E1 | E1 |

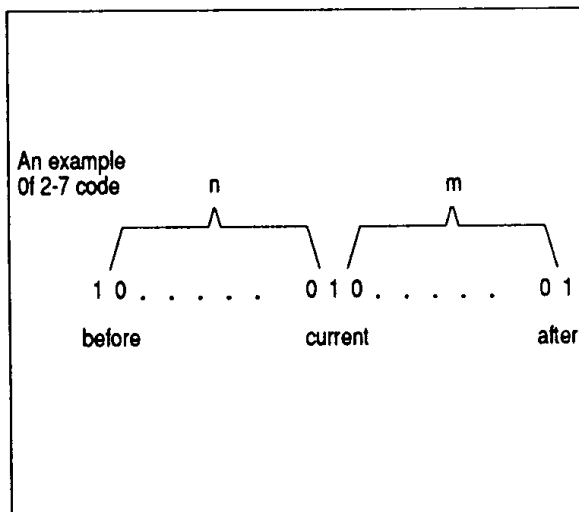
**Table 5 Write Precompensation Table 2**

| n\m | 2  | 3  | 4  | 5  | 6  | 7  |
|-----|----|----|----|----|----|----|
| 2   | N  | E1 | E2 | E2 | E2 | E2 |
| 3   | L1 | N  | E1 | E1 | E1 | E1 |
| 4   | L2 | L1 | N  | N  | E1 | E1 |
| 5   | L2 | L1 | N  | N  | N  | N  |
| 6   | L2 | L1 | L1 | N  | N  | N  |
| 7   | L2 | L1 | L1 | N  | N  | N  |

Note: N: Normal Clock, L2: Late Clock 2, L1: Late Clock 1, E2: Early Clock 2, E1: Early Clock 1, |L2| > |L1|, |E2| > |E1|

**Table 6 Selection of Precompensation Mode**

| Write Precomp. Enable Table Sel | Write Precompensation Table Select |          | Precompensation Method |                        |                        |
|---------------------------------|------------------------------------|----------|------------------------|------------------------|------------------------|
|                                 | HD153009                           | HD153013 | HD153009               | HD153013               |                        |
| L                               | H                                  | 1        | 1                      | External delay element | External delay element |
| L                               | L                                  | 2        | 2                      | External delay element | External delay element |
| H                               | H                                  | —        | 1                      | No precompensation     | Built-in delay         |
| H                               | L                                  | 2        | —                      | Built-in delay         | No precompensation     |



**Figure 1 2-7 Code Example**

**Table 7 Selection of Sync Detect Period**

|                    |         |         |         |         |
|--------------------|---------|---------|---------|---------|
| L3 set             | High    | High    | Low     | Low     |
| L4 set             | High    | Low     | High    | Low     |
| Sync detect period | 6 Bytes | 2 Bytes | 4 Bytes | 4 Bytes |

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This circuit has two modes switched via the Mode Sel pin: normal mode (Mode Sel at high) and frequency verification mode (Mode Sel at low).

**Normal mode:** The Read Gate signal from the controller must be input to the Sync In pin. Immediately after the rising edge of the Read Gate signal, the Sync. Detect signal is set to low during the period specified by the L3 Set and L4 Set pins.

**Frequency verification mode:** 1 shot output activated by the Raw Read Data signal must be provided to the Sync In pin. If the 1 shot output is

not held low during a 2-bytes NRZ signal after the falling Read Gate signal, the Sync. Detect signal must be set to low. The Sync. Detect signal output period is specified by L3 Set and L4 Set pins.

The Sync. Detect signal must be applied to the Phase Sync. pin of this IC to enable the phase comparator to compare phases and frequencies and to synchronize the phase for read. By providing the Sync. Detect signal to the HA16658's GS pin, PLL gain can be increased.

**Table 8 Absolute Maximum Ratings (Ta=25°C)**

| Item                  | Symbol | Rating      | Unit |
|-----------------------|--------|-------------|------|
| Supply voltage        | Vcc    | 7           | V    |
| Input voltage         | Vi     | 5.5         | V    |
| Output voltage        | Vo     | 5.5         | V    |
| Power consumption     | Pc     | 460         | mW   |
| Operating temperature | Topr   | -20 to +75  | °C   |
| Storage temperature   | Tstg   | -65 to +150 | °C   |

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

**Table 9 Electrical Characteristics**

**Table 9-1 DC Characteristics (Ta=20 to +75°C)**

| Item                      | Symbol | Min  | Typ | Max  | Unit | Test Conditions            |
|---------------------------|--------|------|-----|------|------|----------------------------|
| Supply voltage            | Vcc    | 4.75 | 5.0 | 5.25 | V    |                            |
| Input high level voltage  | VIH    | 2.0  |     |      | V    |                            |
| Input low level voltage   | VIL    |      |     | 0.8  | V    |                            |
| High level input current  | IiH    |      |     | 20   | μA   | Vcc = 5.25 V, Vi = 2.7 V   |
| Low level input current   | IiL    |      |     | -400 | μA   | Vcc = 5.25 V, Vi = 0.4 V   |
| Output high level voltage | VOH    | 2.7  |     |      | V    | Vcc = 4.75 V, IOH = 400 μA |
| Output low level voltage  | VOL    |      |     | 0.5  | V    | Vcc = 4.75 V, IOL = 8 mA   |
| High level output current | IOH    |      |     | -400 | μA   |                            |
| Low level output current  | IOL    |      |     | 8    | mA   |                            |
| Off-state output current  | IOZH   |      |     | 20   | μA   | Vcc = 5.25 V, Vo = 2.7 V   |
|                           | IOZL   |      |     | -20  | μA   | Vcc = 5.25 V, Vo = 0.4 V   |





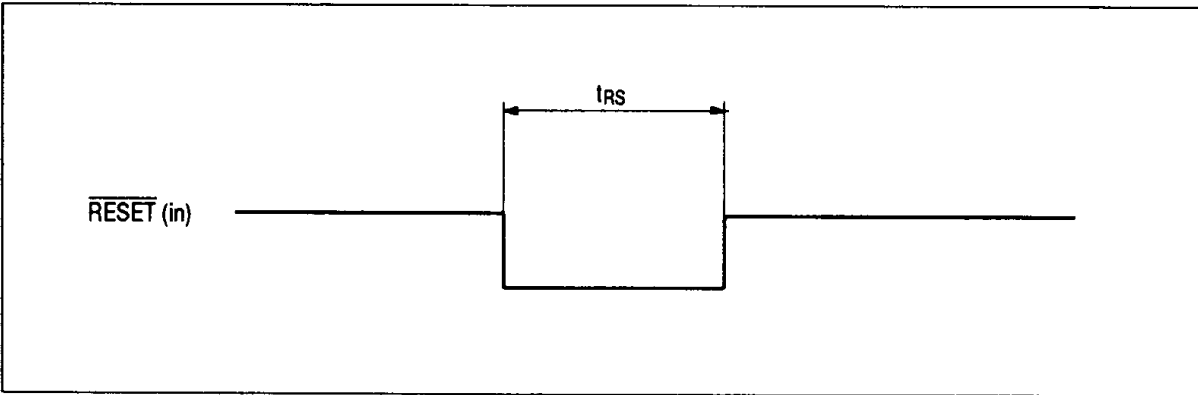
**Table 9-2 AC Characteristics (Ta=25°C)**

| Item  | Symbol | Min | Typ | Max | Unit                | Test Conditions                                   | Note                 |
|---|--------|-----|-----|-----|---------------------|---|----------------------|
| Input clock frequency                           |        |     |     | 30  | MHz                 |   | Reference /VCO clock |
| Data transfer rate                              |        |     |     | 15  | Mbps                |   |                      |
| Reset time                                      | trs    | 50  |     |     | ns                  | Fig. 2  |                      |
| 2-7 read data set-up time                       | tsr    | 15  |     |     | ns                  | Fig. 3  |                      |
| 2-7 read data hold time                         | thr    | 10  |     |     | ns                  | Fig. 3  |                      |
| NRZ read data set-up time                       | tsnr   | 45  |     |     | ns                  | Fig. 4 at 10 Mbps                                 |                      |
| NRZ read data hold time                         | thnr   | 35  |     |     | ns                  | Fig. 4 at 10 Mbps                                 |                      |
| Decode time                                     | tdd    |     | 7   |     | VCO clock           | Fig. 5  |                      |
| Phase sync. time                                | tps    |     |     | 3   | 2-7 Read data pulse | Fig. 6  |                      |
| Early clock out to precomp. clock               | tlwp   |     |     | 30  | ns                  | Fig. 7  |                      |
| Read data delay                                 | tdpc   |     | 25  |     | ns                  | Fig. 8 at 10 Mbps                                 |                      |
| Sync. read data set-up time                     | tssr   | 15  |     |     | ns                  | Fig. 9  |                      |
| Sync. read data hold time                       | thsr   | 10  |     |     | ns                  | Fig. 9  |                      |
| Write clock to read clock                       | twtr   |     |     | 5   | VCO clock           | Fig. 10 VCO clock period = Reference clock period |                      |
| Read clock to write clock                       | trtw   |     |     | 5   | Ref. clock          | Fig. 10 VCO clock period = Reference clock period |                      |
| NRZ write data set-up time                      | tsnw   | 10  |     |     | ns                  | Fig. 11   |                      |
| NRZ write data hold time                        | thnw   | 10  |     |     | ns                  | Fig. 11   |                      |
| Encode time                                     | ted    |     | 7   |     | Ref. clock          | Fig. 12 No write precomp.                         |                      |
|   |        |     | 16  |     | Ref. clock          | Fig. 12 With write precomp.                       |                      |
| Write gate to late write Gate (high)            | TLWG   | 30  |     | 32  | Ref. clock          | Fig. 13   |                      |
| Write gate to late write Gate (low)             | TRWG   |     |     | 20  | ns                  | Fig. 13   |                      |
| Address mark write enable time                  | taml   |     |     | 2   | Ref. clock          | Fig. 14   |                      |
| Address mark write disable time                 | tamh   |     |     | 2   | Ref. clock          | Fig. 14   |                      |
| Address mark detect time                        | tamr   | 30  |     |     | Ref. clock          | Fig. 15   |                      |
| Address mark detect rise time                   | tafh   |     |     | 30  | ns                  | Fig. 15   |                      |
| Address mark detect fall time                   | tافل   |     |     | 30  | ns                  | Fig. 15   |                      |
| Sync detect fall time                           | tsdd   |     |     | 40  | ns                  | Fig. 16   |                      |
| Sync. detect time (normal mode)                 | tsdt   |     | 17  |     | Raw read data       | Fig. 16 at 4 bytes                                |                      |
| Sync. detect fall time                          | tsdd   |     | 8   |     | Raw read data       | Fig. 17   |                      |
| Sync. detect time (frequency verification mode) | tsdt   |     | 17  |     | Raw read data       | Fig. 17 at 4 bytes                                |                      |

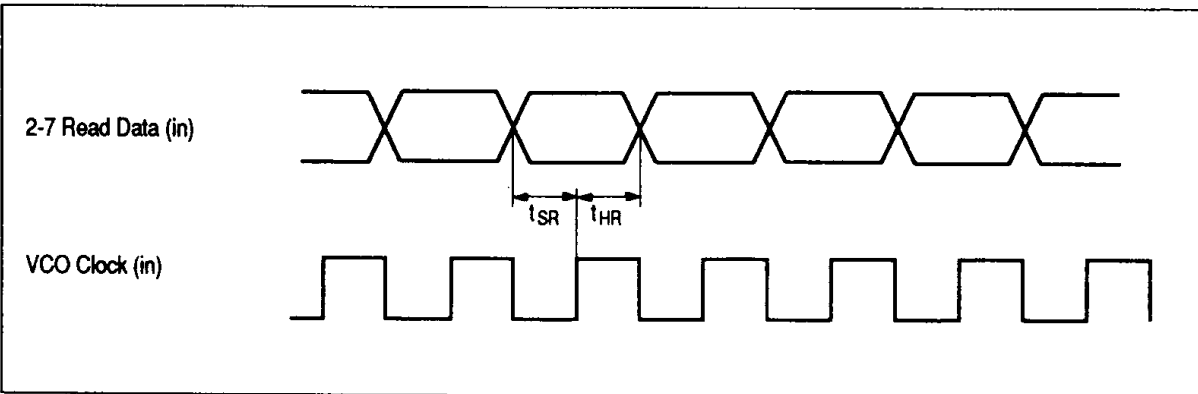
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## AC Characteristics (Ta=25°C) (cont)

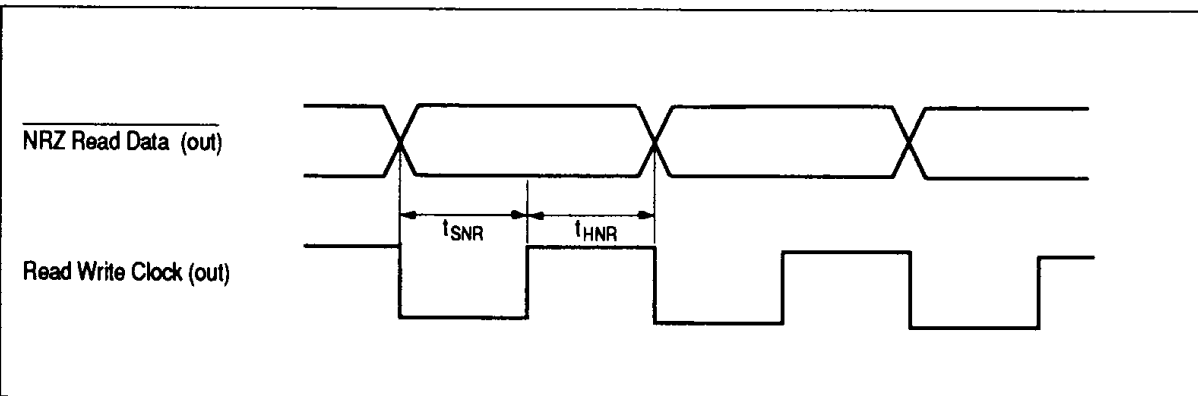
|                   |          |    |    |                                    |
|-------------------|----------|----|----|------------------------------------|
| Internal delay E1 | $t_{E2}$ | -7 | ns | Delay with respect to normal clock |
| Internal delay E2 | $t_{E1}$ | -4 | ns |                                    |
| Internal delay L1 | $t_{L2}$ | 4  | ns |                                    |
| Internal delay L1 | $t_{L2}$ | 7  | ns |                                    |



**Figure 2 Reset Input**

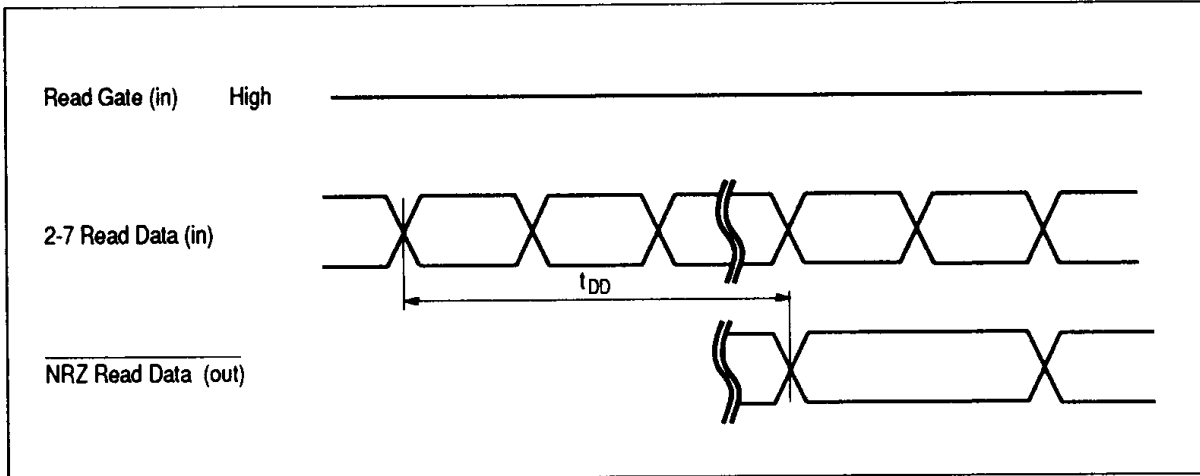


**Figure 3 2-7 Read Data**

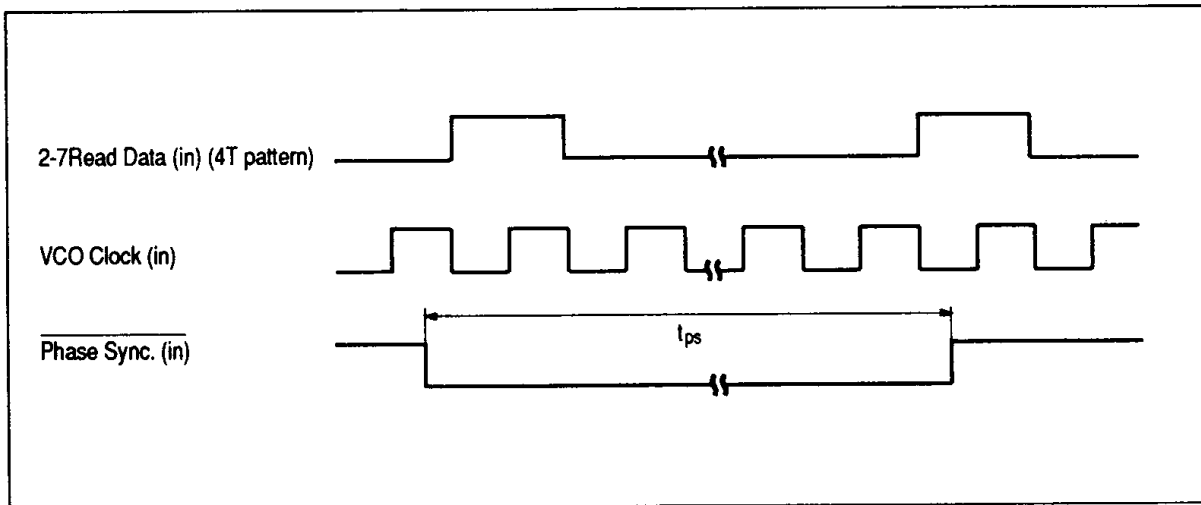


**Figure 4 NRZ Read Data**

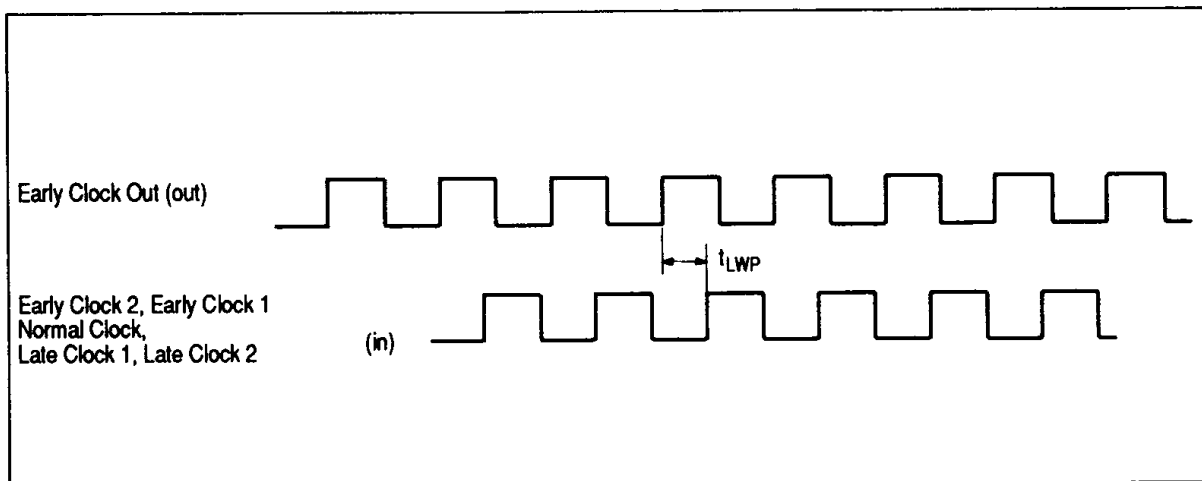




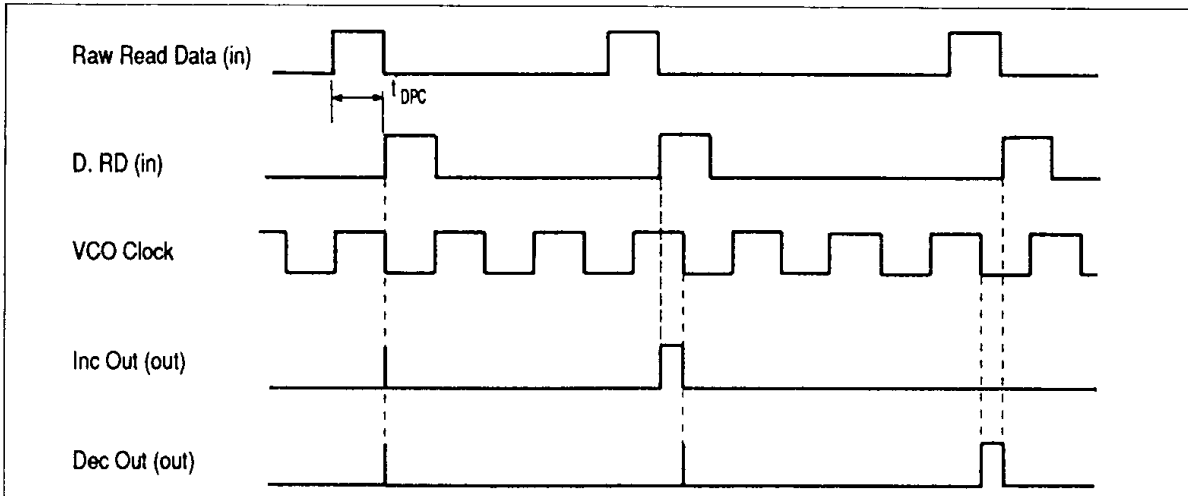
**Figure 5 Decode**



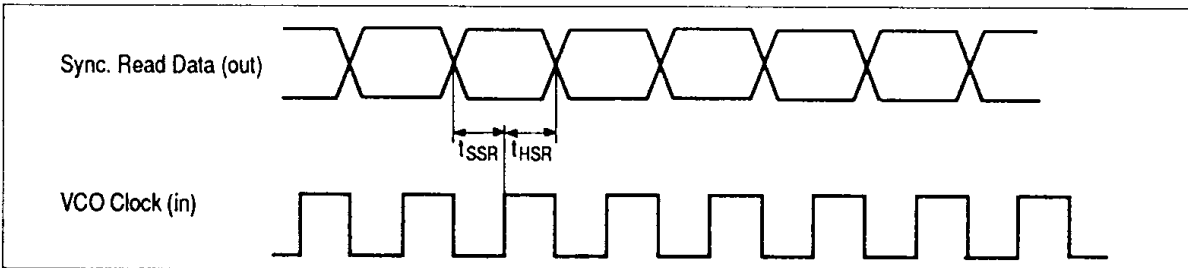
**Figure 6 Phase Synchronization**



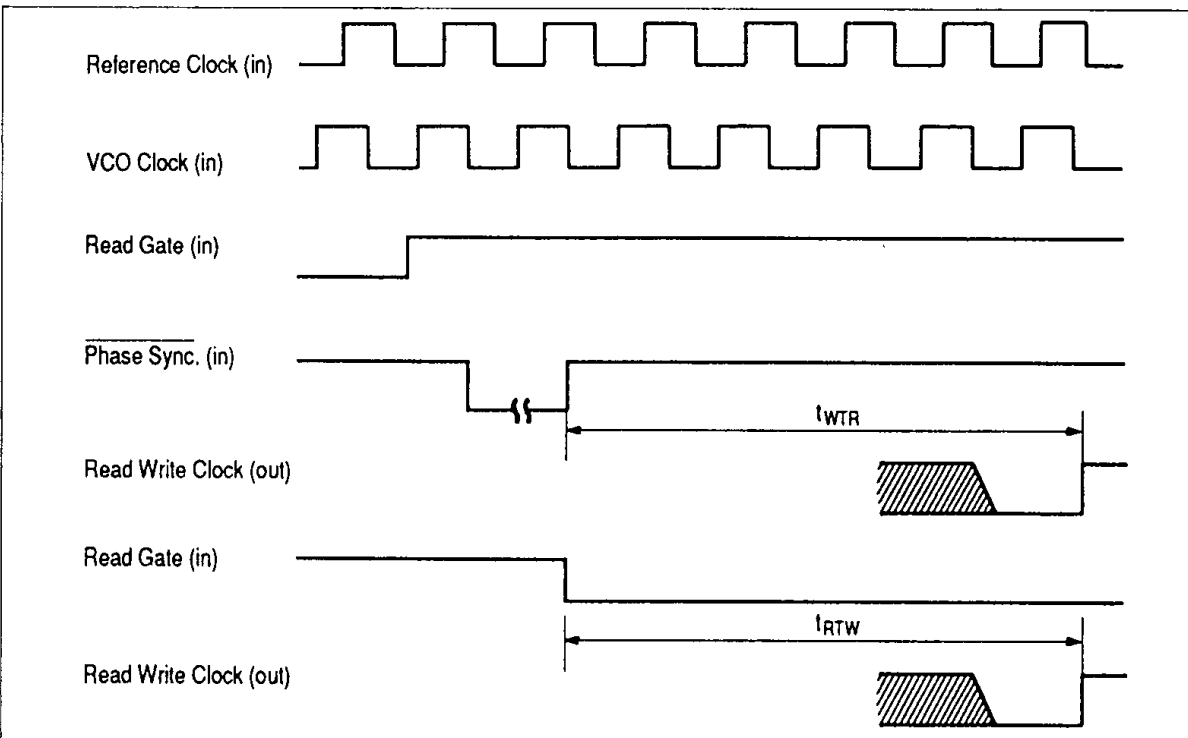
**Figure 7 Write Precompensation**



**Figure 8 Phase Comparison**



**Figure 9 Sync. Read Data**



**Figure 10 Read Write Clock**

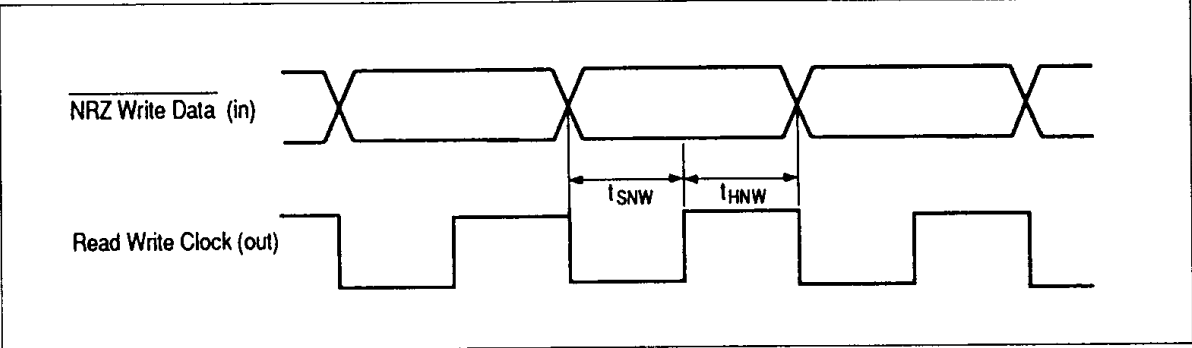


Figure 11 NRZ Write Data Input

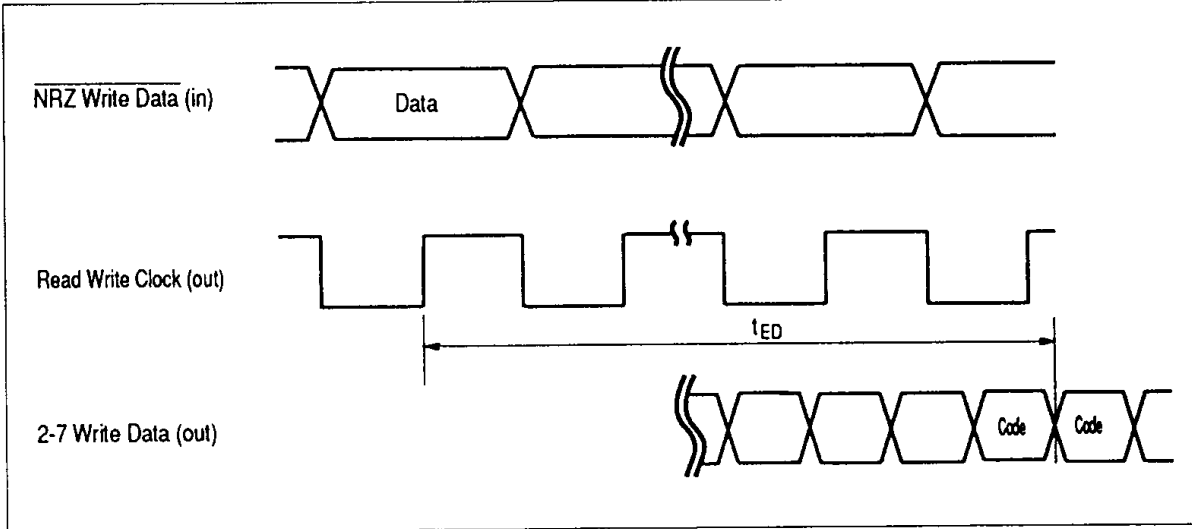


Figure 12 Encode

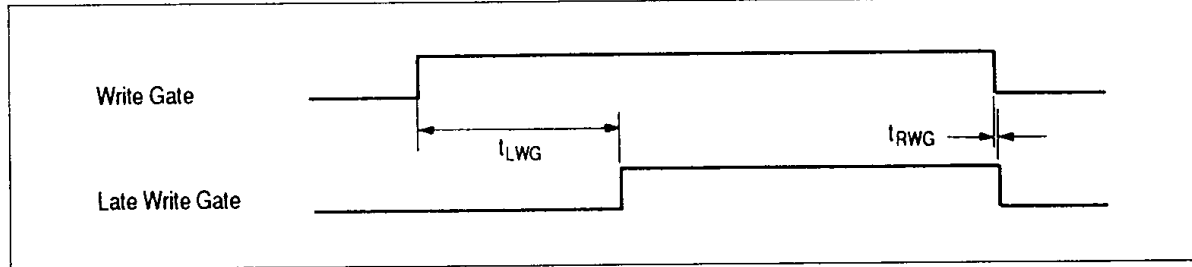


Figure 13 Late Write Gate

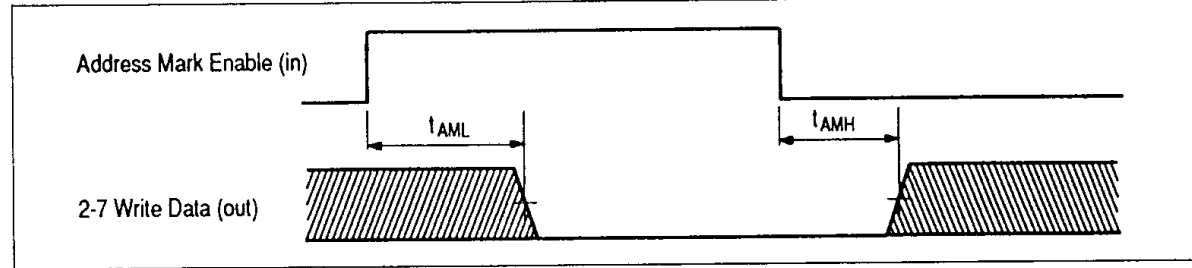


Figure 14 Address Mark Write



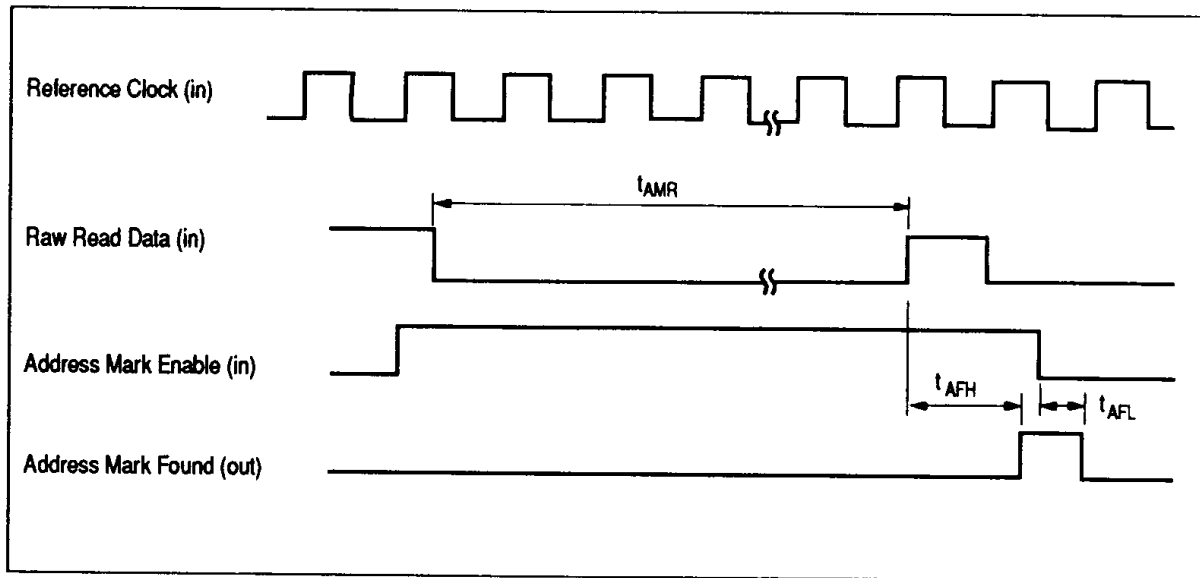


Figure 15 Address Mark Detect

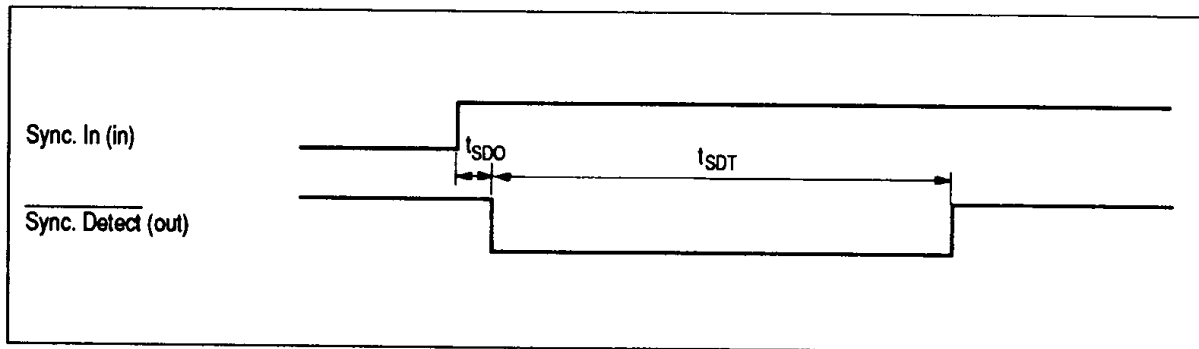


Figure 16 Sync Detect Output(Normal Mode)

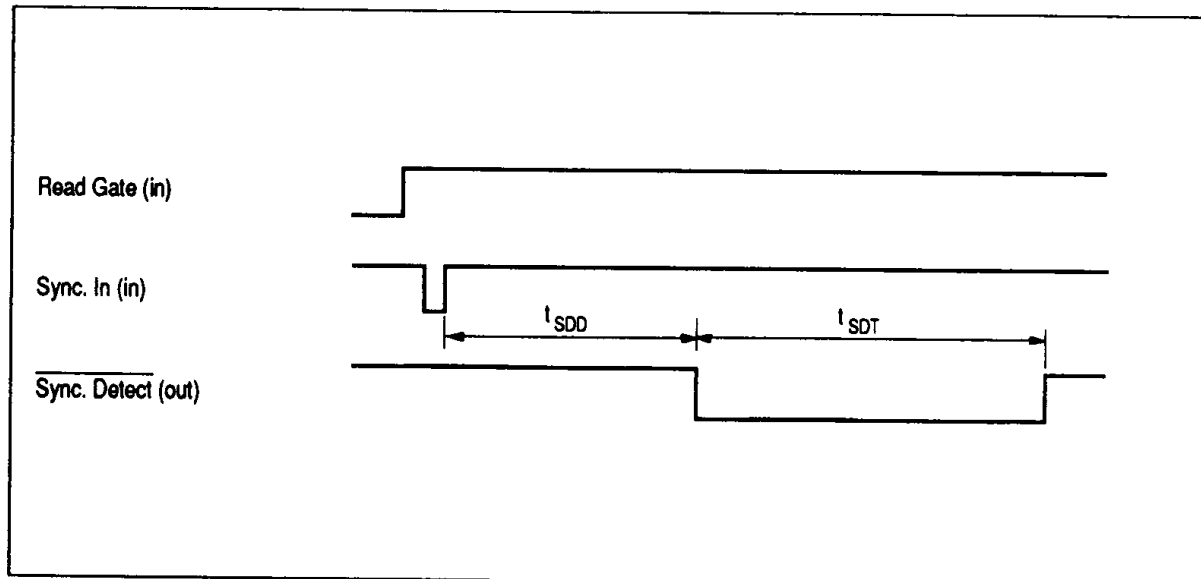


Figure 17 Sync Detect Output(Frequency Verification Mode)

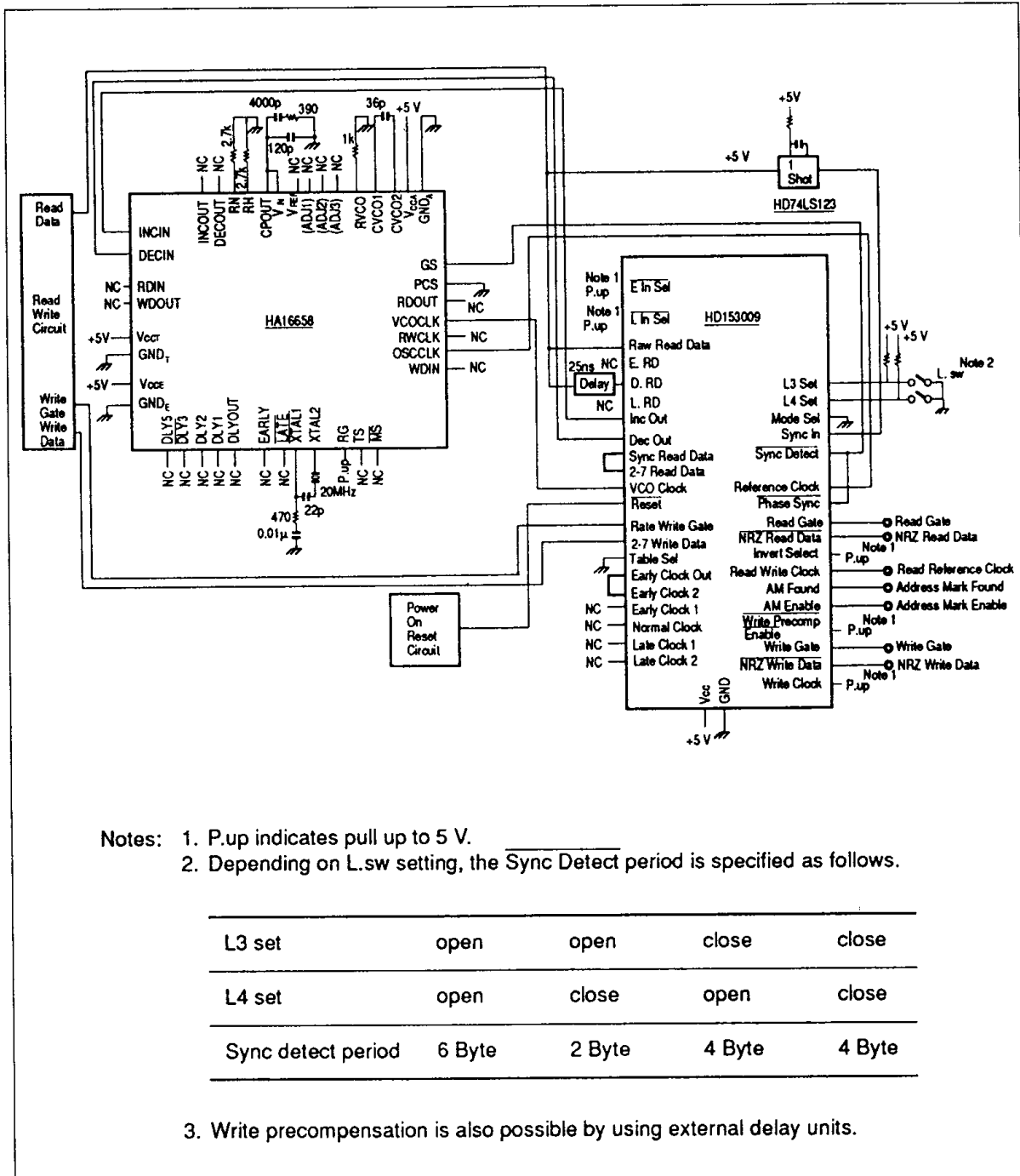


Figure 18 Circuit Example