Bluetooth Multimedia v2.1 + EDR

Datasheet: IS1621N ***Version: 0.96***

ISSC

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1. General Description

ISSC IS1621N is a compact, high integration, ultra-low cost, CMOS single-chip RF + baseband IC for Bluetooth v2.1+EDR (Enhanced Data Rate) 2.4GHz applications. This chip is fully compliant with Bluetooth specification and completely backward-compatible with BT1.1, 1.2 or 2.0 systems.

It incorporates Bluetooth 1M/2M/3Mbps RF, single-cycle 8051, TX/RX modem, memory controller, task/hopping controller, UART interface, and ISSC Bluetooth software stack to achieve the required BT v2.1+EDR functions.

To provide the best audio and voice quality, it also integrates a DSP co-processor, and a high performance stereo CODEC to handle voice and audio applications.

For voice, not only basic A-law/μ-law/CVSD encoding /decoding but also enhanced noise reduction and echo cancellation are implemented by the built-in audio processor to reach the best quality in the both sending and receiving sides. For enhanced audio applications, SBC or MP3 encoding/decoding functions are also carried out by audio processor to satisfy A2DP requirements.

In addition, to minimize the external components required for portable devices, a voltage sensor for battery, battery charger, a switching regulator and LDOs are integrated to reduce BOM cost for various Bluetooth applications.

The device incorporates built-in self-test (BIST) and auto-calibration functions to simplify production test.

2. Features

System Specification

- Compliant with Bluetooth Specification v.2.1 + EDR in 2.4 GHz ISM band

Baseband Hardware

- 16MHz main clock input
- Firmware execution from either internal ROM or external flash

- Built-in internal ROM or 4M flash for program memory
- Built-in 32 KB RAM for data storage and baseband data transfer buffering
- New features for Bluetooth 2.1
  - Encryption Pause and Resume
  - Erroneous Data Reporting
  - Extended Inquiry Response
  - Link Supervision Timeout Changed Event
  - Non-Flushable Packet Boundary Flag
  - Secure Simple Pairing
  - Sniff Subtracting
- Support both Pico-net and Scatter-net applications
- Hard-wired logic for modulation, demodulation, access code correlation, whitening, forward error correction (FEC), header error check (HEC), shorten hamming code, CRC generation/checking, frame check sequence (FCS), encryption bit stream generation, and transmit pulse shaping
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels
- Fast Connection supported

RF Hardware

- Fully Bluetooth 2.1 + EDR system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- +4dBm output power with level control 13 dB from register control.
- For Class2/3, transmitter support without the requirement for external power amplifier and TR switch.
- Build-in channel filter.
- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.

- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with build-in digital trimming for temperature/process variations.

Audio processor

- 16-bit/32-bit run time configurable audio processor
- Single cycle data computing up to 60 MIPS
- Support 64 kb/s A-Law or μ-Law PCM format, or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.
- SBC and optional MP3 supported

Stereo Audio Codec

- 16 bit stereo codec
- Dual mono microphone and stereo line in for ADC
- 94dB SNR stereo DAC playback
- Integrate headphone amplifier for 16Ω speakers
- Capacitor-less headphone driver stage for single-ended speakers

Peripherals

- Built-in Lithium-ion battery charger
- Integrate 3V, 1.8V LDO and Switching mode regulator
- Built-in 10-bit Aux-ADC for battery monitor and voltage sense.

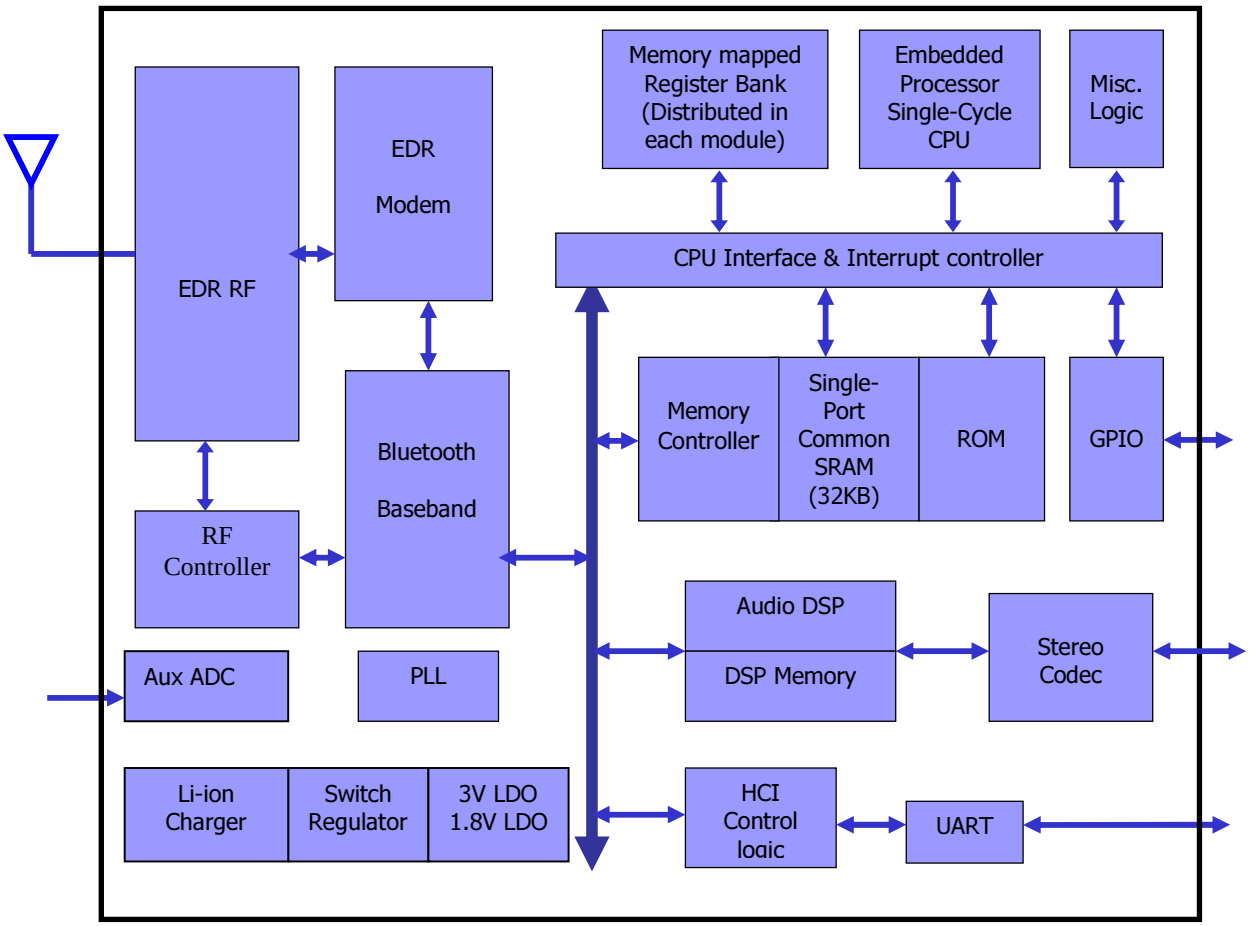
Flexible HCI interface

- High speed HCI-UART (Universal Asynchronous Receiver Transmitter) interface

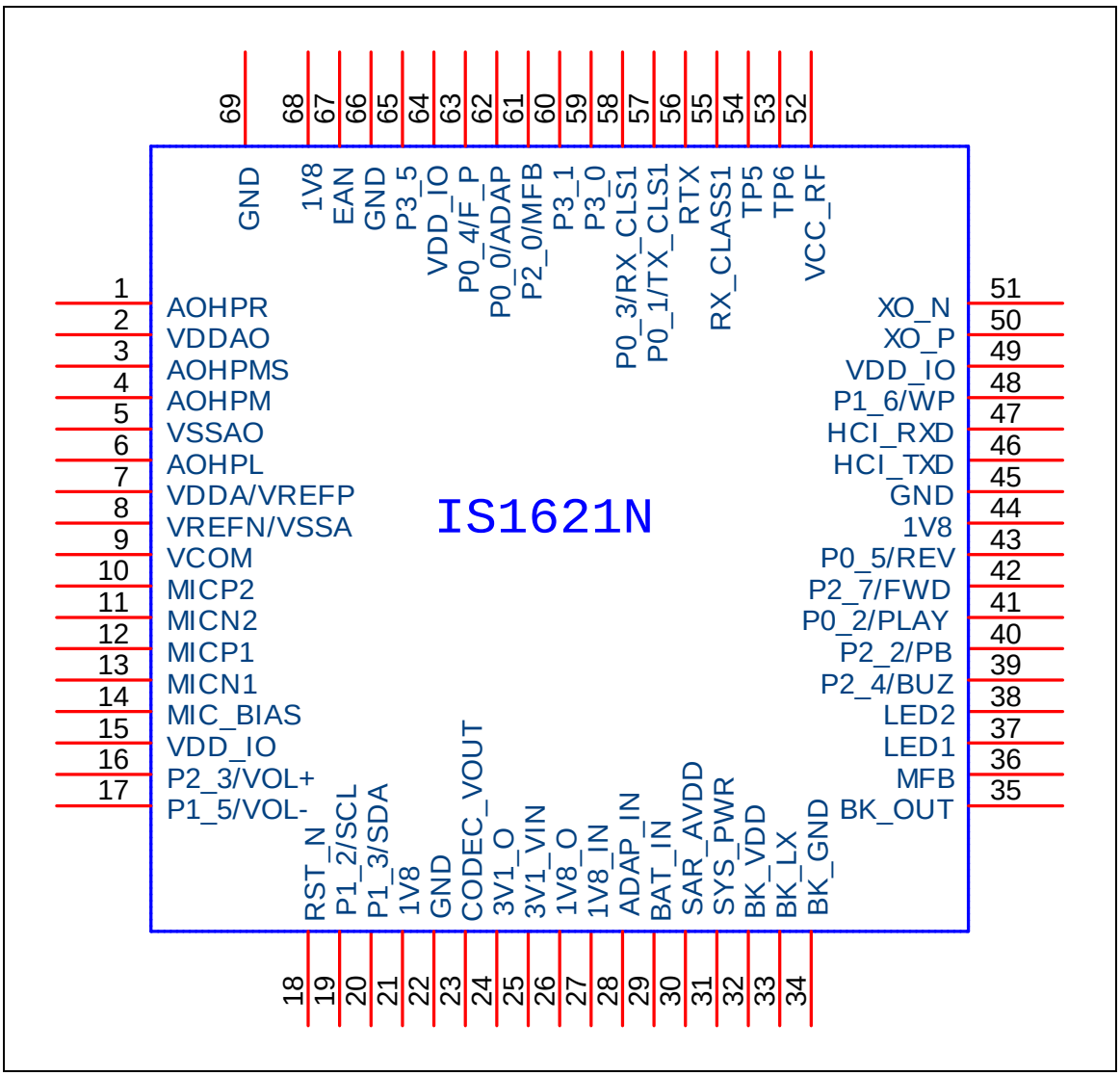
Package

- 68QFN standard package

3. Functional Diagram



4. Pin Assignment



5 Pin Descriptions

Pin No.	I/O	Pin Name	Pin Descriptions
1	AO	AOHPR	R-channed single ended analog headphone output
2	P	VDDAO	Positive power supply dedicated to CODEC output amplifiers.
3	AI	AOHPMS	Headphone common mode sense input
4	AO	AOHPM	Headphone common mode output
5	P	VSSAO	Negative power supply dedicated to CODEC output amplifiers
6	AO	AOHPL	L-channel single ended analog headphone output
7	P	VDDA/VREFP	Positive power supply/reference voltage for CODEC
8	P	VREFN/VSSA	Negative reference/power supply for CODEC Must be connected to the PCB analog ground(AGND)
9	AO	VCOM	Internal biasing voltage for CODEC
10	AI	MICP2	Mic 2 mono differential analog positive input
11	AI	MICN2	Mic 2 mono differential analog negative input
12	AI	MICP1	Mic 1 mono differential analog positive input
13	AI	MICN1	Mic 1 mono differential analog negative input
14	P	MIC_BIAS	Electric microphone biasing voltage
15	P	VDD_IO	I/O power supply input
16	I/O	P2_3/VOL+	GPIO, default pull-high input Be triggered by a LOW level signal Volume up key as the default setting
17	I/O	P1_5/VOL-	GPIO, default pull-high input Be triggered by a LOW level signal Volume down key as the default setting
18	AI	RST_N	System Reset Pin
19	I/O	P1_2/SCL	GPIO, default pull-high input EEPROM clock Clock signal for OLED driving IC BIST Testing
20	I/O	P1_3/SDA	GPIO, default pull-high input EEPROM data Data signal for OLED driving IC BIST Testing
21	P	1V8	Core 1.8V power input
22	P	GND	Digital ground.
23	P	CODEC_VOUT	3.1V LDO output for CODEC power
24	P	3V1_O	3.1V LDO output
25	P	3V1_VIN	3.1V LDO input
26	P	1V8_O	1V8 LDO Output
27	P	1V8_IN	1V8 LDO Input

Pin No.	I/O	Pin Name	Pin Descriptions
28	P	ADAP_IN	External power adaptor input
29	P	BAT_IN	Battery input
30	P	SAR_AVDD	SAR 1.8V input
31	P	SYS_PWR	System Power Output
32	P	BK_VDD	Buck VDD Power Input
33	P	BK_LX	Buck feedback input
34	P	BK_GND	Buck ground
35	P	BK_OUT	Buck output
36	P	MFB	Multi-Function Push Button key, push high
37	AI	LED1	LED Driver 1
38	AI	LED2	LED Driver 2
39	I/O	P2_4/BUZ	GPIO, default pull-high input HIGH or toggle to drive Buzzer/Charging Status/I2C CSB IC BIST testing/ASIC functional testing System Configuration, H: Boot Mode
40	I/O	P2_2	GPIO, default pull-low input. Reserve LED driver/ MFB function Be triggered by a HIGH level signal.
41	I/O	P0_2/Play	GPIO, default pull-high input Be triggered by a LOW level signal Play/Pause key as the default setting
42	I/O	P2_7/FWD	GPIO, default pull-high input Be triggered by a LOW level signal FWD key as the default setting
43	I/O	P0_5/REV	GPIO, default pull-high input Be triggered by a LOW level signal REV key as the default setting ASIC functional testing
44	P	1V8	Core 1.8V power input
45	P	GND	Digital ground
46	O	HCI_TXD	HCI TX data
47	I	HCI_RXD	HCI RX data
48	I/O	P1_6	GPIO P1_6, default pull-high input EEPROM WP. RTS for OLED.
49	P	VDD_IO	I/O power supply input
50	I	XO_P	16MHz Crystal input positive
51	I	XO_N	16MHz Crystal input negative
52	RP	VCC_RF	RF power input for both VCO and IO power
53	I/O	TP6	RF test point

Pin No.	I/O	Pin Name	Pin Descriptions
54	I/O	TP5	RF test point
55	I	RX_CLASS1	Class1/Class2 RX path without TR combiner Combine with P0_1/P0_3 to control the external TR Switch & LNA.
56	I/O	RTX	Class 2 RTX path (TR combiner active); Class1/Class2 TX path
57	I/O	P0_1/TX_CLS1	GPIO, default pull-high input Class1/Class2 Control signal of external TR switch HIGH is TX duration
58	I/O	P0_3/RX_CLS1	GPIO, default pull-high input Class1/Class2 Control signal of external TR switch HIGH is RX duration
59	I/O	P3_0	GPIO, default pull-high input UART_CTS is implemented for OLED control ASIC functional testing
60	I/O	P3_1	GPIO, default pull-high input Be triggered by a HIGH level signal External MCU wake-up signal ASIC functional testing
61	I/O	P2_0	GPIO, default pull-high input I2C SCLK ASIC functional testing System Configuration, H: Application L: Baseband
62	I/O	P0_0/ADAP	GPIO, default pull-low input. Adapter Plug-In Indicator/Reserve LED driver/I2C MCLK IC BIST testing
63	I/O	P0_4/F_P	GPIO, default pull-high input Be triggered by a LOW level signal Fast paring key/External Regulator Enable/I2C SDATA
64	P	VDD_IO	I/O power supply input
65	I/O	P3_5	GPIO 3_5, default pull-high input.
66	P	GND	Digital ground.
67	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash
68	P	1V8	Core 1.8V power input
69	P	GND	Exposed pad as ground

NOTE: Default GPIO Setting

A. P0_1/P0_3 is configured in EEPROM for Class1/Class2 applications.

B. Class1/Class2 Control Signal of external TR switch:

P0_1 High: TX, P0_3 High: RX

C. Music Control:

Play/Pause: P0_2, FWD: P2_7, REV: P0_5,Volume up:P2_3,Volume down:P1_5

D. EEPROM/OLED Control:

P1_6:EEPROM WP/UART_RTS for OLED Control

P1_2:EEPROM Clock/Clock Signal for OLED driving

P1_3:EEPROM Data/Data Signal for OLED driving

P3_0:UART_CTS for OLED control

P3_1:External MCU wake-up signal

E. I2C:

SCLK:P2_0, SDATA: P0_4, CSB:P2_4,MCLK:P0_0

F. External Power Manager Control Signal:

P0_0: Adapter Plug-In Indicator

P2_2: MFB function

P0_4: External Regulator Enable

P2_4: Charging Status

G. Other Function:

Fast Paring Key:P0_4

Buzzer: P2_4

System Configuration: P2_0, P2_4

6 Functional Description

6.1 Overall Architecture

The ISSC IS1621N integrates an enhanced EDR Bluetooth RF & BB core, HCI controller, Audio DSP and an ENHANCED 8051 processor with an internal mask ROM for program memory and SRAM for data memory. An innovative interconnection structure called the Common-Memory Architecture (CMA) is designed to provide a fast and flexible data movement scheme between the embedded processor, Bluetooth core, and peripheral hardware.

For audio and power management, IS1621N provide embedded audio processor, stereo codec and some power management to reduce the external components.

6.2 Radio Frequency (RF)

6.2.1 Transmitter

The internal PA has a maximum output power of +4dBm with level control 8dB from amplitude control. This is applied into Class2/3 radios without external RF PA. For Class1 application, the build-in level control can be used with external PA for power control requirement.

The transmitter features IQ direct conversion to minimize the frequency drift. And it can excess 30dB power range with temperature compensation machine.

6.2.2 Receiver

The LNA can be operated into two type modes. One type is TR-combined mode for single port application. The other type is TR-separated mode for external PA/LNA application.

An ADC is used to sample input analogue wave for digital demodulation. Before the ADC, a channel filter has been integrated into receiver channel to increase the anti-interference capacity and also reduce the external component count.

For avoiding temperature variation issues, a temperature sensor with temperature calibration is utilized into bias current and gain control of LNA, Mixers, and RF AMP.

6.2.3 Synthesizer

The internal loop filter is used to reduce external RC components. This can reduce cost and variations for components. This internal LC tank for VCO is utilized to reduce variation for components. The cost is down at the same time.

A fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.

6.3 MODEM

There are three different modulations for Bluetooth v2.1 + EDR. Table 6.3 summarizes these modulations and data rate.

Figure 6.3 Modulation type for Bluetooth v2.1 + EDR

Data Rate	Modulation	Bits/Symbol
BDR: 1 Mbps	GFSK	1
EDR: 2 Mbps	π/4 DQPSK	2
EDR: 3 Mbps	8DPSK	3

6.3.1 Basic Data Rate MODEM (BDR)

On the Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v2.1+EDR specification.

Figure 6.3.1 Data format for BDR

Access Code	Header	Payload

6.3.2 Enhanced Data Rate MODEM (EDR)

On the Bluetooth v2.1+EDR specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v2.1+EDR specification. For the viewpoint of

baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8DPSK.

Figure 6.3.2.A Data format for EDR

Access Code	Header	Guard	Sync	Payload	Trailer

For π/4 DQPSK modulation, each symbol carries 2 bits of information. For its constellation diagram, although there are 8 possible phase states, the encoding scheme guarantees the trajectory of the modulation between symbols is restricted to 4 states. For a given starting point, every phase change between symbols is restricted to +45°, +135°, -45°, and -135°.

Figure 6.3.2.B Phase shift & bit pattern for 2 MHz data rate

Phase Shift	Bit Pattern
+45° (+π/4)	00
+135° (+3π/4)	01
-135°(-3π/4)	11
-45°(-π/4)	10

For 8DPSK modulation, each symbol carries 3 bits of information. For its constellation diagram, it is similar toπ/4 DQPSK but the trajectory of the modulation between symbols has 8 possible phase states. For a given starting point, every phase change between symbols is restricted to 0°, +45°, +90°, +135°, +180°, -135°, -90°, and -45°.

Figure 6.3.2.C Phase shift & bit pattern for 3 MHz data rate

Phase Shift	Bit Pattern
0° (+0)	000

+45° (+π/4)	001
+90° (+π/2)	011
+135° (+3π/4)	010
+180° (+π)	110
-135° (-3π/4)	111
-90° (-π/2)	101
-45° (-π/4)	100

6.4 Baseband

The following modules implemented in hardware constitute the Bluetooth Baseband Core. The frequency hopping sequence generator produces the correct hop frequency control sequence based on the Bluetooth clock, Bluetooth device address, and the current operating mode.

The access code generates the access code based on the Lower Address Part (LAP) of the Bluetooth device address. The access code is comprised of the preamble, sync word and trailer bits. The detection of the access code uses correlation to detect a valid access code.

Bluetooth uses two types of FEC: 1/3 repetition code and (15, 10) shorten Hamming code respectively. The former basically repeats each transmitted bit three times while the latter has 15 bits of codeword which contains 5 parity bits. The code has capability of correction of all single-bit errors in each codeword.

The purpose of HEC is to protect the header bits. Dedicated header error code generator calculates the HEC bits in the header of a transmitted packet. While on the receiver side, HEC detects corrupted headers.

A 16-bit CRC is adopted to protect payload data transmitted using certain types of Bluetooth packets.

Information confidentiality can be protected by encryption of the packet payload. Dedicated encryption/decryption hardware is designed into the baseband core.

6.5 MCU

The embedded processor for IS1621N is a single-cycle 8051 CPU. The embedded processor will be referred to as simply the processor, 8051, or MCU throughout the remainder of this document. There are a few minor differences between a standard 8051 and this CPU. These include:

1. Alteration of memory timings to match internal and external memory configurations.
2. Modification of idle mode to disable internal CPU clocking. Only externally-clocked interrupt sources can allow the CPU to recover from idle mode.

A single-port synchronous interface is provided to memory. From this single port, the bandwidth is divided among the 7 interfaces spread amongst 5 physical busses described below:

- Embedded processor bus
- Baseband TX bus
- Baseband RX bus
- HCI TX bus
- HCI RX bus
- Audio bus
- DMA bus

In addition, attached to the embedded processor bus are a register bank, a dedicated single-port memory (data segment 1), and flash memory (program segment). The processor coordinates all link control procedures and data movement using a set of pointer registers. For example, when an HCI packet (from the host via USB or UART) is received into the HCI buffer, the processor is interrupted. The processor can then read a status register to determine the HCI packet type and determine whether to set up the Baseband pointer registers for this memory region for RF-retransmission, or to otherwise directly perform packet processing with the CPU.

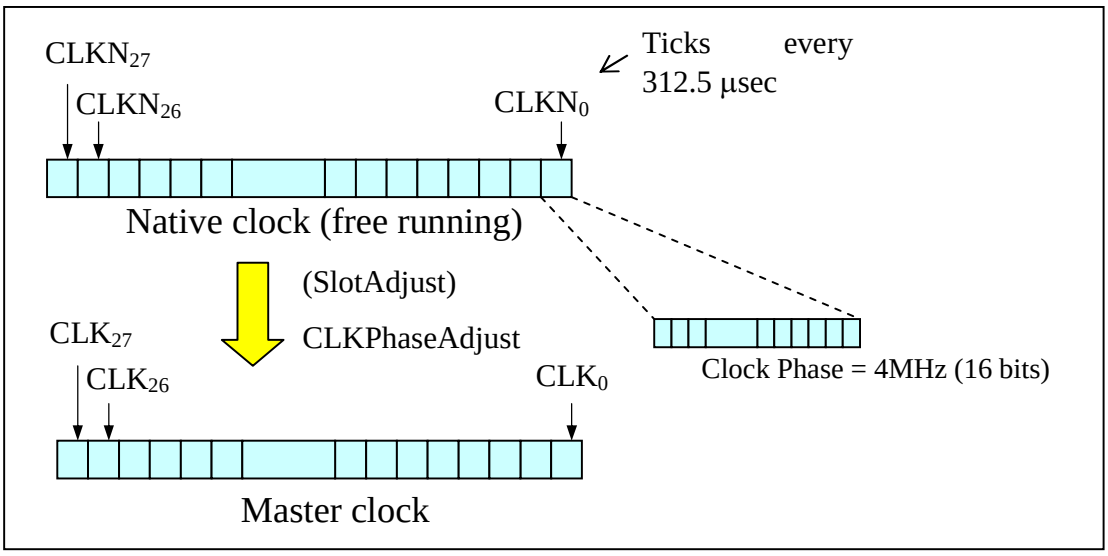
6.6 Bluetooth Clock and Timers

A Bluetooth standard 28-bit counter running at 3.2 kHz implements the native clock defined by Bluetooth specification. This clock provides the transmission and receiving timing of a half time slot (312.5 μs). Another finer counter implemented in 16 bits is also provided as the phase of a half time slot. This phase information is very helpful when a Bluetooth slave wants to adapt to its master's clock. The counter is pre-scalable for the purpose of power saving operations. The diagram below describes a standard Bluetooth native clock and master clock. The clock signal is also used as a slot boundary signal to trigger a baseband packet transmission or receipt.

There are several timers provided by the system, two timers for TX/RX and the others for general purpose.

The powerful pre-scheduling functions for the transceiver are realized different sets of programmable timers. Each set of timers is associated with the task of transmission or receiving. When the timer is configured by firmware, it will automatically execute the TX or RX task at a specific time. Sub-tasks and timing for a TX task remain to be defined.

Figure 6.6 Bluetooth clock



6.7 HCI Control Logic for USB/UART

Hardwired control logic is presented in front of the UART devices for HCI protocol handling and packet buffering. This control logic is part of the HCI controller defined in Bluetooth specification 1.2. This logic is partially responsible for the HCI protocol handling to/from the host and it also maps the registers of the UART devices indirectly to the 8051 such that the system can receive or send a HCI packet to/from the respective host interface. Major functions of this logic include:

- HCI packet formatter and de-formatter (identifying the packet type)
- Frame boundary determination, segmentation and reassembly of HCI packets.
- HCI packet transmission, receiving, and buffering (using common memory HCI buffer).
- Independent receive / transmit channels
- Universal device interface

6.7.1 HCI UART Interface

An embedded HCI UART (Universal Asynchronous Receiver Transmitter) with programmable data rate up to 3Mbps is included in this design. The HCI UART supports the following functions:

- Full-Duplex operation
- Programmable BAUD rate (using 16-bit input clock divider to obtain Baud Rate x16 or x24 or x13 clock base)
- 7 or 8 Data bits
- 1 or 2 Stop bits
- Even / Odd / Mark / Space / None Parity configurations
- Break Generation / Detection
- Maskable individual interrupts to CPU and combined Error interrupt to HCI
- Selectable Direct CPU interface or interface to HCI module

6.8 General Purpose I/O

The IS1621N provides several general purpose I/O ports. These general I/Os can be defined as input or output port individually by setting specific register bit. While setting as an input port, a build-in 50KΩ pull high or pull low resistor can be enabled for different application purpose.

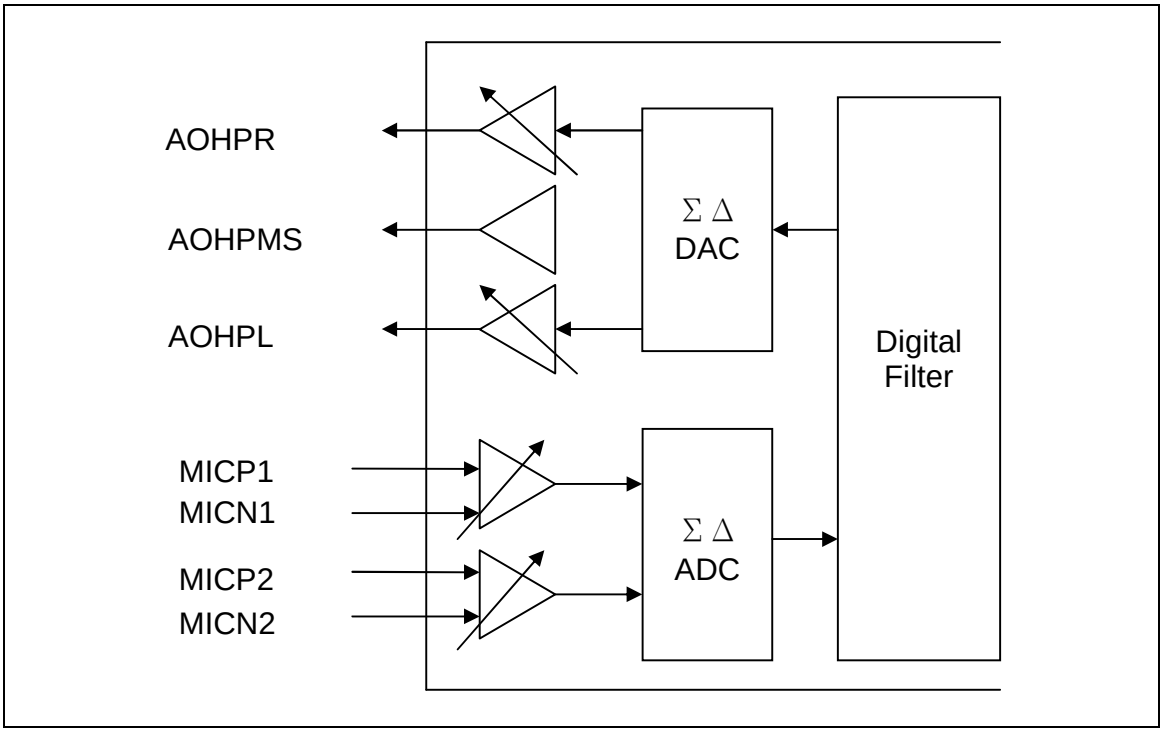
6.9 Audio Processor

The audio processor is a 16/32 bit run time configurable fixed point DSP core with hardware accelerator. The maximum 60MIPS single cycle 16-bit/32-bit data computing provides the combination of performance and power, memory saving. The standard A-law/μ-law/CVSD voice function and SBC A2DP audio are implemented in the firmware. The enhanced audio functions, like AEC, noise reduction, and optional codec like MP3, WMA can also be achieved with enhanced algorithm.

6.10 Audio Codec

The build in codec contains a stereo analog to digital convert (ADC), a stereo digital to analog converter (DAC) and additional analog circuits like headphone driver and microphone amplifier.

Figure 6.10 Audio Codec



6.10.1 ADC

The ADC interface can be configured to a stereo line input or two mono microphone inputs. While used as line input, the ADC supports 44.1k Hz or 48k Hz sampling rate. If used for mono microphone, the ADC supports variety sampling rate from 8k Hz to 48k Hz. The microphone input has 42 dB programmable analog gain and 48db digital gain. A regulated MIC_Bias is available

6.10.2 DAC

The DAC output is available for both line level and through the headphone amplifier to drive a low impedance headphone. The headphone output volume is adjustable by the combination of the digital/analog gain control. For the common single-end audio output requirement, a three-wire capacitor-less headphone output stage can be chosen.

6.11 Auxiliary ADC

The 10-bit auxiliary analog to digital converter (SAR ADC) provides one dedicated channel for battery power detection and one other channel for external peripheral sensing. This ADC has 10 bits resolution that provides a high accurate monitoring for battery voltage. The operating current is very low and almost consumes no power when disabled.

6.12 Power Management

IS1621N has three power control functions, Lithium-ion/Polymer battery charger, switch-mode regulator and linear regulators.

The charger includes four operation modes, reviving mode, trickle mode, constant current mode and constant voltage mode. Charging termination is based on the minimum current and will start re-charge if the battery falls below the threshold voltage.

The switch mode regulator provides the RF and baseband core supplies.

Two linear regulators are used to generate the power for chip I/O and codec.

6.13 Miscellaneous (Watchdog Timer, and Clock Divider)

System related functions such as watchdog timer, Endian control, and interrupt vectors are also provided. The purpose of the watchdog timer is to provide a reset to CPU in case when the CPU fails to service the watchdog timer in a pre-defined (programmable) period.

7 Electrical Characteristics

Recommended operate condition

Symbol	Parameter	Min	Typical	Max	Unit
V_{DD18}	Digital core supply voltage SAR ADC supply voltage CODEC supply voltage	1.62	1.8	1.92	V
V_{DDIO}	I/O supply voltage RF supply voltage	2.43	2.7	3.63	V
$T_{OPERATION}$	Operating temperature range	-40	+25	+85	ºC
T_{stg}	Storage temperature	-40		+125	ºC
V_{LDO}	LDO supply voltage	2.1		3.6	V
V_{BAT_IN}	Input voltage for SAR ADC	0.9		3.6	V

Digital I/O pins (I/O pins at V_{DDIO})

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = 4mA	2.4		-	V
V_{OL}	Low-level output voltage	I_{OL} = 4mA	-	-	0.4	V

Transmitter section for BDR

VCC_RF = 2.7V Temperature = 25ºC	Typ	Unit
Maximum RF transmit power	4	dBm
RF power variation over temperature range with compensation enable	1.5	dB
RF power variation over temperature range with compensation disable	2.7	dB
RF power control range	13	dB
RF power range control range resolution	0.5	dB
20db bandwidth for modulated carrier	780	kHz
Adjacent channel transmit power F = F0 ± 2Mhz	-41	dBm
Adjacent channel transmit power F = F0 ± 3Mhz	-45	dBm
Adjacent channel transmit power F = F0 ≥ 3Mhz	-50	dBm
Δf1avg Maximum Modulation	165	kHz
Δf2avg Minimum Modulation	152	kHz
Δf1avg / Δf2avg	0.98	
Initial carrier frequency tolerance	5	kHz
Drift Rate	7	kHz/50us
Drift (single slot packet)	8	kHz
Drift (five slot packet)	10	kHz
2^{nd} Harmonic Content	-50	dBm
3^{rd} Harmonic Content	-45	dBm

Receiver section for BDR

Temperature = 25ºC		**Typ**	**Unit**
	Frequency (GHz)		
Sensitivity at 0.1% BER for all packet types	2.402	-87	dBm
	2.441	-88	dBm
	2.480	-87.5	dBm
Maximum received signal at 0.1% BER		≥-10	dBm
	Frequency (GHz)	**Typ**	**Unit**
Continuous power required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at the unbalanced port of the balun	30-2000	≥0	dBm
	2000-2400	-15	dBm
	2500-3000	-15	dBm
C/I co-channel		7	dB
Adjacent channel selectivity C/I F = F0 + 1 MHz		4	dB
Adjacent channel selectivity C/I F = F0 - 1 MHz		-3	dB
Adjacent channel selectivity C/I F = F0 + 2 MHz		-45	dB
Adjacent channel selectivity C/I F = F0 - 2 MHz		-23	dB
Adjacent channel selectivity C/I F = F0 + 3 MHz		-48	dB
Adjacent channel selectivity C/I F = F0 - 5 MHz		-48	dB
Adjacent channel selectivity C/I F = Fimage		-22	dB
Maximum level of inter-modulation interference		-30	dBm
Spurious output level		≤-130	dBm/Hz

Transmitter Section for EDR

Temperature = 25ºC		**Typ**	**Unit**
Maximum RF transmit power		1	dBm
Relative transmit power		-1.3	dB
π/4 DQPSK max carrier frequency stability w0		1.9	kHz
π/4 DQPSK max carrier frequency stability wi		2.1	kHz
π/4 DQPSK max carrier frequency stability | w0 + wi |		3.4	kHz
8DPSK max carrier frequency stability w0		1.5	kHz
8DPSK max carrier frequency stability wi		2.9	kHz
8DPSK max carrier frequency stability | w0 + wi |		4.0	kHz
π/4 DQPSK Modulation Accuracy	RMS DEVM	7	%
	99% DEVM	12	%
	Peak DEVM	18	%
8 DPSK Modulation Accuracy	RMS DEVM	7	%
	99% DEVM	12	%
	Peak DEVM	19	%
In-band spurious emissions	F > F0 + 3MHz	-45	dBm
	F < F0 - 3MHz	-45	dBm
	F = F0 - 3MHz	-41	dBm
	F = F0 - 2MHz	-28	dBm
	F = F0 – 1MHz	-30	dB
	F = F0 + 1MHz	-30	dB
	F = F0 + 2MHz	-26	dBm
	F = F0 + 3MHz	-28	dBm
EDR Differential Phase Encoding		No Error	%

Receiver Section for EDR

Temperature = 25°C		**Typ**	**Unit**
	Modulation		
Sensitivity at 0.01% BER	π/4 DQPSK	-88	dBm
	8DPSK	-82	dBm
Maximum received signal at 0.01% BER	π/4 DQPSK	≥-10	dBm
	8DPSK	≥-10	dBm
C/I co-channel	π/4 DQPSK	8	dB
	8DPSK	18	dB
Adjacent channel selectivity C/I F = F0 + 1 MHz	π/4 DQPSK	-10	dB
	8DPSK	-5	dB
Adjacent channel selectivity C/I F = F0 - 1 MHz	π/4 DQPSK	-10	dB
	8DPSK	-6	dB
Adjacent channel selectivity C/I F = F0 + 2 MHz	π/4 DQPSK	-40	dB
	8DPSK	-41	dB
Adjacent channel selectivity C/I F = F0 - 2 MHz	π/4 DQPSK	-23	dB
	8DPSK	-22	dB
Adjacent channel selectivity C/I F = F0 + 3 MHz	π/4 DQPSK	-45	dB
	8DPSK	-45	dB
Adjacent channel selectivity C/I F = F0 - 5 MHz	π/4 DQPSK	-45	dB
	8DPSK	-45	dB
Adjacent channel selectivity C/I F = FImage	π/4 DQPSK	-20	dB
	8DPSK	-12	dB

Audio Codec: ADC

Test Condition:

T= 25°C, Vdd=3.3V, 1KHz sine wave input, Bandwidth = 20~20KHz

Parameter	Condition	Min.	Typ.	Max.	Unit
Input Level	Line/microphone input, Full scale			2.8	Vpp
Resolution			16		bits
Input Sampling Rate		8		48	kHz
SNR	A-weighted 1KHz@full scale, Line input, microphone input		86		dB
	A-weighted 1KHz@full scale, Microphone boost enable		75		
THD			-70		dB
Digital Gain				48	dB
Analog Gain				42.5	dB
Gain Step			1.5		dB
Input resistance	$R_{L,}$ Microphone input		12		kOhm
	$R_{L,}$ Line input		80		
Output capacitance	Cp			25	pF

Audio Codec: DAC

Test Condition:

T= 25°C, Vdd=3.3V, 1KHz sine wave input, Bandwidth= 20~20KHz

Parameter	Condition	Min.	Typ.	Max.	Unit
Output Level	Full scale		2.35		Vpp
Resolution			16		bits
Output Sampling Rate		8		48	KHz
SNR	A-weighted 1KHz@full scale		94		dB
Max Output Power	R_L=16Ohm		40		mW
	R_L=32Ohm		20		mW
THD	16Ohm load		-65		dB
Digital Gain		-42		0	dB
Analog Gain		-22.5		0	dB
Gain Step			1.5		dB
Output resistance	R_L	16			Ohm
Output capacitance	Cp			100	pF

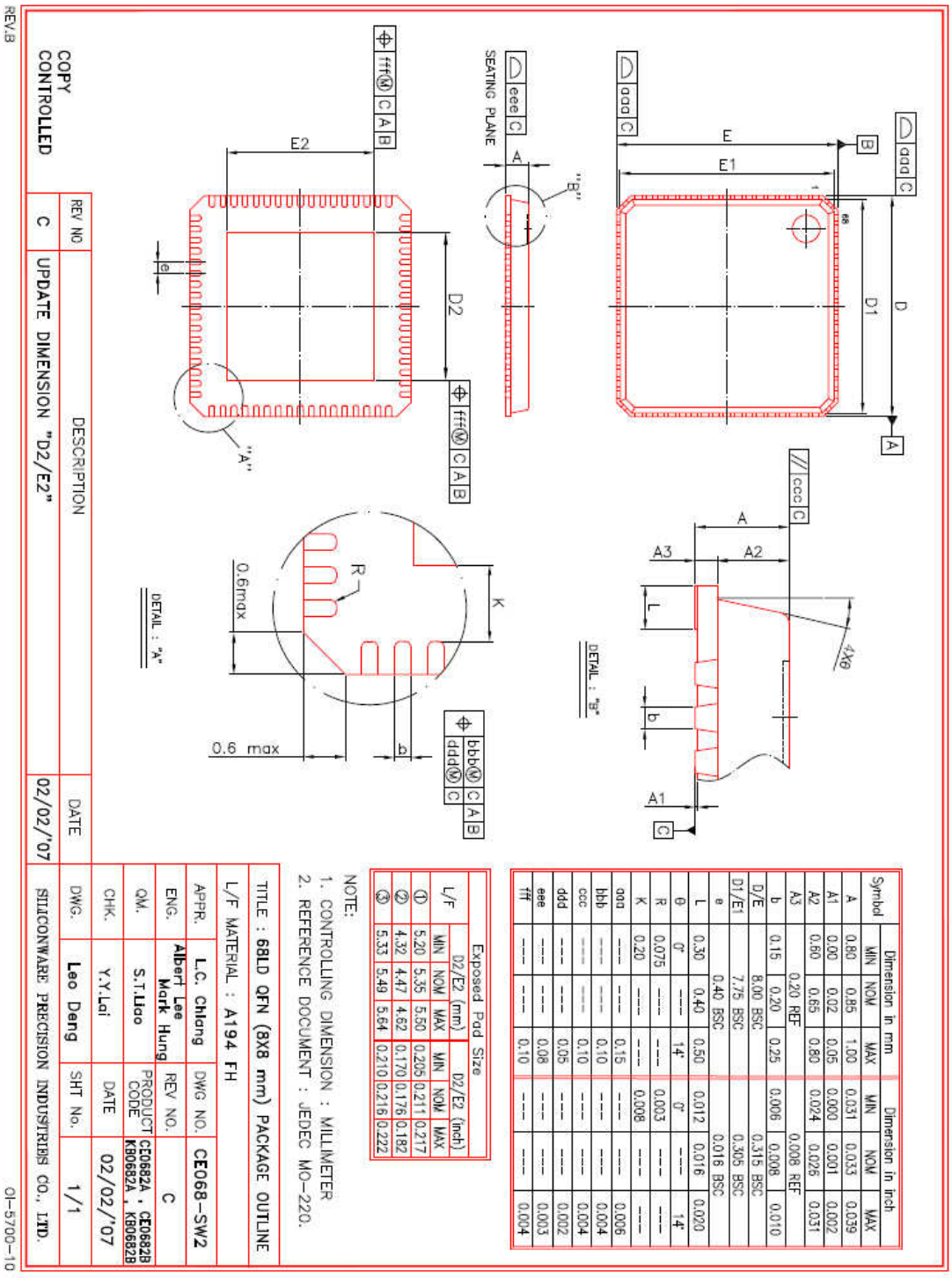
Battery Charger

Parameters	Test Condition	MIN	TYP	MAX	Unit
Supply voltage (V_{adap})		4.5		5.5	V
Charging operating current (I_{DD})	$V_{DD} > V_{DD}$ (min)		6		mA
V_{DD} sleep current (I_{DS})	$V_{BAT} \geq V_{DD}$ (min), $V_{BAT} - V_{DD} \geq 0.8V$		1		μA
Fast charge current (I_{CC})		20		150	mA
Float voltage (with correct trim value)		4.16	4.2	4.24	V
Float voltage trim step size			20		mV
Trickle charge voltage			2.9		V
Trickle charge current, % of charge current			10		%
Re-charge Voltage			4.1		V

Clock

Parameters	Test Condition	MIN	TYP	MAX	Unit
Crystal Frequency			16		MHz
Frequency Tolerence			±20		ppm
Operating Temperature		-20		70	^{O}C
Trimming Capacitance			6.4		pF
Trimming Step Size			0.2		pF

8 Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		8.00 BSC			0.315 BSC	
D1/E1		7.75 BSC			0.305 BSC	
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	----	14°	0°	----	14°
R	0.075	----	----	0.003	----	----
K	0.20	----	----	0.008	----	----
aaa	----	----	0.15	----	----	0.006
bbb	----	----	0.10	----	----	0.004
ccc	----	----	0.10	----	----	0.004
ddd	----	----	0.05	----	----	0.002
eee	----	----	0.08	----	----	0.003
fff	----	----	0.10	----	----	0.004

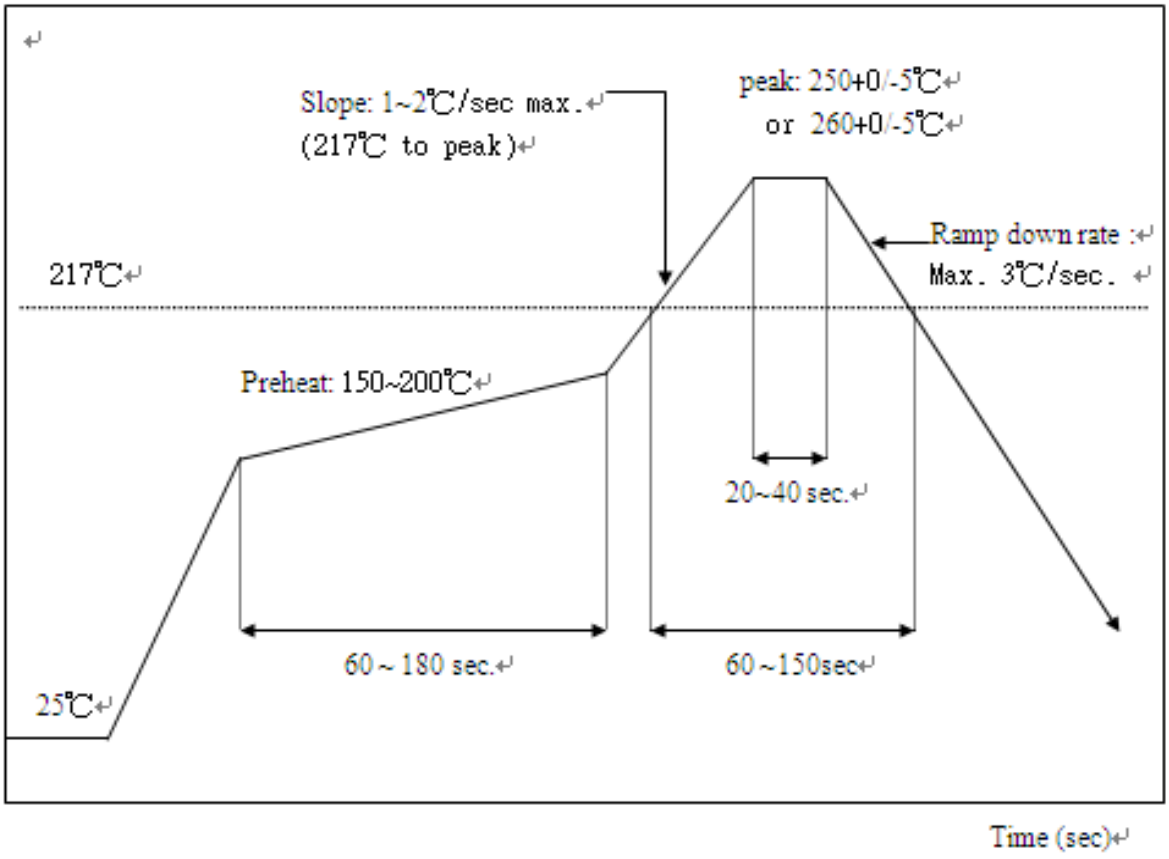
Exposed Pad Size						
L/F	D2/E2 (mm)			D2/E2 (inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
①	5.20	5.35	5.50	0.205	0.211	0.217
②	4.32	4.47	4.62	0.170	0.176	0.182
③	5.33	5.49	5.64	0.210	0.216	0.222

Appendix A. Reflow Profile

1.) Follow: IPC/JEDEC J-STD-020 C

2.) Condition:

Average ramp-up rate (217℃ to peak): 1~2℃/sec max.
Preheat：150~200C、60~180 seconds
Temperature maintained above 217℃：60~150 seconds
Time within 5℃ of actual peak temperature: 20 ~ 40 sec.
Peak temperature：250+0/-5℃ or 260+0/-5℃
Ramp-down rate : 3℃/sec. max.
Time 25℃ to peak temperature : 8 minutes max.
Cycle interval：5 minus



Appendix B. BQB certification

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