Ordering number : ENA1229B

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

CMOS IC

LE25FW403A — 4M-bit (512K×8) Serial Flash Memory 30MHz SPI Bus

Overview

The LE25FW403A is an onboard programmable flash memory device with a 512K×8-bit configuration. It uses a single 3.0V power supply and supports the serial interface. It has three erase functions depending on the size of memory area in which the data is to be erased: the chip erase function, the sector (64K bytes) erase function, and a page (256 bytes) erase function. A page program method is supported for data writing and it can program any amount of data from 1 to 256 bytes. The page program time depends on the number of bytes programmed and the IC provides a high-speed program time of 1.5ms (typ) when programming 256 bytes at one time. Moreover, equipped with a page write function that allows anywhere from 1 to 256 bytes of data in a page to be rewritten, this device is optimal for applications that perform small-scale rewriting.

Features

- Read/write operations enabled by single 3.0V power supply: 2.7 to 3.6V supply voltage range
- Operating frequency : 30MHz
- Temperature range : 0 to 70°C
- Serial interface : SPI mode 0, mode 3 supported
- Sector size : 256 bytes/page sector, 64K bytes/sector
- Page erase, sector erase, chip erase functions
- Page program function (1 to 256 bytes/page), Page write function (1 to 256 bytes/page)
- Hardware protect function (lower 256 pages)
- Hardware reset function

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- Highly reliable read/write
  Number of rewrite times: 10^5 times
  Page erase time : 10ms (typ.), 20ms (max.), Number of rewrite times: 10^4 times or less
  : 25ms (typ.), 300ms (max.), Number of rewrite times: 10^5 times or less
  Sector erase time : 30ms (typ.), 500ms (max.)
  Chip erase time : 300ms (typ.), 5s (max.)
  Page program time : 1.5ms/256 bytes (typ.), 2.5ms/256 bytes (max.)
  Page write time : 11ms (typ.), 22.5ms (max.), Number of rewrite times: 10^4 times or less
  : 25ms (typ.), 300ms (max.), Number of rewrite times: 10^5 times or less
- Status functions
  Ready/busy information
- Data retention period : 20 years
- Package : LE25FW403ATT MSOP8 (225mil)

Package Dimensions

unit:mm (typ)
3276

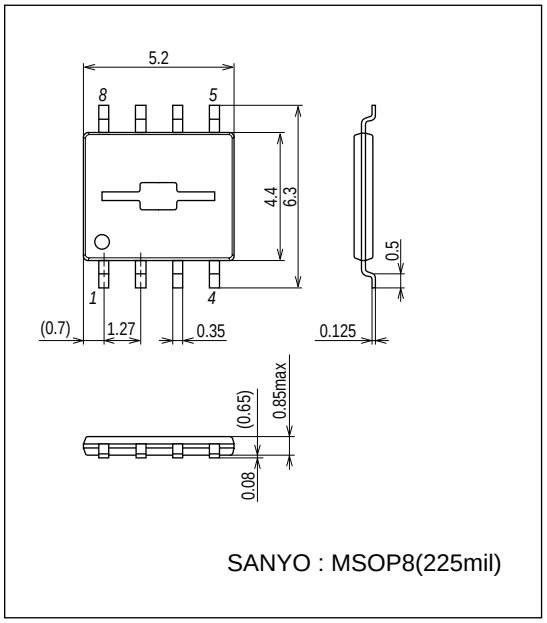


Figure 1 Pin Assignment

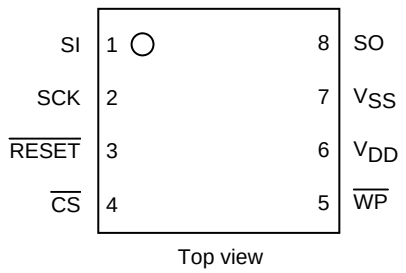


Figure 2 Block Diagram

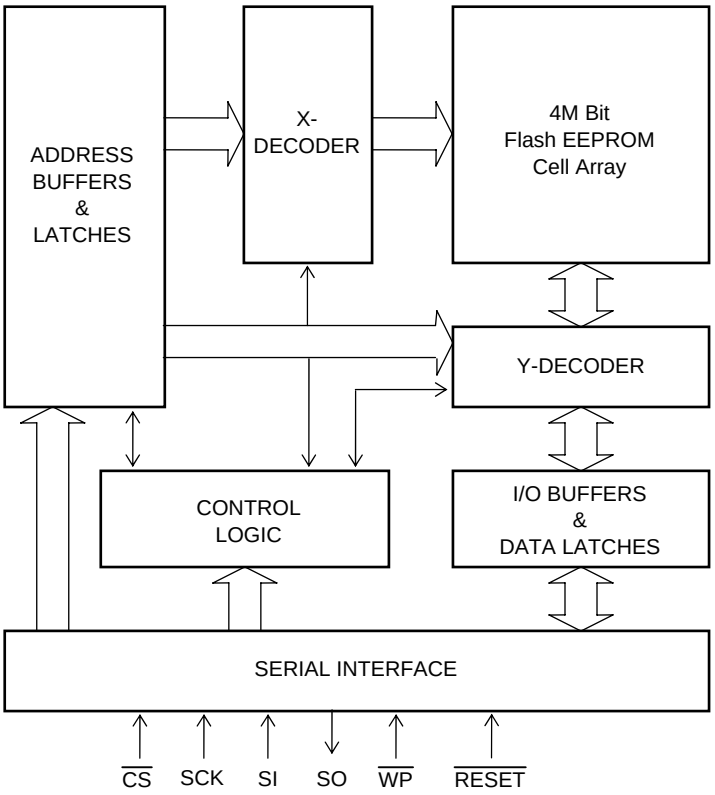


Table 1 Pin Description

Symbol	Pin Name	Description
SCK	Serial clock	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI	Serial data input	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock.
SO	Serial data output	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock.
$\overline{CS}$	Chip select	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
$\overline{WP}$	Write protect	Lower 256 pages are protected when the logic level of this pin is low.
$\overline{RESET}$	RESET	The device resets when the logic level of this pin is low. However, reset is disabled when write (erase, program, or page write) are being internally executed by the device.
V_{DD}	Power supply	This pin supplies the 2.7 to 3.6V supply voltage.
V_{SS}	Ground	

Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0			
	0Bh	A23-A16	A15-A8	A7-A0	X		
Page erase	DBh	A23-A16	A15-A8	X			
Sector erase	D8h	A23-A16	X	X			
Chip erase	C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *1	PD *1	PD *1
Page write	0Ah	A23-A16	A15-A8	A7-A0	PD *1	PD *1	PD *1
Write enable	06h						
Write disable	04h						
Power down	B9h						
Status register read	05h						
Read silicon ID	9Fh *2						
Exit power down mode	ABh						

Explanatory notes for Table 2

X = don't care, h = Hexadecimal notation, A23-A19 = don't care for all commands

Even if $\overline{CS}$ is raised for longer than the bus cycle given in the command settings table, the command will be recognized. However, $\overline{CS}$ must be raised between one bus cycle and the next.

*1. PD: Program data. Input any number of bytes of data from 1 to 256 bytes in 1-byte units.

*2. After the first bus cycle, Silicon ID repeatedly outputs 62h (manufacturer code), 11h (device code), and 00h (dummy code).

Device Operation

The LE25FW403A features electrical on-chip erase functions using a single 3.0V power supply, that have been added to the EPROM functions of the industry standard that support serial interfaces. Interfacing and control are facilitated by incorporating the command registers inside the chip. The read, erase, program and other required functions of the device are executed through the command registers.

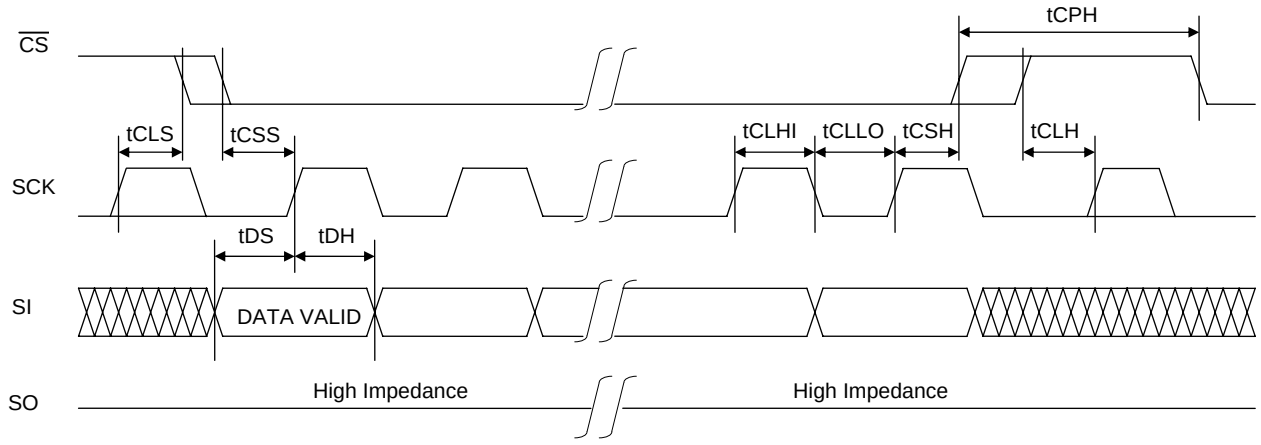
The command addresses and data are latched for program, erase and write operations.

Figures 3 and 4 show the timing waveforms of the serial data input.

First, at the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are introduced internally starting with bit 7 in synchronization with the rising SCK edge. At this time, output pin is in the high-impedance state. The output pin is placed in the low-impedance state when the data is output starting with bit 7 synchronized to the falling clock edge during read, status register read and silicon ID.

The LE25FW403A supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

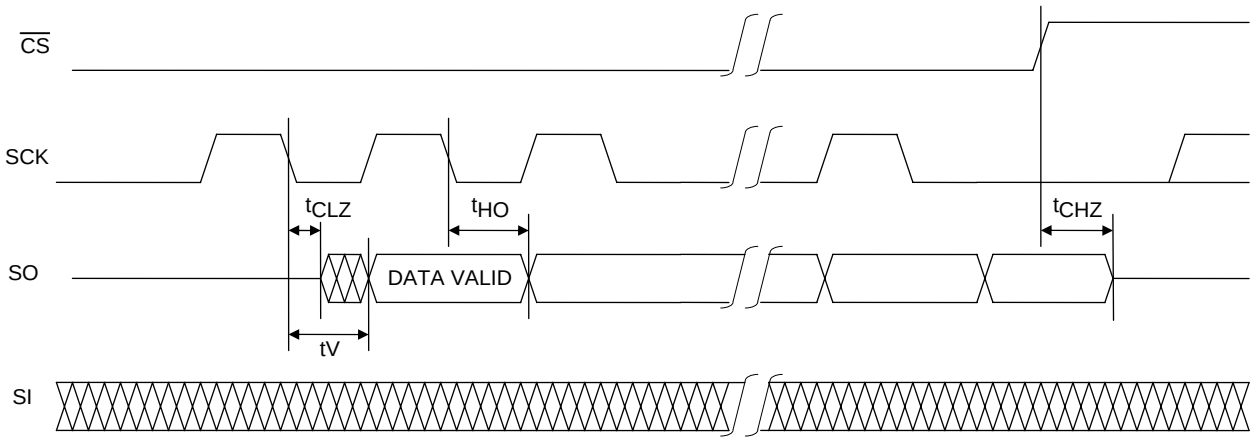
Figure 3 Serial Input Timing



SPI Mode definition

* SPI mode 0: SCK is low logic level when $\overline{CS}$ falls
* SPI mode 3: SCK is high logic level when $\overline{CS}$ falls

Figure 4 Serial Output Timing



Command Definition

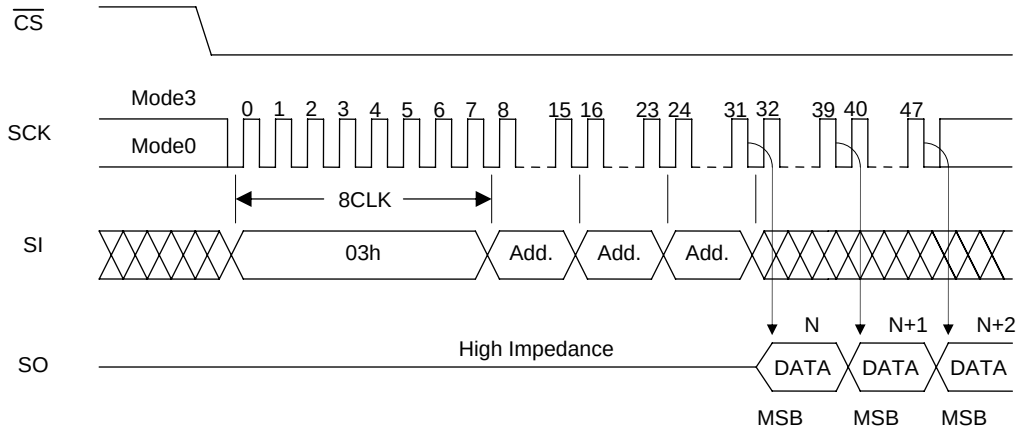
"Table 2 Command Settings" provides a list and overview of the commands. A detailed description of the functions and operations corresponding to each command is presented below.

1. Read

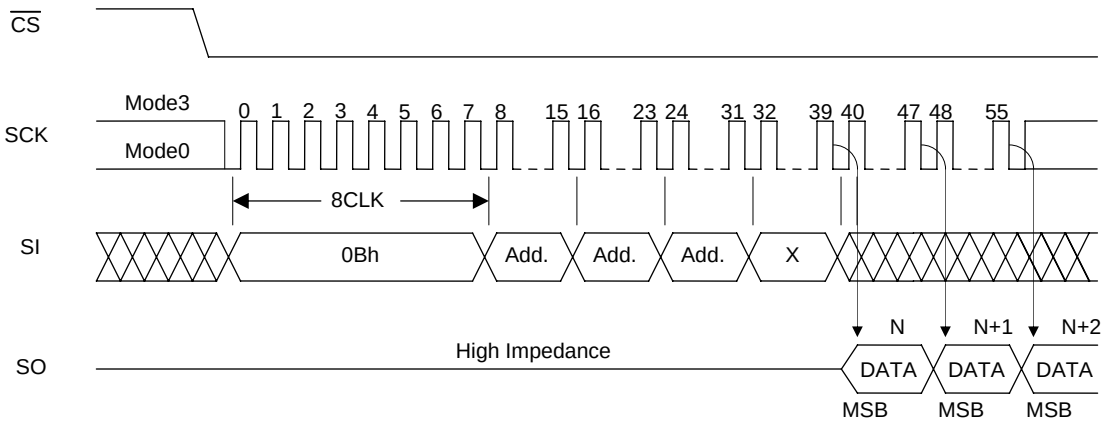
Figure 5 shows the read timing waveforms.
There are two read commands, the 4 bus cycle read and 5 bus cycle read. Consisting of the first through fourth bus cycles, the 4 bus cycle read inputs the 24-bit address following (03h) and the data in the designated address is output synchronized to SCK. The data is output on the falling clock edge of fourth bus cycle bit 0.
Consisting of the first through fifth bus cycles, the 5 bus cycle read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output using the falling clock edge of fifth bus cycle bit 0. The only difference between these two commands is whether the dummy bits in the fifth bus cycle are input.
While SCK is being input, the address is automatically incremented inside the device and the corresponding data is output in sequence.
If the SCK input is continued after the data up to the highest address (7FFFFh) is output, the internal address returns to the lowest address (00000h) and data output is continued.
By setting the logic level of $\overline{CS}$ to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin is in a high-impedance state.

Figure 5: Read

4 Bus Read



5 Bus Read



2. Status Registers

Device status can be detected using status registers.
Table 3 gives the contents of status registers.

Table 3 Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{RDY}$	0	Ready	0
		1	Erase/Program/Write	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2		0	Reserved bits	0
Bit3		0	Reserved bits	0
Bit4		0	Reserved bits	0
Bit5		0	Reserved bits	0
Bit6		0	Reserved bits	0
Bit7		0	Reserved bits	0

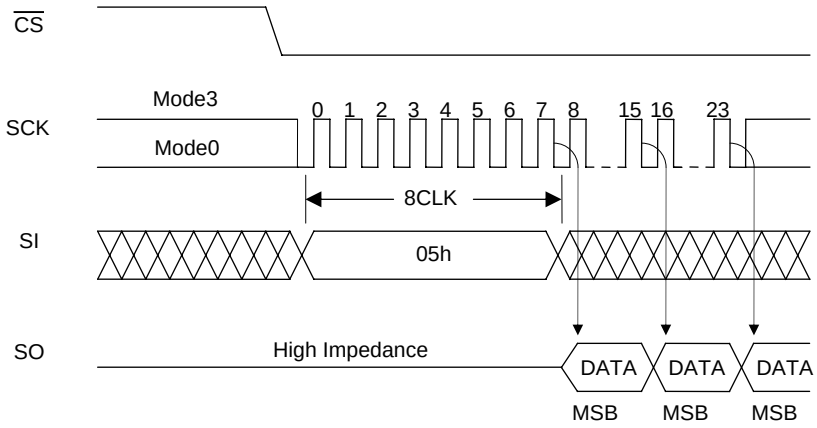
2-1. Status Register Read

The contents of the status registers can be read using the status register read command. This command can be executed even during the following operations.

- Page erase
- Sector erase
- Chip erase
- Page program
- Page write

Figure 6 shows the timing waveforms of the status register read.
Consisting only of the first bus cycle, the status register read command outputs the contents of the status register from bit 7 synchronized to the falling edge of the clock (SCK) when (05h) is input. If the clock (SCK) is continued after data up to $\overline{RDY}$ (bit 0) are output, the data is output by returning to the bit 7. Data is output from the falling clock of the first bus cycle bit 0.

Figure 6 Status Register Read



$\overline{\text{RDY}}$ (bit 0)

The $\overline{\text{RDY}}$ register is for detecting the write (program, erase and page write) end. When it is "1", the device is in a busy state, and when it is "0", it means that write is completed.

WEN (bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not protected.
WEN can be controlled using the write enable and write disable commands. By inputting the write enable command (06h), WEN can be set to "1"; by inputting the write disable command (04h), it can be set to "0." In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.

- At power-on
- Upon completion of page erase, sector erase or chip erase
- Upon completion of page program
- Upon completion of page write
- After hardware reset operations

* If a write operation has not been performed inside the LE25FW403A because, for instance, the command input for any of the write operations (page erase, sector erase, chip erase, page program, or page write) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

Bit2, Bit3, Bit4, Bit5, Bit6, Bit7
These are reserved bits.

3. Write Enable

Write enable command sets the status register WEN to “1.” The write enable command must be issued before performing any of the operations listed below.

- Page erase
- Sector erase
- Chip erase
- Page program
- Page write

Figure 7 shows the timing waveforms. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

4. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. Figure 8 shows the timing waveforms when the write disable operation is performed. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h).
To exit write disable status (WEN = 0), set WEN to 1 using the write enable command (06h).

Figure 7 Write Enable

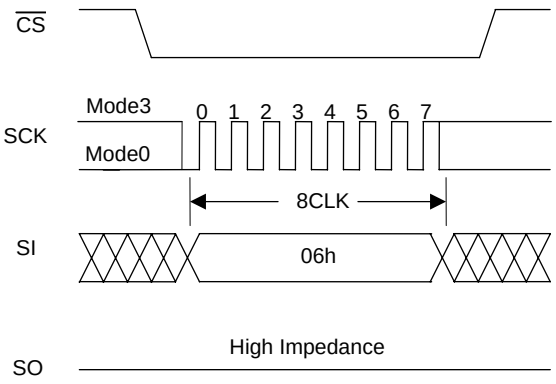
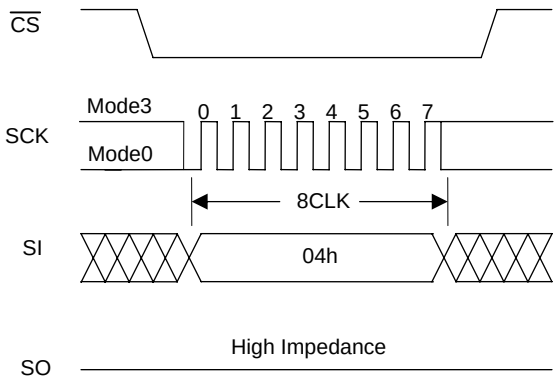


Figure 8 Write Disable



5. Power-down

The power-down command sets all the commands, with the exception of the command to exit from power-down, to the acceptance prohibited state (power-down). Figure 9 shows the timing waveforms. The power-down command consists only of the first bus cycle, and it is initiated by inputting (B9h). The power-down state is exited using the power-down exit command. Figure 10 shows the timing waveforms of the power-down exit command. The power-down exit command consists only of the first bus cycle, and it is initiated by inputting (ABh). Power-down state is exited also when power is tuned off or when hardware reset is performed.

Figure 9 Power-down

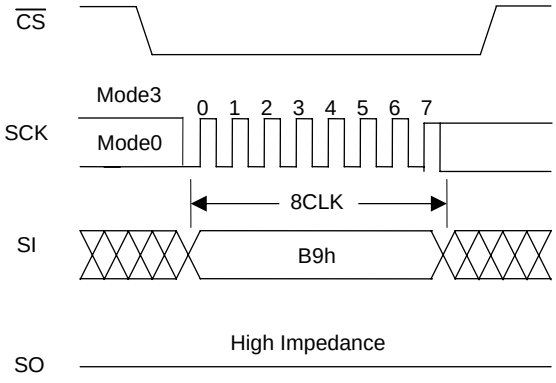
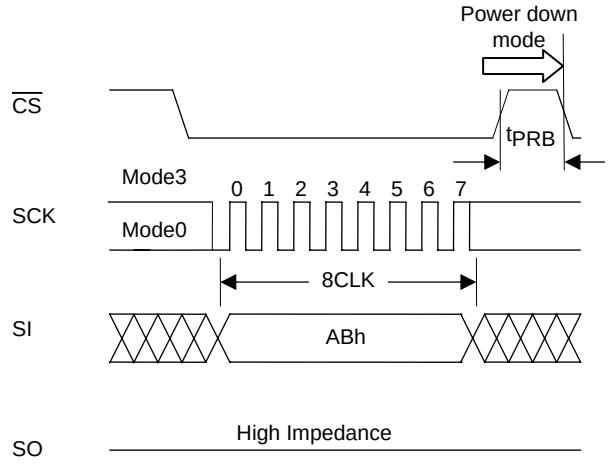


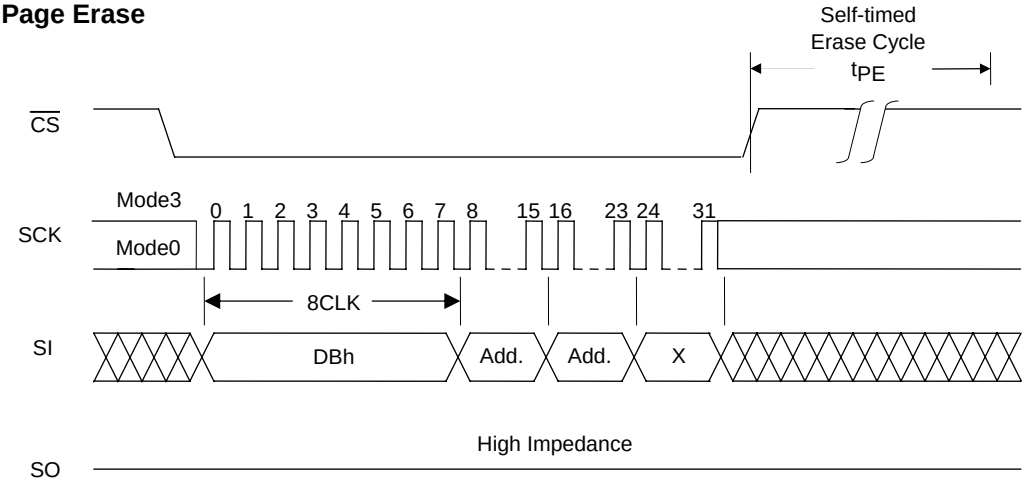
Figure 10 Exiting from Power-down



6. Page Erase

Page erase operation sets the memory cell data in any pages to "1." A page consists of 256 bytes. Figure 11 shows the timing waveforms, and Figure 21 shows a page erase flowchart.
The page erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (DBh). Addresses A18 to A8 are valid, and all others are "don't care."
After the command has been input, the erase operation starts from the rising edge of $\overline{CS}$, and it ends automatically under the control of internal timer. Also, end of erase operation can be detected using status register.
Page erase time depends on the number of rewrites performed. The page erase time is 10ms (typ)/20ms (max) for up to 10^4 rewrites, and 25ms (typ)/300ms (max) for up to 10^5 rewrites.

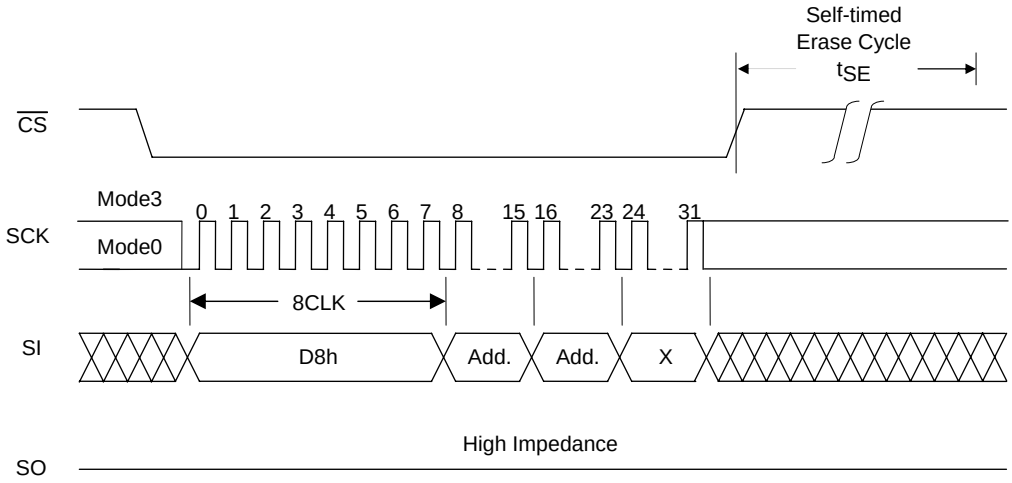
Figure 11 Page Erase



7. Sector Erase

Sector erase operation sets the memory cell data in any sectors to "1." A sector consists of 64K bytes. Figure 12 shows the timing waveforms, and Figure 21 shows an erase flowchart.
The sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D8h). Addresses A18 and A16 are valid, and all others are "don't care."
After the command has been input, the erase operation starts from the rising edge of $\overline{CS}$, and it ends automatically under the control of internal timer. Also, end of erase operation can be detected using status register.
Sector erase time is 30ms (typ)/500ms (max).
If the lower 256 pages are being protected by setting the $\overline{WP}$ pin to low logic level, the sector erase operation cannot be performed on sectors including the lower 256 pages.

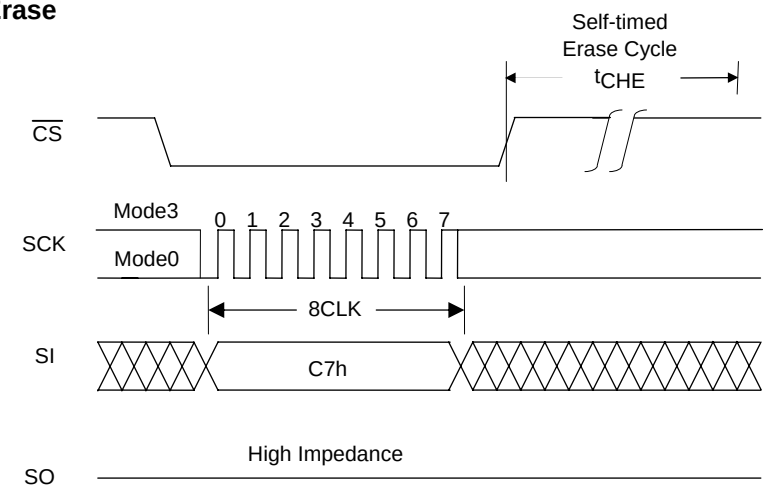
Figure 12 Sector Erase



8. Chip Erase

Chip erase operation sets the memory cell data in all the sectors to "1." Figure 13 shows the timing waveforms, and Figure 21 shows an erase flowchart.
The chip erase command consists only of the first bus cycle, and it is initiated by inputting (C7h).
After the command has been input, the erase operation starts from the rising edge of $\overline{CS}$, and it ends automatically under the control of internal timer. Also, end of erase operation can be detected using status register.
Chip erase time is 300ms (typ)/5s (max).
If the lower 256 pages are being protected by setting the $\overline{WP}$ pin to low logic level, the chip erase operation cannot be performed.

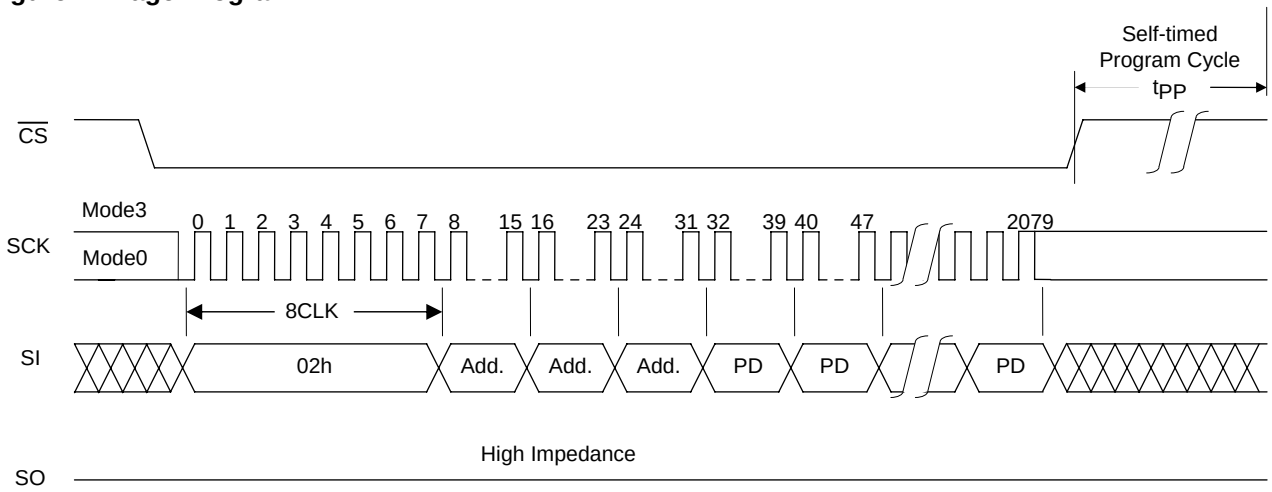
Figure 13 Chip Erase



9. Page Program

Page program operation can be used to program any number of bytes from 1 to 256 bytes for the erased pages (page addresses: A18 to A8).
Figure 14 shows the timing waveforms, and Figure 22 shows a program flowchart.
After $\overline{CS}$ is set low, the command code (02H) is input followed by the 24-bit addresses. Addresses A18 to A0 are valid. After this, the program data can be loaded until $\overline{CS}$ rises. If the loaded data exceeds 256 bytes, the 256 bytes loaded last are programmed.
Also, if the address of data being loaded reaches the last address of a page (A7 to A0: FFh), the device returns to the start address of the same page (A7 to A0: 00h).
Program data must be loaded in 1-byte units. The program operation is not performed if data is loaded in less than byte units and $\overline{CS}$ is set high.
The page program time depends on the number of bytes programmed. When programming 256 bytes, the page program time is 1.5ms (typ)/2.5ms (max).

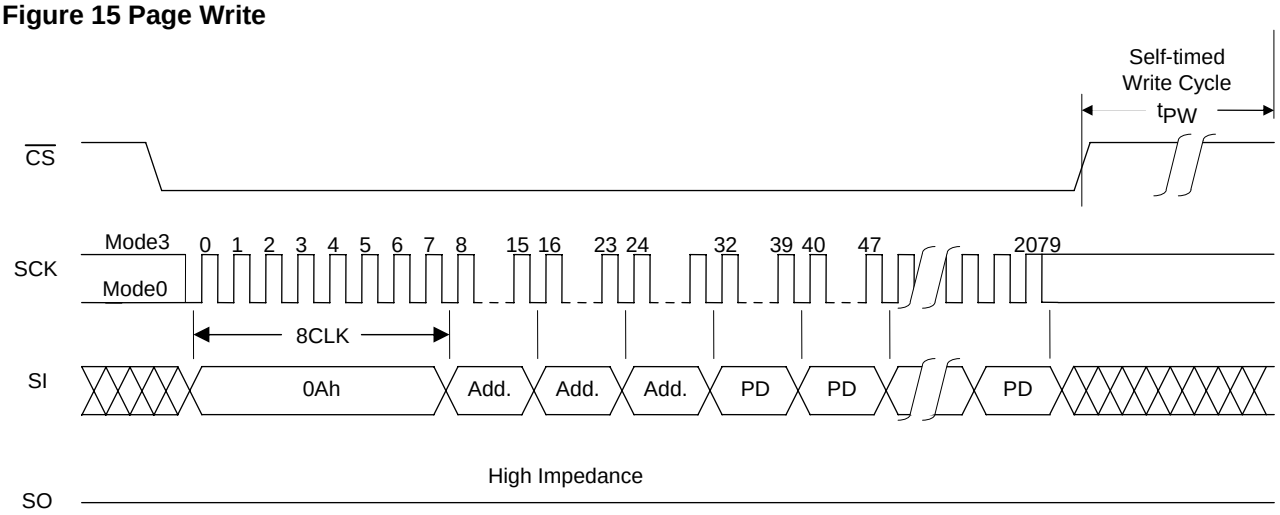
Figure 14 Page Program



10. Page Write

Page write operation can be used to rewrite any number of bytes of data from 1 to 256 bytes in a page (page addresses: A18 to A8) without executing erase operation beforehand. Figure 15 shows the timing waveforms, and Figure 23 shows a flowchart. After $\overline{CS}$ is set low, the command code (0AH) is input followed by the 24-bit addresses. Addresses A18 to A0 are valid. After this, re-write data can be loaded until $\overline{CS}$ rises. If loaded data exceeds 256 bytes, the 256 bytes loaded last are programmed. If the loaded data is less than 256 bytes, data not loaded on the same page is not rewritten. In addition, if the address of data being loaded reaches the last address of a page (A7 to A0: FFh), the device returns to the start address of the same page (A7 to A0: 00h).
Rewrite data must be loaded in 1-byte units. The rewrite operation is not performed if data is loaded in less than byte units and $\overline{CS}$ is set high. The page write time depends on the number of rewrites. The page write time is 11ms (typ)/22.5ms (max) for up to 10^4 rewrites, or 25ms (typ)/300ms (max) for up to 10^5 rewrites.

Figure 15 Page Write



11. Silicon ID Read

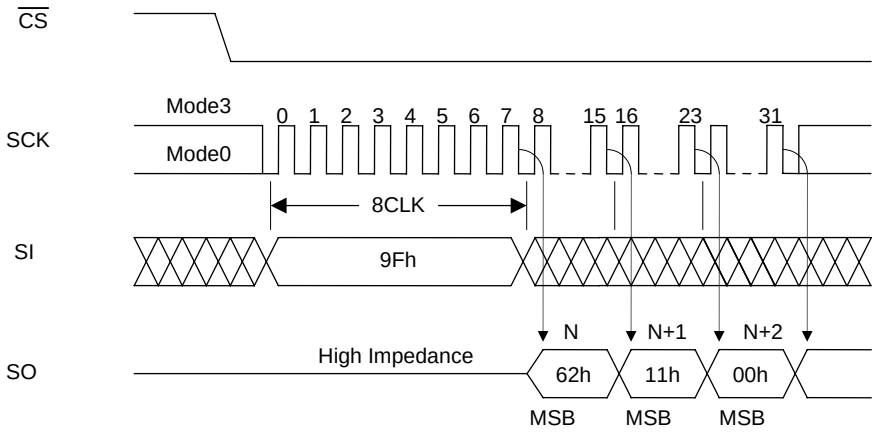
Silicon ID read allows manufacturer code and device code information to be read. Figure 16 shows the timing waveforms, and Table 6 gives the silicon ID codes.

Table 6 Silicon ID Codes

	Output Code
Manufacturer code	62h
Device code	11h
Dummy code	00h

The silicon ID read command consists of only the first bus cycle. If (9Fh) is input, the manufacturer code 62h, device code 11h, and dummy code 00h are output in synchronization with the falling edge of SCK. If SCK input continues, the IC repeatedly outputs the data described above.
Data output is performed from the falling edge of clock at the first bus cycle, bit 0. Silicon ID read is terminated by making $\overline{CS}$ go to high logic level.
The silicon ID read command is not accepted during write operations.

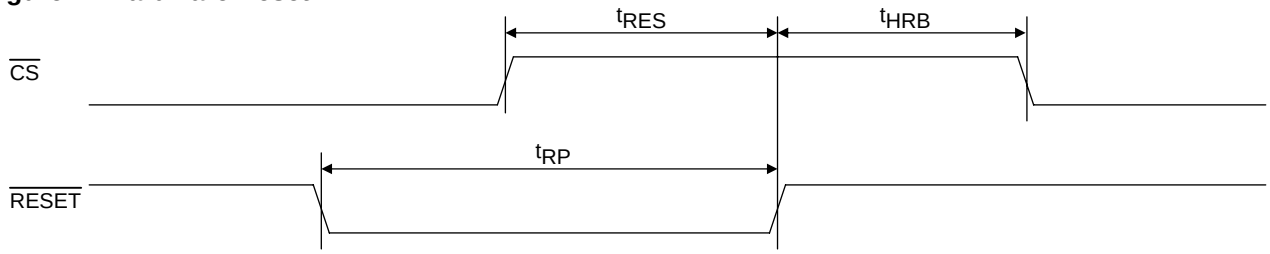
Figure 16 Silicon ID Read



12. Hardware Reset

A hardware reset can be performed by setting the $\overline{\text{RESET}}$ pin to low logic level. Figure 17 shows the timing waveforms. The hardware reset is disabled while write operation (erase, program, or page write) is being executed in the device. The pin SO is held in the high-impedance state while the device is in the reset mode.

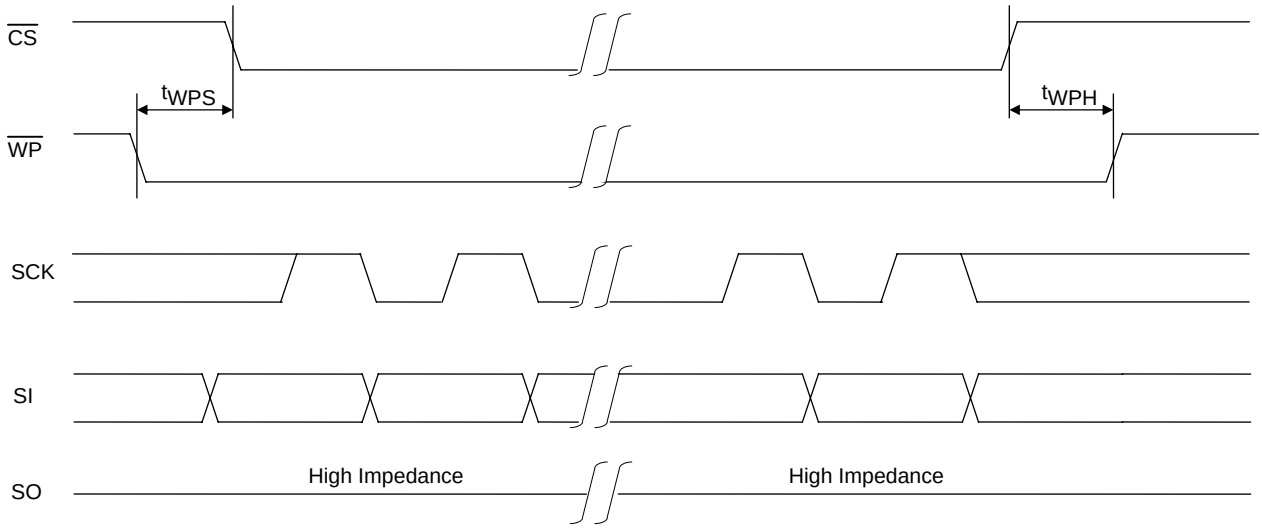
Figure 17 Hardware Reset



13. Hardware Data Protection

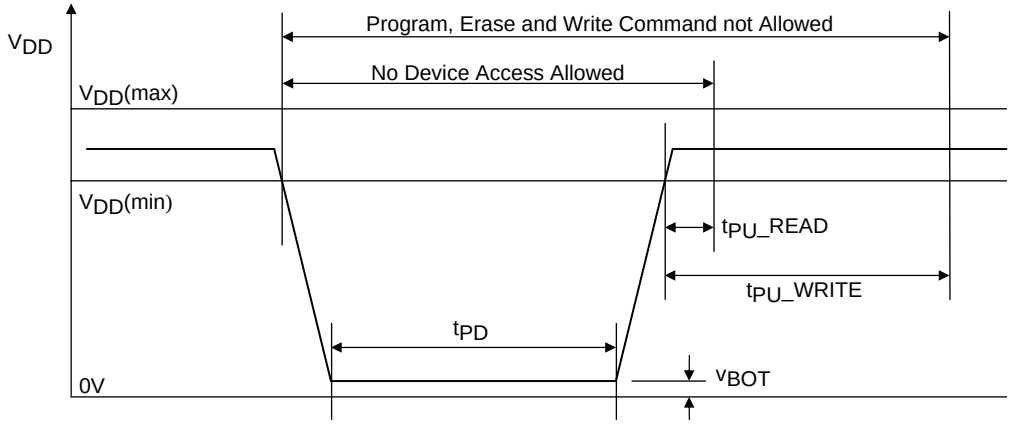
Lower 256 pages can be protected by setting the $\overline{\text{WP}}$ pin to low logic level. Figure 18 shows the timing waveforms. In addition, the device has an internal power on reset function to prevent unintentional write operations at power on.

Figure 18 Write Protection



In order to protect against unintentional writing at power-on, the LE25FW403A incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.
No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 19 Power-down Timing



14. Software Data Protection

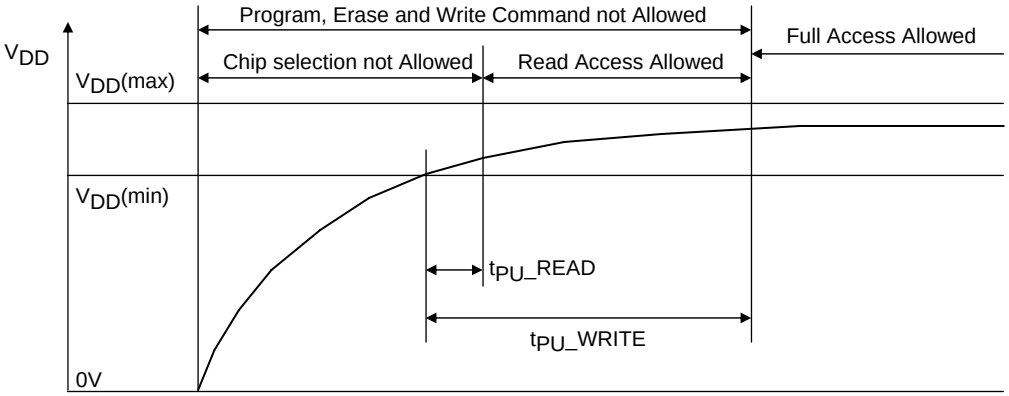
The LE25FW403A eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

- When a write command is input and the rising $\overline{CS}$ edge timing is not in a bus cycle (8 CLK units of SCK)
- When the page program and page write data is not in 1-byte increments

15. Power On

V_{DD} is applied to $\overline{CS}$ at power on to prevent unintentional write operations.
To start read operations, turn the power on and input a command 100μs (t_{PU}_READ) after the power supply voltage has reached 2.7V or higher and has been stabilized.
In addition, to start write operations, turn the power on and input a command 10ms (t_{PU}_WRITE) after power supply voltage has reached 2.7V or higher and has been stabilized.

Figure 20 Power On Timing



16. Decoupling Capacitor

A 0.1μF ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage		With respect to V_{SS}	-0.5 to +4.6	V
DC voltage (all pins)		With respect to V_{SS}	-0.5 to V_{DD}+0.5	V
Storage temperature	Tstg		-55 to +150	°C

Operating Conditions

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage			2.7 to 3.6	V
Operating ambient temperature			0 to 70	°C

Allowable DC Operating Conditions

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Read mode operating current	I_{CCR}	$\overline{CS}$=0.1V_{DD}, $\overline{RESET}$=$\overline{WP}$=0.9V_{DD} SI=0.1V_{DD}/0.9V_{DD}, SO=open, Operating frequency=30MHz, V_{DD}=V_{DD} max			6	mA
Write mode operating current	I_{CCW}	V_{DD}=V_{DD} max			15	mA
CMOS standby current	I_{SB}	$\overline{CS}$=$\overline{RESET}$=$\overline{WP}$=V_{DD}-0.3V, SI=V_{SS}/V_{DD}, SO=open, V_{DD}=V_{DD} max			10	μA
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{DD}, V_{DD}=V_{DD} max			2	μA
Output leakage current	I_{LO}	V_{IN}=V_{SS} to V_{DD}, V_{DD}=V_{DD} max			2	μA
Input low voltage	V_{IL}	V_{DD}=V_{DD} max	-0.3		0.3V_{DD}	V
Input high voltage	V_{IH}	V_{DD}=V_{DD} min	0.7V_{DD}		V_{DD}+0.3	V
Output low voltage	V_{OL}	I_{OL}=100μA, V_{DD}=V_{DD} min			0.2	V
		I_{OL}=1.6mA, V_{DD}=V_{DD} min			0.4	
Output high voltage	V_{OH}	I_{OH}=-100μA, V_{DD}=V_{DD} min	V_{DD}-0.2			V

Power-on Timing

Parameter	Symbol	Ratings		unit
		min	max	
Time from power-on to read operation	t_{PU_READ}	100		μs
Time from power-on to write operation	t_{PU_WRITE}	10		ms
Power-down time	t_{PD}	10		ms
Power-down voltage	v_{BOT}		0.2	V

Pin Capacitance at Ta=25°C, f=1MHz

Parameter	Symbol	Conditions	max	unit
Output pin capacitance	C_{DQ}	V_{DQ}=0V	12	pF
Input pin Capacitance	C_{IN}	V_{IN}=0V	6	pF

Note: These parameter values do not represent the results of measurements undertaken for all devices but rather values for some of the sampled devices.

AC Characteristics

Parameter		Symbol	Ratings			unit
			min	typ	max	
Clock frequency		f_{CLK}			30	MHz
Input signal rising/falling time		t_{RF}			20	ns
$\overline{CS}$ setup time		t_{CSS}	10			ns
$\overline{CS}$ hold time		t_{CSH}	10			ns
$\overline{CS}$ wait pulse width		t_{CPH}	25			ns
Output high impedance time from $\overline{CS}$		t_{CHZ}			15	ns
Data setup time		t_{DS}	5			ns
Data hold time		t_{DH}	5			ns
SCK setup time		t_{CLS}	10			ns
SCK hold time		t_{CLH}	10			ns
SCK logic high level pulse width		t_{CLHI}	16			ns
SCK logic low level pulse width		t_{CLLO}	16			ns
Output low impedance time from SCK		t_{CLZ}	0			ns
Output data time from SCK		t_V		8	15	ns
Output data hold time		t_{HO}	0			ns
Page erase cycle time	Number of rewrite times: 10^4 times or less	t_{PE}		10	20	ms
	Number of rewrite times: 10^5 times or less			25	300	ms
Sector erase cycle time		t_{SE}		30	500	ms
Chip erase cycle time		t_{CHE}		0.3	5	s
Page programming cycle time (256 bytes)		t_{PP}		1.5	2.5	ms
Page programming cycle time (n bytes)				0.04+ n*1.46/256		
Page write cycle time	Number of rewrite times: 10^4 times or less	t_{PW}		11	22.5	ms
	Number of rewrite times: 10^5 times or less			25	300	ms
$\overline{WP}$ setup time		t_{WPS}	50			ns
$\overline{WP}$ hold time		t_{WPH}	50			ns
Reset setup time		t_{RES}	10			ns
Reset pulse width		t_{RP}	100			ns
Hardware reset recovery time		t_{HRB}	1			µs
Power-down recovery time		t_{PRB}	25			ns

AC Test Conditions

Input pulse level·····0V, 3.0V
Input rising/falling time·····5ns
Input/Output timing level·····High data: 2.0V, Low data: 0.8V
Output load·····30pF

Note: As the test conditions for "typ", the measurements are conducted using 3.0V for V_{DD} at room temperature.

Figure 21 Erase Flowchart

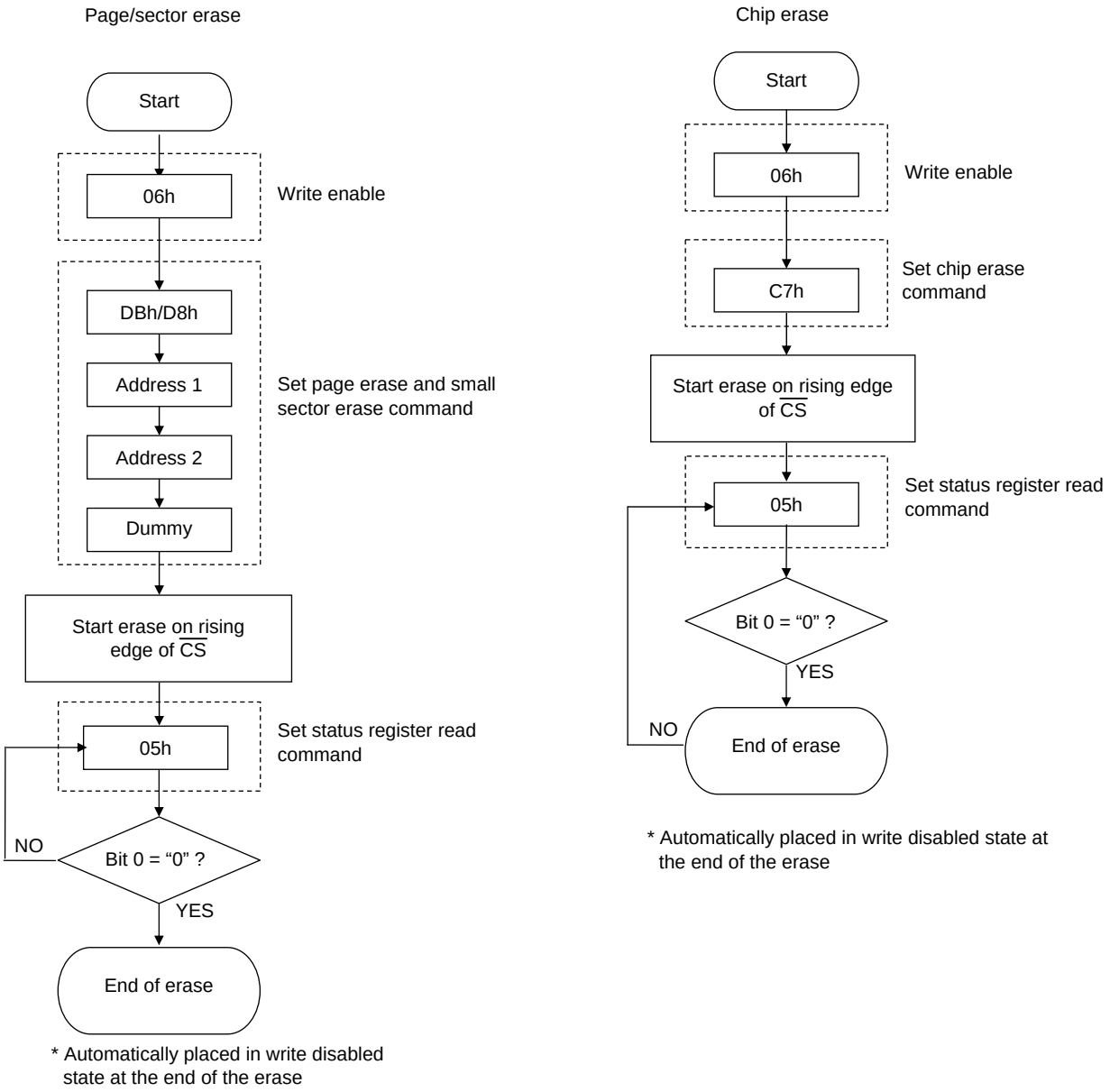
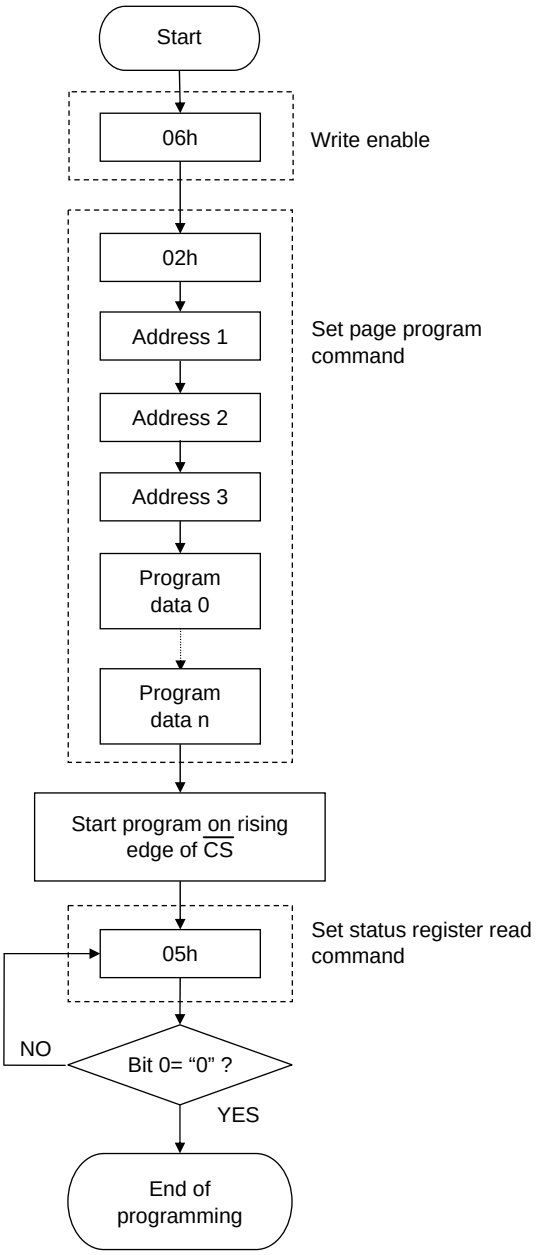
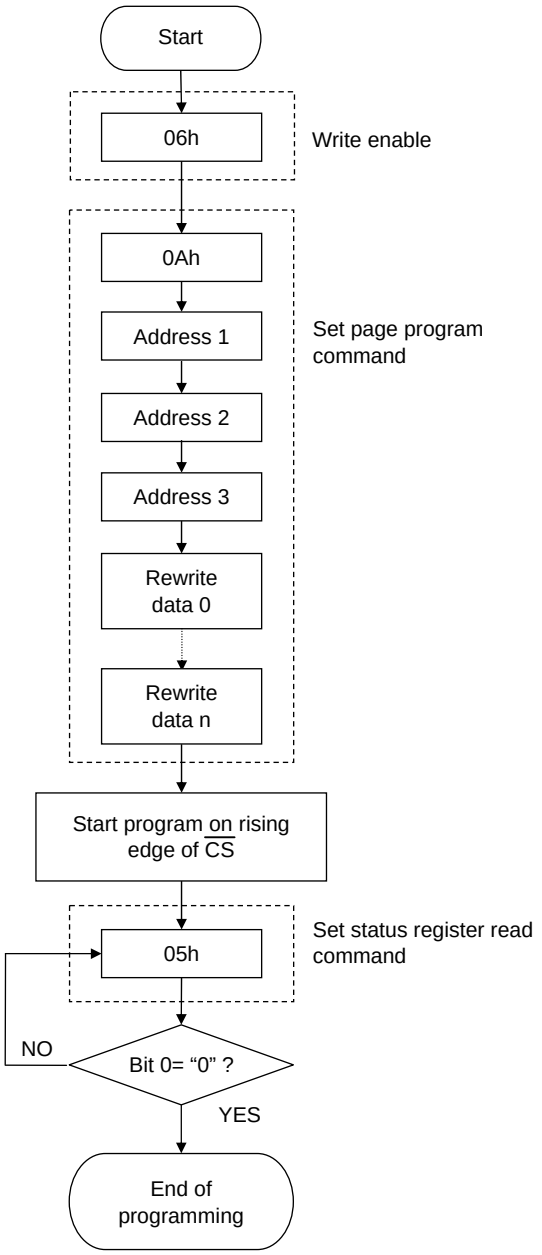


Figure 22 Program Flowchart



* Automatically placed in write disabled state at the end of the programming operation.

Figure 23 Page Write Flowchart



* Automatically placed in write disabled state at the end of the programming operation.